Power Amplifier Design Methodology

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12/03/2018

Typical Class-A PA Power Densities and R_{LOPT}

- 90/65nm CMOS
  - $V_{MAX} = 1.5V$, $J_{sat,p} = 0.6\frac{mA}{\mu m}$; $P_{sat} = 0.11\frac{mW}{\mu m}$; $R_{LOPT} = 2.5k\Omega \cdot \times m$.
- $0.15\mu m$ GaN FET
  - $V_{MAX} = 40V$, $J_{sat,p} = 1\frac{mA}{\mu m}$; $P_{sat} = 5\frac{mW}{\mu m}$; $R_{LOPT} = 40k\Omega \cdot \times m$.
- 50GHz GaAs HBT
  - $V_{MAX} = 6V$, $J_{sat,p} = 0.5\frac{mA}{\mu m}$; $P_{sat} = 0.375\frac{mW}{\mu m}$; $R_{LOPT} = 12k\Omega \cdot \times m$.
- 230GHz SiGe HBT
  - $V_{MAX} = 3V$, $J_{sat,p} = 3.9\frac{mA}{\mu m}$; $P_{sat} = 1.5\frac{mW}{\mu m}$; $R_{LOPT} = 770\Omega \cdot \times m$.

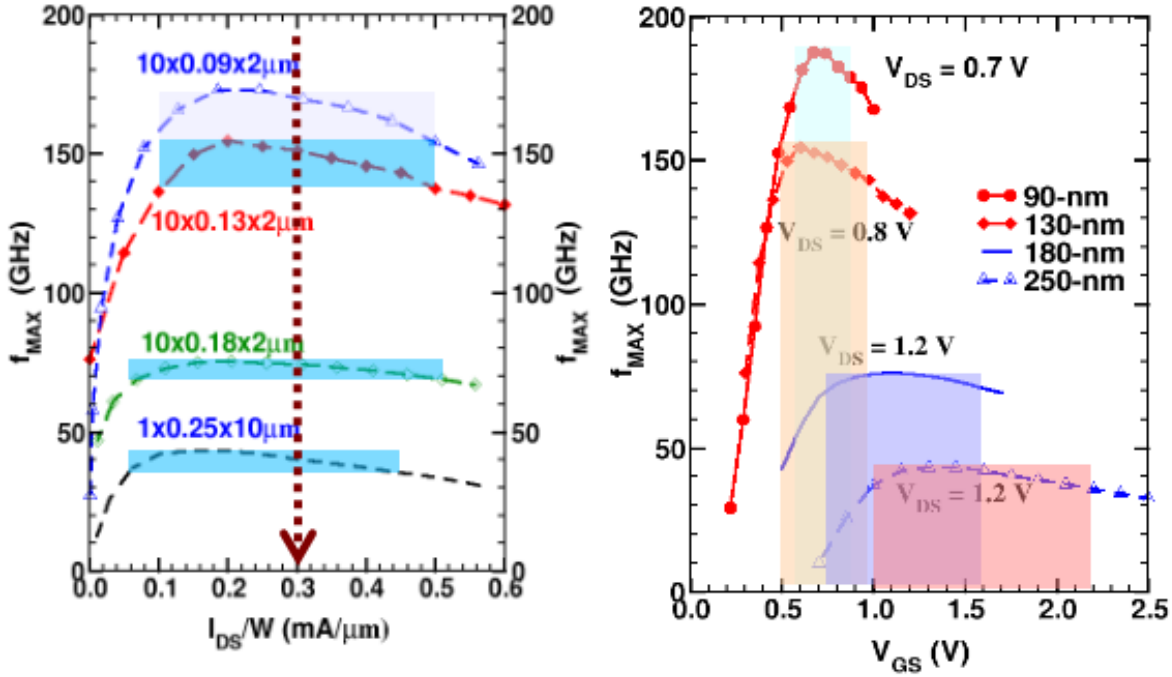
Example of 1W PA Design (through 40GHz)

- 90/65nm CMOS: W=0.09mm; $R_{LOPT} = 0.27\Omega$ (impossible to match to 50Ω)
- 150nm GaN FET: W=0.2mm; $R_{LOPT} = 200\Omega$ (each to match from 50Ω)
- 50GHz GaAs HBT: I_E=2.66mm; $R_{LOPT} = 4.5\Omega$ (possible to match to 50Ω)
- 230GHz SiGe HBT: I_E=0.67mm; $R_{LOPT} = 1.16\Omega$ (possible but difficult to match from 50Ω)
  Conclusion: Need a high voltage device for $> 1W$ or $> +30dBm$ power level.

PA Design Equations (1)

- Linear swing of a class-A PA depends on the flatness of the f_{MAX} vs J_D characteristics
- OP_{1dB} is maximized when the transistor is biased at the peak f_T current density, J_{pfT}
- SiGe HBT J_{pfT} increases as square of the technology scaling factor
  - Despite of reduction in breakdown voltage, large output power can be obtained in the newer technology nodes
  - Enables higher ferquency designs
- In CMOS, linear voltage swing at the input/output decreases with each new node while J_{pfT} remains largely constant at $0.3 - 0.4\frac{mA}{\mu m}$
  - In CMOS PAs, the OP_{1dB} current swing $J_{swing,pp}$ remains largely constant across nodes at $\approx 0.4\frac{mA_{pp}}{\mu m}$, to avoid transistor cutoff

PA Design Equations (2)



- The OP_{1dB} can be directly linked to technology data and W

$$OP_{1dB} = W \cdot J_{swing,pp} \frac{(V_{DD} - V_{DSsat})}{4}$$

$$= W \cdot J_{swing,pp} \frac{(V_{MAX} - V_{DSsat})}{8}$$

only valid when the output is terminated on R_{LOPT}

PA Design Equations (3)

- To obtain saturated output power P_{SAT}, the corresponding current swing $J_{sat,pp}$ is $0.6 - 0.7\frac{mA_{pp}}{\mu m}$ for nFETs and $2 \cdot J_{pfT}$ fro HBTs
- The maximum current that can pass through a MOSFET is limited by I_{ON}
  - continues to increase with CMOS scaling
  - I_{ON} values as high as $1.3\frac{mA}{\mu m}$ and $1\frac{mA}{\mu m}$ have been reported in 45nm NMOS and PMOS respectively.
- For class A, B, and AB PAs, the maximum voltage swing $V_{sat,pp}$ of the fundamental at P_{SAT} is $\approx 2V_{DD}$, which is limited by V_{MAX}
  - The maximum peak-to-peak current swing at the fundamental frequency is limited by $J_{sat,pp}$
  - Thus, the saturated output power for these PA classesu is limited by

$$P_{sat} = \frac{WJ_{sat,pp}V_{DD}}{4} = \frac{WJ_{sat,pp}V_{MAX}}{8}$$

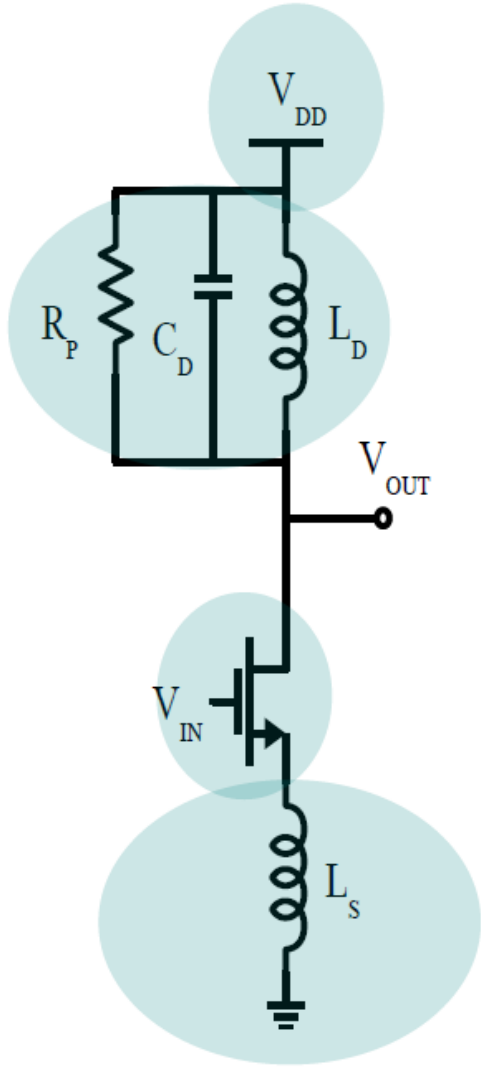
mmWave Class-A PAs: Need for Multi-Stage Design

- Multistage PA topologies are essential to obtain adequate gain at mmWaves, esp. in CMOS
- $\approx 8-10dB$ MAG of a 90nm or 65nm CMOS is degraded by $3-4dB$
  - due to the limited load impedance that can be realized at the drain output at high frequencies, and
  - due to the losses of the matching networks
- The optimal distribution of power gain and bias current (and hence P_{1dB}) across the gain stages can be obtained by inspecting the expression

$$\frac{1}{OP_{1dB_{cascade}}} = \frac{1}{OP_{1dB_3}} + \frac{1}{OP_{1dB_2} \cdot G_3} + \frac{1}{OP_{1dB_1} \cdot G_2 \cdot G_3}$$

- In order to minimize the power consumption and to improve the efficiency of the overall PA for the given OIP_{1dB}, the gain and voltage swing of each stage must be maximized.

Schematic of the Output Stage used for the Design Methodology



mmWave class-A PA Design Algorithm (1)

- **Step 1:** Starting at the output stage, determine the maximum allowed voltage swing for the given technology.
  - From the load line theory, the optical linearity and output power are obtained when the transistor is biased such that the drain voltage swings equally between $V_{DS,sat}$ and V_{MAX}, centered at V_{DD}.
  - V_{MAX} is dictated by the breakdown or reliability limit.
  - Thus, the maximum voltage swing is $V_{swing} = V_{MAX} - V_{DS,sat}$, where $V_{MAX} = 2V_{DD} - V_{DS,sat}$
- **Step 2:** Set the bias current density to $J_{pfT} = 0.3 - 0.4\frac{mA}{\mu m}$ to maximum linearity.

mmWave class-A PA Design Algorithm (2)

- **Step 3:** Determine the bias current that meets the P_{1dB} requirements and, from that find W.
  - An expression for P_{1dB} can be derived from the load line theory

$$P_{1dB} = I_{swing}\frac{(V_{DD} - V_{DS,sat})}{4}$$

    where $I_{swing} = 0.4\frac{mA}{\mu m} \cdot W$ is the maximum current swing before 1dB compression, instead of $2 \cdot I_{DC}$
  - In most scaled CMOS technologies, the value of VDS, sat corresponding to the optimal linearity bias point of $0.3\frac{mA}{\mu m}$ is about 0.3V.
  - We have $W = 4\frac{P_{1dB}}{0.4\frac{mA_{pp}}{\mu m}\cdot(V_{DD}-VDS,sat)}$ and $I_{DC} = W \cdot 0.3\frac{mA}{\mu m}$.
- **Step 4:** Add a degeneration inductor L_S to improve stability.
  - Otherwise, the input resistance can become negative for an inductively loaded CS stage.
  - Iterations may be needed since L_S also changes MAG.
  - The degeneration inductor also improves linearity.

mmWave class-A PA Design Algorithm (3)

- **Step 5:** Add an output matching network (to transform from Z_0 to R_{LOPT}) for the last stage and (if necessary) inter-stage matching networks for intermediate stages to maximize power transfer.
- **Step 6:** Repeat steps 1-5 for each preceding stage with the V_{swing} determined by V_{input} for the subsequent stage to avoid gain compression.
- **Step 7:** Design the first stage to be input-matched to $Z_0 = 50\omega$. A cascode topology may be used in the first stage for higher gain.
  In multistage PAs, the size and bias current of transistor increase towards the output.

Example: A 65nm CMOS Output Stage with P_{1dB} of 7dBm at 60GHz

- **Given:** $V_{DD} = 0.7V$, $V_{DS,sat} = V_{MIN} = 0.2V$ at $0.3\frac{mA}{\mu m}$
- **Goal:** $OIP_{1dB} = 7dBm = 5mW$
- We determine $V_1 = V_{DD} - VDS, sat = 0.5V$ or $1V_{pp}$ and $V_{MAX} = 1.5V$
- From $OIP_{1dB} = 5mW = \frac{V_1 \cdot I_{swing}}{4}$
  - $\Longrightarrow I_{swing} = 40mA_{pp}$ and $W = \frac{I_{swing}}{0.4\frac{mA_{pp}}{\mu m}} = 100\mu m$
- $R_{LOPT(P_{1dB})} = \frac{2V_1}{I_{swing}} = \frac{1000}{40} = 25\Omega$
  - The corresponding DC bias current in the output transistor is $I_{DC} = W \cdot 0.3\frac{mA}{\mu m} = 30mA$
  - $P_{DC} = I_{DC} \cdot V_{DD} = 30mA \cdot 0.7V = 21mW$
  - $\eta = 22.2\%$
- Note that we ignored the losses in the output matching network due to its finite Q.

Example: A SiGe HBT Output Stage at 60GHz

- **Given:** $V_{CC} = 1.5V$. The J_{pfT} is $2\frac{mA}{\mu m}$, the linear current swing at J_{pfT} bias is$3\frac{mA_{pp}}{\mu m}$, and $V_{CE,sat} = V_{MIN} = 0.5V$.
- **Goal:** $OIP_{1dB} = 10dBm = 10mW$
- We determine $V_1 = V_{CC} - VCE, sat = 1V$ or $2V_{pp}$ and $V_{MAX} = 2.5V$
- From $OIP_{1dB} = 10mW = \frac{V_1 \cdot I_{swing}}{4}$
  - $\Longrightarrow I_{swing} = 40mA_{pp}$ and $I_E = \frac{I_{swing}}{3\frac{mA_{pp}}{\mu m}} = 13.3\mu m$
- $R_{LOPT(P_{1dB})} = \frac{2V_1}{I_{swing}} = \frac{2000}{40} = 50\Omega$
  - The corresponding DC bias current in the output transistor is $I_{DC} = I_E 2\frac{mA}{\mu m} = 26.7mA$
  - $P_{DC} = I_{DC} \cdot V_{DD} = 26.7mA \cdot 1.5V = 40mW$
  - $\eta = 25\%$
- The output matching network is simplified because it only needs to tune out the reactance of the output transistor.
- Note that we ignored the losses in the output matching network due to its finite Q.

Computer-based Algorithmic Class-A PA Design Methodology to Obtain a Target $OP_{1dB}(1)$

- **Step 1:** Start with a periodic S-parameter simulation at the desired frequency of operation.
  - Bias the transistor at the maximum linearity bias current density.
  - Use the transistor size calculated by hand analysis and 50Ω input and output ports.
  - Plot MAG as a function of P_{in} and find IP_{1dB}. This corresponds to $OP_{1dB} = IP_{1dB} + MAG$.
  - Set this OP_{1dB} power level to be at least 1-2dBm larger than the target. Otherwise will need to increase the transistor size.
- **Step 2:** Plot the real and imaginary parts of Z_{in} and Z_{out}. Examine their values at the IP_{1dB} input power level and conjugate match the input and output at this input/output power level.

Computer-based Algorithmic Class-A PA Design Methodology to Obtain a Target $OP_{1dB}(2)$

- **Step 3:** Re-run the periodic S-parameter simulation on the matched amplifier and plot P_{out} versus P_{in}, Gain versus P_{in} and PAE versus P_{in}.
  - A load-pull simulation should be conducted to further tweak the output impedance and to obtain the maximum possible output power.
  - If you still cannot achieve the desired output power, repeat Steps 1-2 after further increasing transistor sizes.

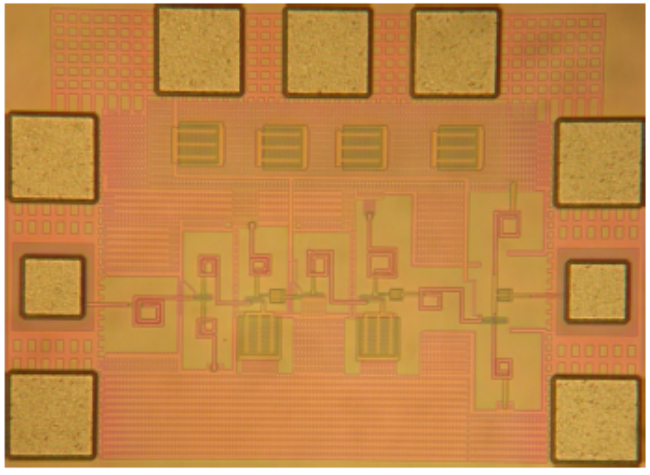
PA Output Power Control

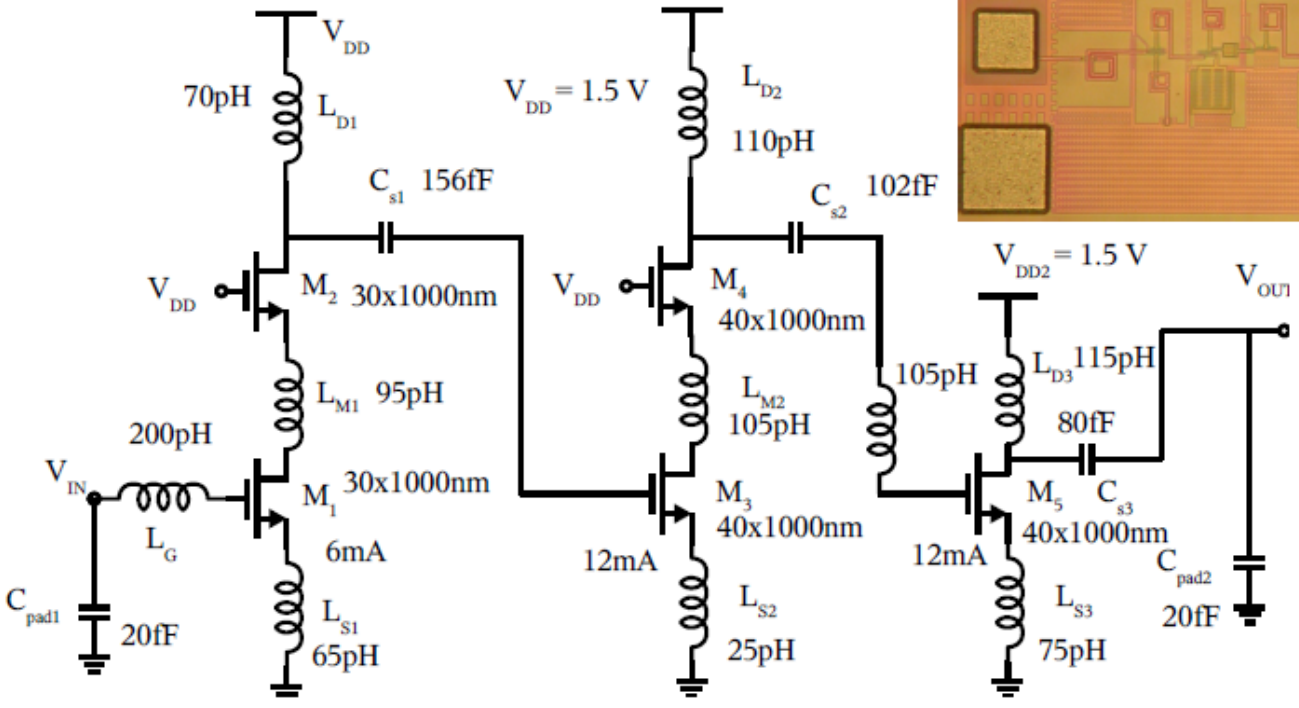
- The TX power level is usually specified by the various IEEE standards.
- Most of these standards mandate at least some capability to dynamically control the output power level.
- Its also desirable that the efficiency of the PA doesn't degrade as the output power is reduced (or **back-off**).
- Several techniques have been developed for improving back-off energy efficiency.

PA Linearity

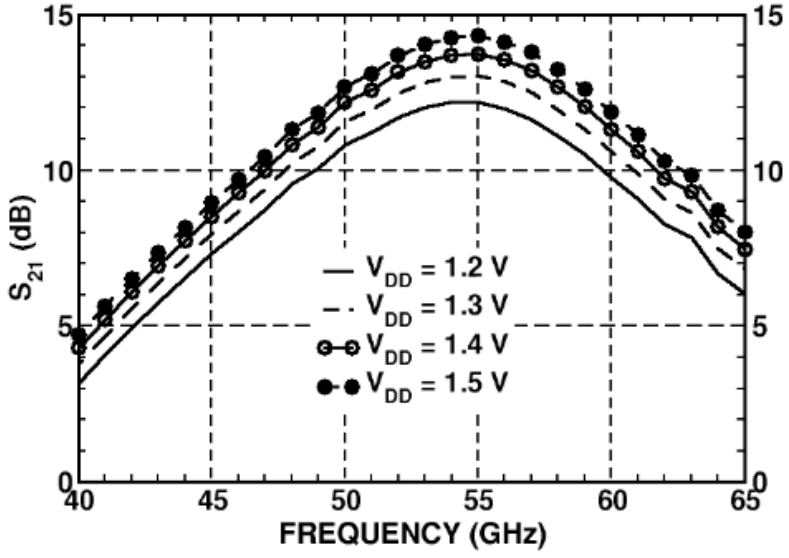
- Methods to improve PA linearity remain very attractive area of research.
- Two transmitter specification parameters address the PA linearity performance.
  - The spectral mask
  - The error vector magnitude (EVM) of the output signal
- Depending upon the modulation format, the PA design is either limited by the spectral mask or by the EVM specification.
- In general, in higher data-rate standards, which require more complex modulations and higher BW efficiency, the EVM specification is more difficult to satisfy.

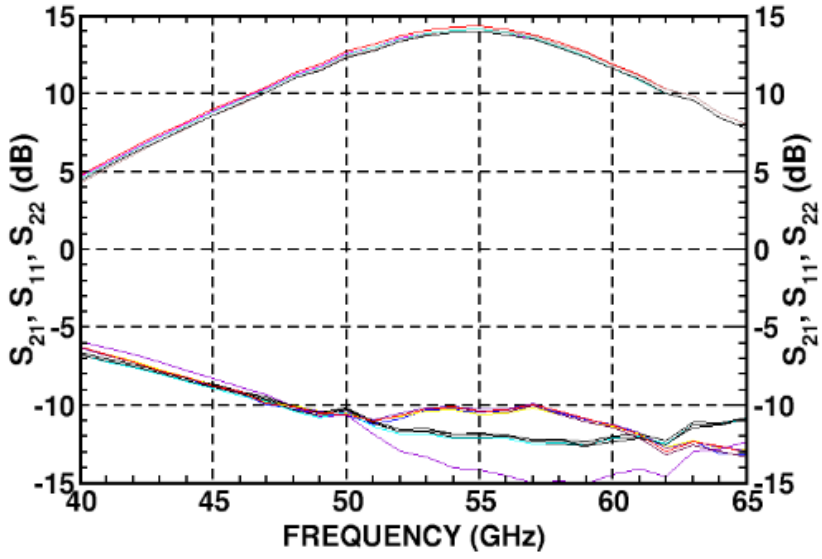
2-Stage Cascode PA with CS Output Stage in 90nm CMOS (1)



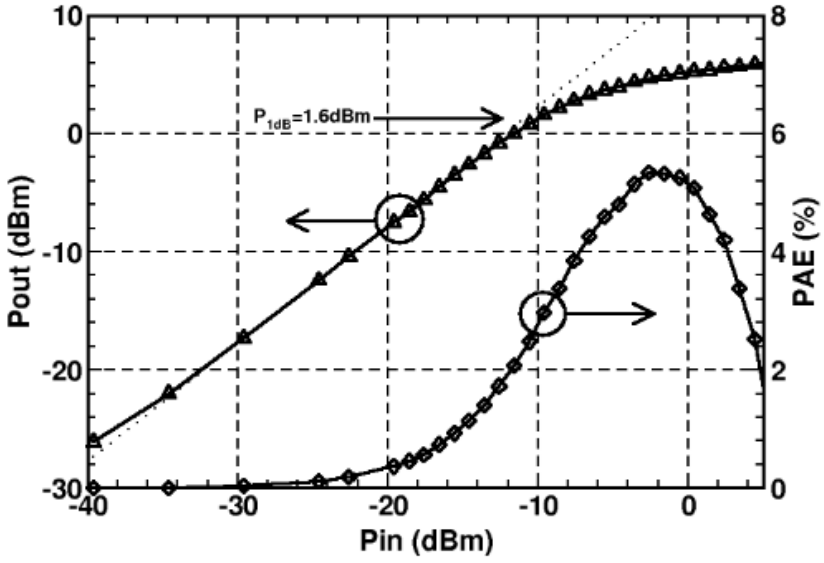


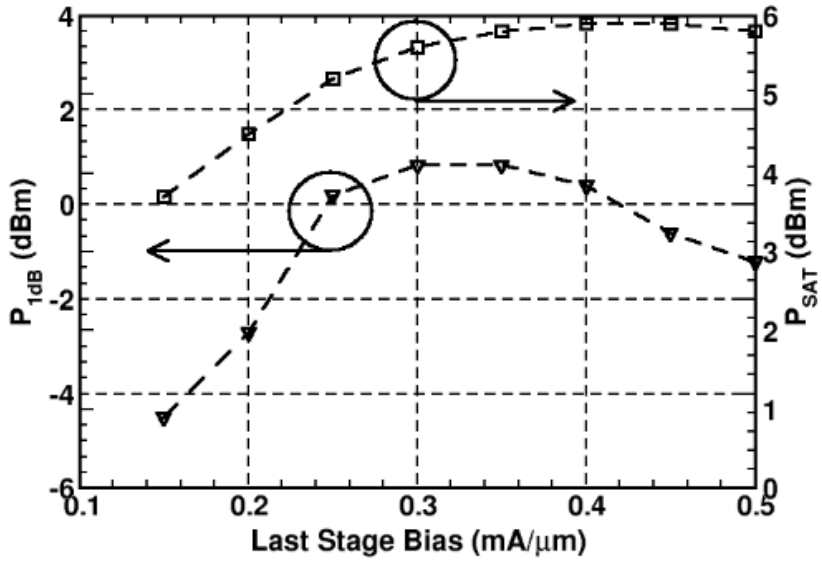
2-Stage Cascode PA with CS Output Stage in 90nm CMOS (2)





2-Stage Cascode PA with CS Output Stage in 90nm CMOS (3)





Other PA Concepts (Read in the Textbook)

- Non-idealities in PA
  - Drain inductance
  - Thermal runaway in Bipolar PAs
  - Avalanche breakdown
- Efficiency enhancement techniques
  - Dynamic biasing
  - PA subranging
  - Envelope tracking
  - PWM modulated class-E PA with envelop restoration
  - Doherty amplifier
  - Dephasing
  - Digital Predistortion

Other PA Concepts (Read in the Textbook)

- Power combining techniques
  - Transformer based power combining
  - Series stacking of transistors (super-cascode)
  - Spatial power combining

References

- S. Voinigescu, "High-Frequency Integrated Circuits," The Cambridge RF and Microwave Engineering Series, 1st ed., 2013.