Mixer Design Methodology

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Mixer Specifications

- RF, LO, IF frequencies
- Conversion (power) gain
- Linearity
- Noise Figure (receive/downconversion mixers only)
- Isolation

Receive (down-converter) mixer topology

- Doubly balanced
- Good for MOS, BJT and BiCMOS
- RF (low-noise) linear input amplifier + mixing quad
- RF signal applied to bottom pair
- LO signal applied to mixing quad
- IF LPF output
- LO and or RF trap at IF output
- Image rejection must be placed before mixing quad or built into the topology.

Transmit (up-converter) mixer topology

- Doubly balanced
- MOS, BJT and BiCMOS
- IF linear input amplifier + mixing quad
- IF signal applied to bottom pair
- LO signal applied to mixing quad
- RF BPF (tuned) output at top
- Image rejection must be placed after mixing quad or built into the topology

Mixer Figure of Merit

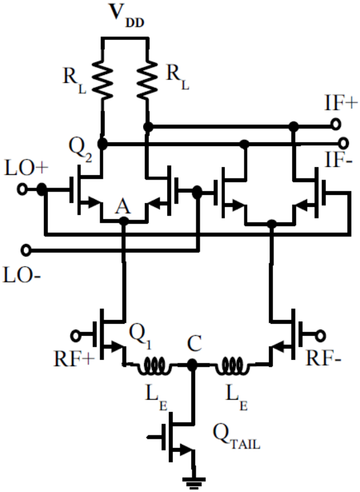
- In the downconversion mixers, maximize the linearity (IIP_3 or IIP_2), increase the conversion gain and decrease the NF and power dissipation

$$FoM_{downconverter} = \frac{IIP_3 G_c IS_{LO-RF} f}{(F_{SSB} - 1) P_{DC} P_{LO}}$$

- For an upconverter, maximize the linearity (OP_{1dB}), increase the conversion gain and decrease the power dissipation

$$FoM_{upconverter} = \frac{G_c OP_{1dB} IS_{LO-RF} f^2}{P_{DC} P_{LO}}$$

Gilbert Mixer with Degeneration



Design Methodology for Downconverters (1)

- **Step 1:** If the mixer has conversion gain, set the DC voltage drop V_{RL} on the IF load resistors R_L (if present) and the V_{DS} of the mixing quad transistors to satisfy the desired peak-to-peak output linear voltage swing V_{OMAX}

$$V_{RL} = \frac{V_{OMAX}}{2} = V_{DS} - V_{DS,SAT} = \frac{I_{TAIL} R_L}{2}$$

- **Step 2:** Set the bias current density of the transistors in the transconductor pair to J_{OPT}. Following condition must be satisfied:

$$W_1 = \frac{I_{D1}}{J_{OPT}} = \frac{I_{TAIL}}{2J_{OPT}}$$

Design Methodology for Downconverters (2)

- **Step 3:** Set the bias current density of the mixing quad transistors for maximum switching speed $Jpf_T/2$ for MOSFETs. Following condition must be satisfied:

$$W_2 = \frac{I_{TAIL}/4}{J_{pf_T}/2} = \frac{I_{TAIL}}{2J_{pf_T}}$$

- This step fixes the size ratio of the transconductor W_1 and mixing quad transistors (W_2) to

$$\frac{W_2}{W_1} = \frac{J_{OPT}}{J_{pf_T}} \approx 0.5$$

for MOSFETs

Design Methodology for Downconverters (3)

- **Step 4:** Size (i.e. find W_1) the transistors in the RF transconductor for the desired R_{SOPT} as the desired RF frequency f_{RF}. The source impedance is the LNA output impedance. For a differential mixer

$$R_{out}|_{LNA} = R_{SOPT}|_{mixer} \approx \frac{2f_{Teff}}{f \cdot g'_{meff} W_1} \sqrt{\frac{g'_m(R'_s + W_f R'_g(W_f))}{k_1}}$$

where f_{Teff} and g'_{meff} are for the cascode stage of the transconductor, when the bottom transistors is biased at J_{OPT}

Design Methodology for Downconverters (4)

- At this stage, the sizes of all transistors in the transconductor and the mixing quad, and the tail current source are fixed

$$W_1 = N_{f1} \cdot W_f = \frac{2f_{Teff}}{f_{RF} \cdot g'_{meff} R_{out}|_{LNA}} \sqrt{\frac{g'_m(R'_s + W_f R'_g(W_f))}{k_1}}$$

Design Methodology for Downconverters (5)

- **Step 5:** Add inductive source degeneration L_S to satisfy the linearity target (more important than noise and conversion gain). If the mixer is designed for noise matching, the linearity is given by

$$IIP_2 \propto \frac{f_{RF} g_m R_{out}|_{LNA}}{f_{Teff}}$$

$$L_S = \frac{R_{out}|_{LNA}}{2\pi f_{Teff}}$$

- **Step 6:** Add inductor L_G in series with the gate of M_1 to tune out the imaginary part of the input impedance.
- **Step 7:** The LO swing must be large enough to fully switch the mixing quad, yet not too large to cause the transistors in the quad to exit the active region.
  - Typical swing is $400 - 500mV_{pp}$ per side in 65nm and 90nm CMOS mixing quads.

Design Methodology for Upconverters (1)

- **Step 1:** If the mixer has conversion gain, set the swing on the resonant load resistors R_P (which includes the transistor r_o) at the RF output and the V_{DS} of the mixing quad transistors to satisfy the peak-to-peak linear output voltage condition

$$V_{OMAX} = 2(V_{DS} - V_{DS,SAT}) = I_{TAIL} \cdot R_P \qquad (1)$$

- I_{TAIL} is set by the power budget $(V_{DD} \cdot I_{TAIL})$ allocated to the upconverter but can be decoupled from the output swing and gain condition.
- When designing for the minimum power consumption, the smallest possible I_{TAIL} results from Eq. 1 with V_{OMAX} given as a design specification and the maximum realizable R_P ar f_{RF} being a technology constant.

Design Methodology for Upconverters (2)

- **Step 2:** Set the bias current density of the transistors in the transconductor pair to J_{pf_T}. This fixes transistor size to

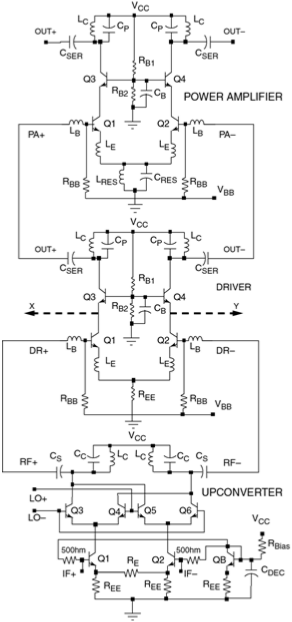
$$W_1 = \frac{I_{TAIL} R_L}{2J_{pf_T}}$$

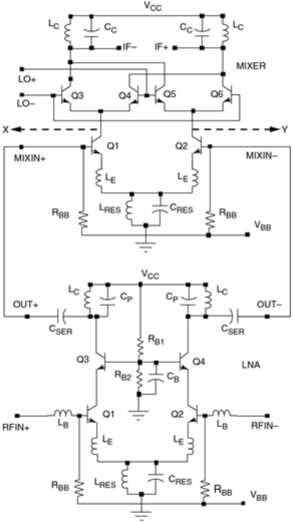
- **Step 3:** Set the bias current density of the mixing quad transistors for maximum switching speed $Jpf_T/2$ for MOSFETs. The quad transistor size becomes

$$W_2 = \frac{I_{TAIL} R_L}{2J_{pf_T}} = W_1$$

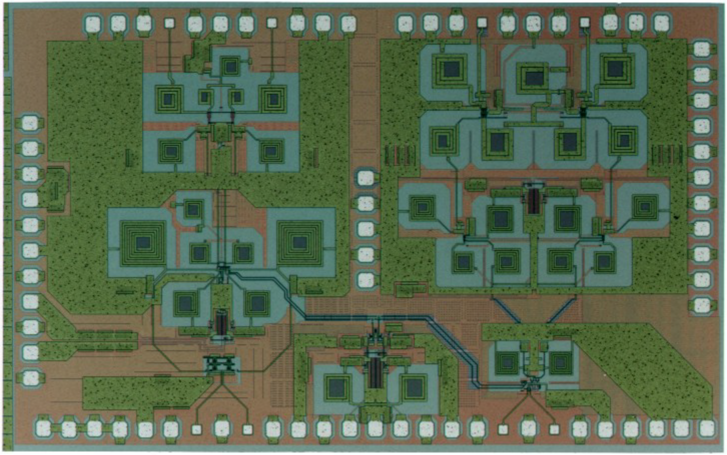
- **Step 4:** Add resistive source degeneration R_S to meet linearity target $IIP_3 \propto R_S \cdot I_{TAIL}$

Example: 5GHz Up/Downconverter Mixers

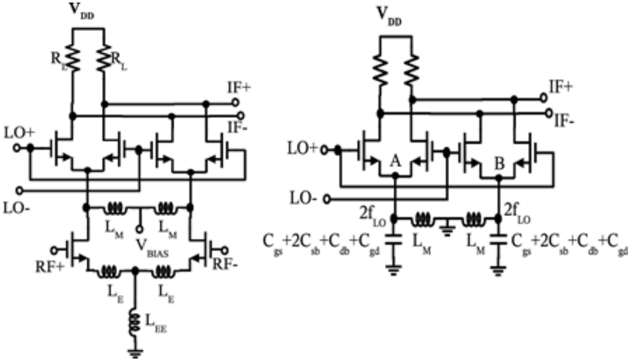




Example: 5GHz Up/Downconverter Mixers



Gilbert Mixer with Inductive Broadbanding

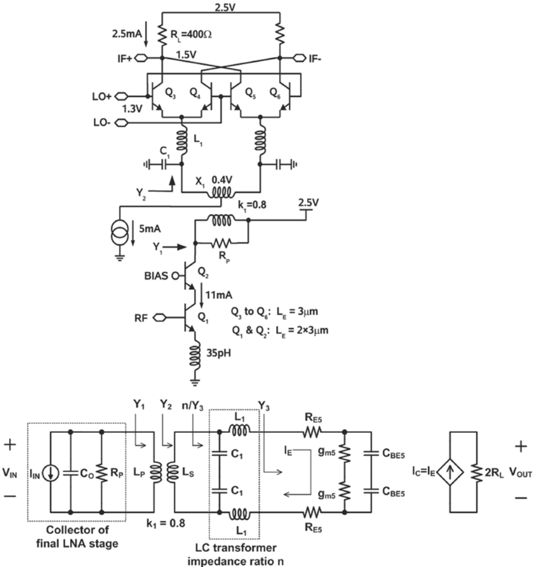


Low Voltage Mixer Topologies (1)

- Despite of many advantages, conventional Gilbert mixer has shortcomings.
  - Vertical stacking of at least two high-frequency path transistors between supply and ground.
  - Makes operation challenging with/below 1.2V CMOS.
- Over the years, several topologies have been proposed.
  - Idea is to have only one high-frequency transistors between supply and ground (along with the load).

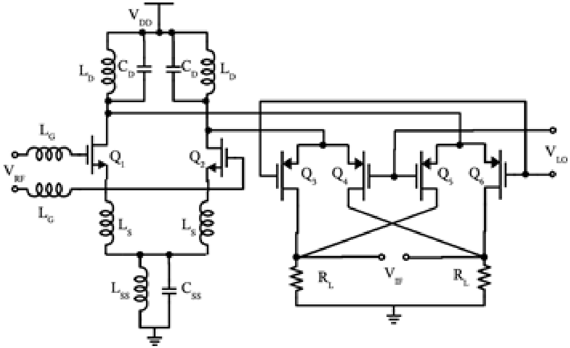
Low Voltage Mixer Topologies (2)

- Gilbert cell mixing quad with transformer coupling of RF signals.



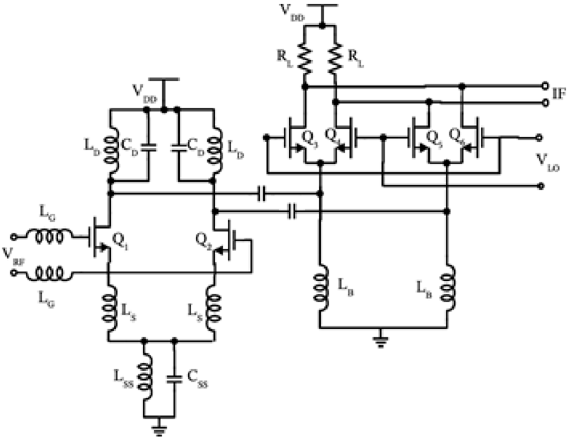
Low Voltage Mixer Topologies (3)

- Folded Gilbert cell with PMOS as the switching quad.



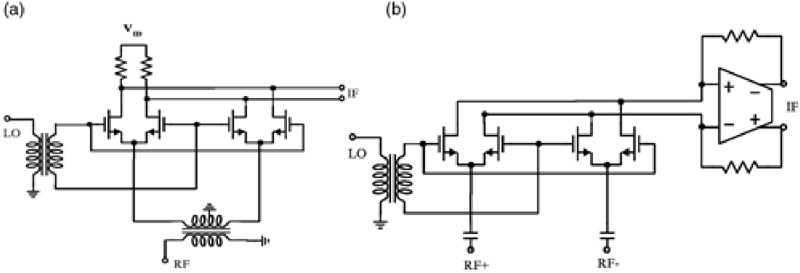
Low Voltage Mixer Topologies (4)

- Folded Gilbert cell with NMOS as the switching quad.



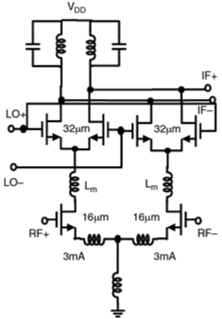
Low Voltage Mixer Topologies (4)

- Passive FET mixer where mixing quad consists of zero-biased FET switches which don't consume DC power.
  - Has high IIP3 but suffers from high-conversion loss, high LO power and high NF.
  - Transformer and/or AC coupling of RF and IF signals.
  - LO and RF ports can be interchanged.



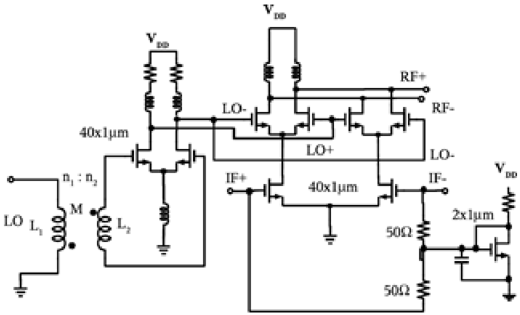
Example: 60GHz Downconverter in 90nm CMOS

- Gilbert mixer topology with 1.2V supply; tight headroom.
- Common-mode resistor replaced by a 70pH inductor to relax headroom; 140pH broadbanding inductors to increase gain and NF.
- Transconductor biased at $J = 0.18\frac{mA}{\mu m}$.
- Output is a low-Q resonant tank; BW of 3.5-5GHz.
- Downconversion gain is 2-3dB.



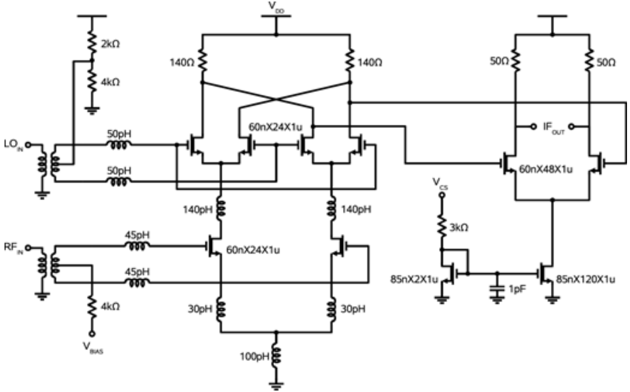
Example: 60GHz Upconverter in 90nm CMOS

- Using topology similar to the previous example.
- Large output power and linearity are the main concern.
- All transistors biased at $J = 0.3\frac{mA}{\mu m}$ with $W = 40\mu m$.
- IF input is broadband from DC to 6GHz and driven directly from off-chip 50Ω resistors.
- Upconversion gain is -6dB.
- Inductive broadbanding is not employed since its efficacy is in the IF path.



70-100GHz Downconversion (DN) Mixer in 65nm CMOS

- The DN example shown two slides earlier was scaled from 60GHz to 90GHz and ported to 65nm and 45nm CMOS.
  - Entire mmWave circuits are salable across frequency and technology nodes.
- $J = 0.18 \frac{mA}{\mu m}$. Measured DN gain was 4dB with NF=8dB.
- Mixer is noise-impedance matched through a 1:1 xfmr to the LNA output impedance of $75 O\Omega$.



140GHz Transformer-coupled DN Mixer in 65nm CMOS

- Inductive degeneration is implemented with 21pH inductors and 100pH in the common-mode on the RF path.
- Xfmrs with 1:1 turn ratio placed at the RF and LO ports for single-ended to differential conversion, and between G_m and mixing quad.
- Both G_m and mixing quad pair draw 6mA. G_m pair is biased at $J = 0.18\frac{mA}{\mu m}$ for lowest NF.

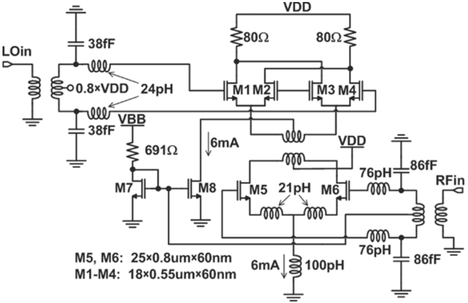
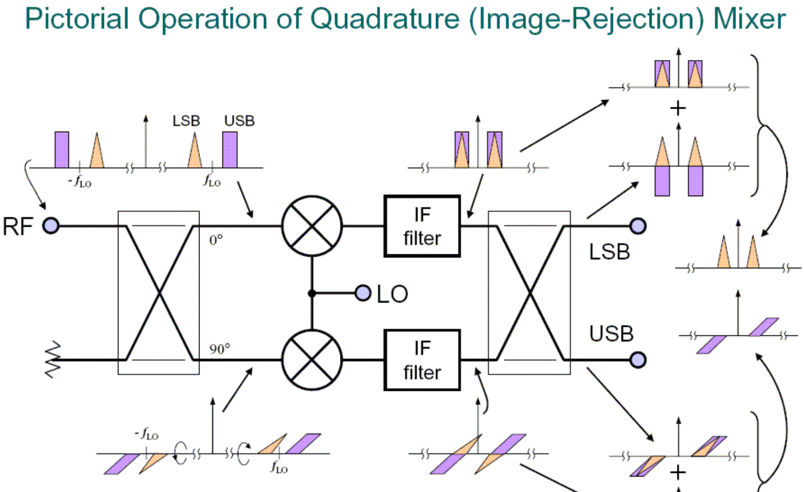


Image-Reject and SSB Mixer Topologies (1)

- Mixer rejects IM signal without the need for image-reject filter.
- Need two 90° hybrid couplers and an in-phase power splitter or adder (combiner).
- Three possible topologies depending upon which mixer port the 90° hybrids are placed.
- Topology suitable for image-reject downconverters is shown on the next slide.

Image-Reject and SSB Mixer Topologies (2)



Rules:

1. Mixers translate frequency but preserve phase.
2. Quadrature couplers do not shift phase on pass arm (i.e., 0° arm), but give 90° phase shift through cross arm (i.e., 90° arm).

Image-Reject and SSB Mixer Topologies (3)

- The first 90° hybrid splits the phase of the incoming RF signal and mixes it with the LO.
- The two IF outputs are then low-pass filtered and combined by the second 90° hybrid coupler.
- Provides lower sideband (LSB) and the upper sideband (USB) signals at separate ports.

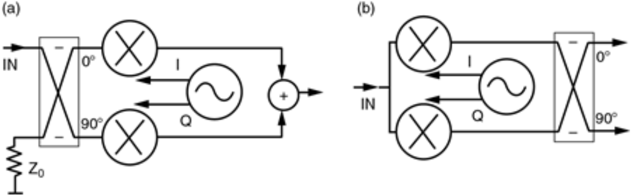
$$v_{LSB} = \frac{A_C V_{LO} V_L}{2} cost(\omega_{IF} t)$$

$$v_{USB} = \frac{-A_C V_{LO} V_U}{2} sin(\omega_{IF} t)$$

- See notations and derivations in the textbook.

mmWave Image-Reject Mixer Topologies

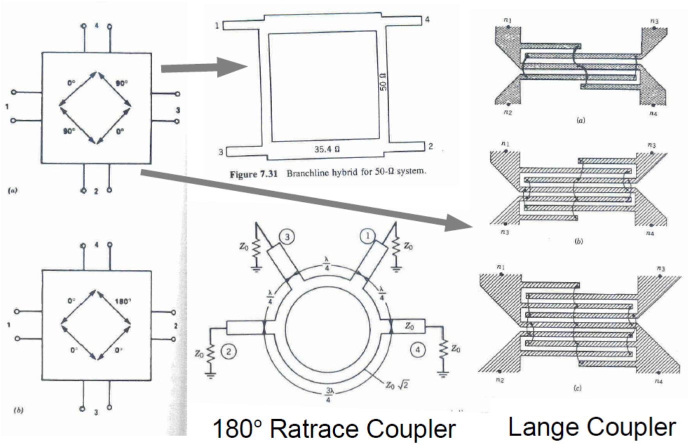
- Two other image-reject and SSB mixers are possible, if a quadrature VCO is employed instead of the second hybrid.



(a) Single-side band modulator, and (b) image-reject mixer topologies based on quadrature VCOs.

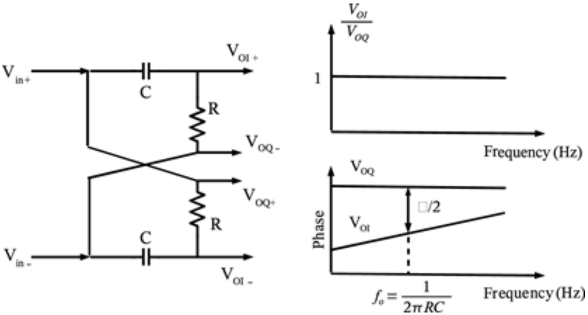
Broadband 90° and 180° Hybrid Couplers

- Need 90° and 180° hybrid couplers.
  - 90° coupler: Lange or branchline
  - 180° coupler: ratrace (Marchand) balun
  - In-phase Wilkinson splitter.



Lumped 90° RC Phase Shifter

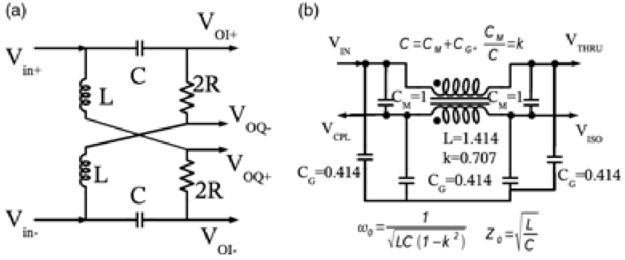
- 90° RC phase shifter, also called polyphase shifter.
  - Constant phase difference *vs* frequency or constant amplitude *vs* frequency possible, but not with both.
  - To increase bandwidth, several cascaded filter sections with staggered center frequencies are typically employed.



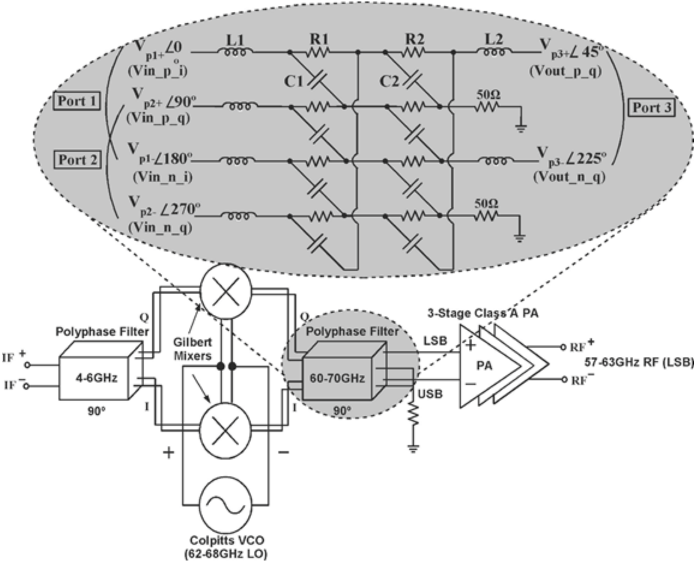
LRC Polyphase Filter and Lumped 90° Hybrid Coupler

- Improved quadrature all-pass filter employs inductors to extend the bandwdith over which the 90° phase shift is maintained with little amplitude imbalance.
- The transfer function is described by

$$\begin{bmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{bmatrix} = \begin{bmatrix} \frac{\pm s^2 + 2\frac{\omega_0}{Q}s - \omega_0^2}{s^2 + 2\frac{\omega_0}{Q}s + \omega_0^2} \\ \frac{\mp s^2 - 2\frac{\omega_0}{Q}s - \omega_0^2}{s^2 + 2\frac{\omega_0}{Q}s + \omega_0^2} \end{bmatrix}$$



60-70GHz Two-Stage LRC Polyphase Filter in a SSB WLAN SiGe TX



References

- S. Voinigescu, "High-Frequency Integrated Circuits," The Cambridge RF and Microwave Engineering Series, 1st ed., 2013.