LNA Design Methodology

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LNA Design

- Goal is to maximize LNA figure of merit:

$$FoM_{LNA} = \frac{G \cdot IIP_3 \cdot f_0}{(F-1) \cdot P}$$

- To minimize

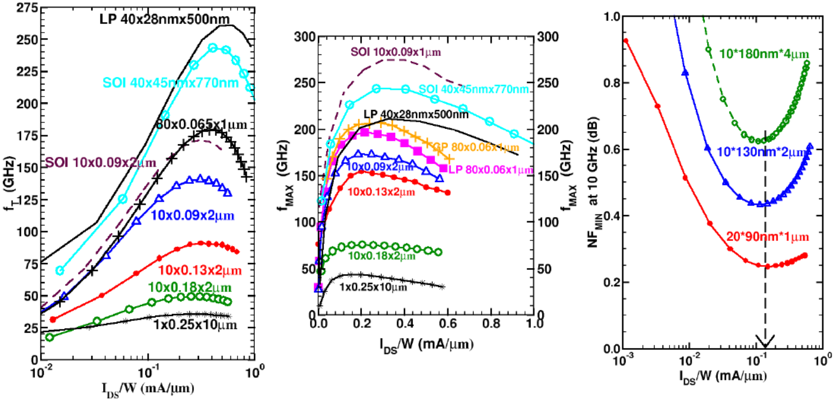
$$F = F_{min} + \frac{R_n}{G_S}|Y_S - Y_{SOPT}|$$

  we require noise match, i.e. $R_{SOPT} = \frac{1}{G_{SOPT}} = Z_0 = 50\Omega$
- To maximize power gain (G), we require input impedance match, i.e. $R_{in} = Z_0 = 50\Omega$, and also conjugate match at the output.
- The imaginary components of Z_{SOPT} and Z_{in} must be made equal to zero.

Design Philosophy

- Take advantage of what silicon does best: transistors.
- Use Si passives only sparingly:
  - Q is fairly low and undermines overall noise figure
  - Inductors are (significantly) larger than transistors, hence expensive.
- Make transistor sizing part of the noise matching step.
- Use only reactive (loss-less) feedback or minimize the noise contribution of resistive feedback components.
- Avoid active loads if at all possible.

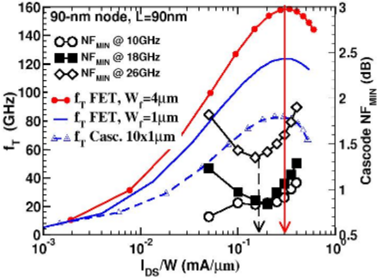
NMOS Characteristic Current Densities

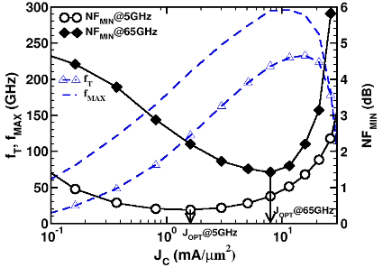


- J_{pfT} = where f_T reaches its max (NMOS$= 0.3 - 0.4\frac{mA}{\mu m}$)
- J_{pfMAX} = where f_{MAX} reaches its max (NMOS$= 0.2 - 0.3\frac{mA}{\mu m}$)
- J_{OPT} = where NF_{min} reaches its min (NMOS$= 0.15 - 0.2\frac{mA}{\mu m}$)

Biasing LNA Topology for Minimum Noise

- In CMOS, cascode $J_{OPT} = 0.15mA/\mu m$ irrespective of W_f, node, and frequency
- Lowest current for optimally biased MOS-LNA is 150mA for single $1\mu m$ finger





Active Device Matching

- Find optimal W_f for F_{min} at a given frequency
- We can set $R_{SOPT} = Z_0$ by optimizing transistor layout

$$R_{SOPT} = \frac{f_{Teff}}{f} \cdot \frac{1}{N_f W_f \cdot f \cdot g'_{meff}} \sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}}$$

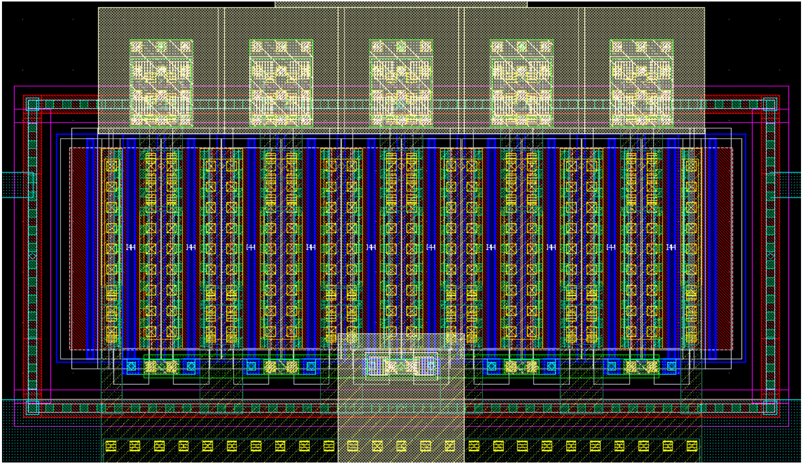
$$X_{SOPT} = j\frac{f_{Teff}}{f} \cdot \frac{1}{Z_0 N_f W_f \cdot f \cdot g'_{meff}}$$

- Thus, the mumber of fingers for a fixed $W_f = W_{OPT}$

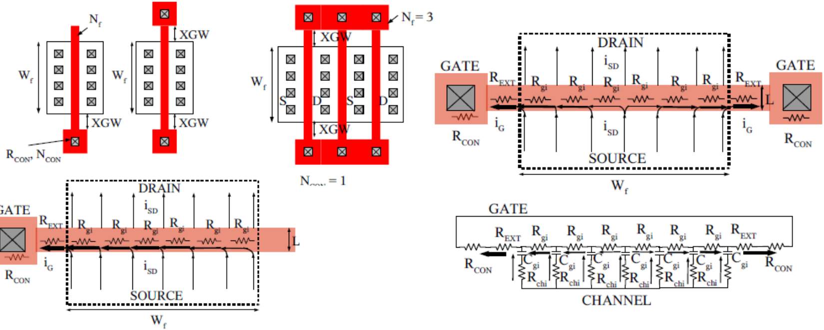
$$N_f = \frac{f_{Teff}}{f} \cdot \frac{1}{Z_0 W_f \cdot f \cdot g'_{meff}} \sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}}$$

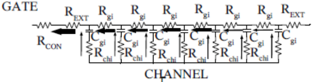
where $k_1 = 0.5 \ldots 1$, depending on the choice of W_f.

Typical MOSFET for High-Frequency Applications



Gate Resistance Calculations





$$R_g = \frac{\left[\frac{R_{CON}}{N_{CON}} + \frac{RSHG}{L}\left(XGW + \frac{W_f}{6}\right)\right]}{2\,N_f}$$

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Gate Resistance Calculations

- Gate fingers are contacted on one side, the expression for gate resistance is

$$R_g = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{SHG}}{L}(W_{ext} + \frac{W_f}{3})}{N_f}$$

- Gate fingers are contacted on both sides, the expression for gate resistance becomes

$$R_g = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{SHG}}{L}(W_{ext} + \frac{W_f}{6})}{2N_f}$$

  - where $W = N_f W_f$ is the total gate width, N_f is the number of fingers, L is physical gate length.
  - W_{ext} is the distance between the gate contact and active region.
  - R_{SHG} is the sheet resistance per sq. of the poly or metal gate, typically 10Ω in 90nm CMOS.
  - N_{CON} is the number of metal-to-gate vias per contact
  - R_{CON} is the metal-to-gate via resistance, typically $15 - 20\Omega$ in 90nm CMOS

Passive Device Matching

- For LNA stage with inductive degeneration (CS or cascode), a passive input match is obtained as

$$R_{in} = R_g + R_s + \omega_T L_S = Z_0$$

- This results in design equation $L_S = \frac{Z_0 - R_g - R_s}{\omega_T}$
- The imaginary parts of Z_{in} and Z_{SOPT} are within 20% of each other, which are tuned out by the series inductance $L_G \approx \frac{\omega_T}{\omega^2 g_{meff}} - L_S$
- An output match is provided using L-match (or other suitable matching network) to maximize power gain (G).

Design Methodology for CS and Cascode LNA

- **Step 1:** Set the V_{DS} of transistor for maximum linearity, such that clipping of output is avoided. In case of CS stage, use $V_{DS} = V_{DD}$
- **Step 2:** Determine the J_{OPT} of the amplifier. Maintain this current density throughout the rest of the design steps. This is equivalent to solving: $\frac{\partial F_{min}(J)}{\partial J} = 0$.
- **Step 3:** Select the best FET finger width that leads to the best NF_{min} without degrading f_{MAX}. In FinFETs, finger width is fixed by the process. This is equivalent to solving: $\frac{\partial F_{min}(W_f)}{\partial W_f} = 0$.
- **Step 4:** Size the transistor such that $Re\{Z_{SOPT}\} = Z_0$ which is equivalent to $\frac{\partial F_{Z_0}(N_f)}{\partial N_f} = 0$.
  This is carried out by connecting gate fingers in parallel.

Design Methodology for CS and Cascode LNA (2)

- At the end of Step 4, the bias current and size of all transistors in the LNA stages are known. All the transistors maust be laid out in Cadence and the layout parasitics should be extracted, before proceeding to the next step. Otherwise, the matching network will have to be redesigned after parasitic extraction.
- **Step 5:** Add the degeneration inductance L_S to set the real part of the input impedance to Z_0 without affecting Z_{SOPT}; $L_S = \frac{Z_0 - R_g - Rs}{2\pi f_T}$.
- **Step 6:** Add the gate inductance L_G such that the imaginary parts of Z_{in} and Z_{SOPT} become equal to zero.
- **Step 7:** Design the output matching network (L-match etc.) to maximize the power delivered to the load over the bandwidth of interest. An L-match using L_P and C_1 allows DC blocking for the next stage.
- **Step 8:** Add bias circuitry without degrading the noise figure.

Frequency Scaling of CMOS LNAs

The J_{OPT} of NMOSFET does not change with frequency, and in technology prior to 45nm CMOS, with technology node. Thus we can scale an existing LNA design in frequency from f_0 to $f_0^{'} = \alpha f_0$ using the steps:

- **Step 1:** Bias transistors for minimum noise at $J_{OPT} = 0.15 \frac{mA}{\mu m}$.
- **Step 2:** Device sizing: W_f remains unchanged but $N_f^{'} = \frac{N_f}{\alpha}$ and $W^{'} = \frac{W}{\alpha}$
- **Step 3:** Input impedance matching: L_S remains largely unchanged since f_T has not changed but the source and gate resistances are now larger because of overall smaller W

Frequency Scaling of CMOS LNAs (2)

$$L_S^{'} = \frac{Z_0 - \alpha(R_g + R_s)}{2\pi f_T} \approx L_S$$

$$L_G^{'} = \frac{1}{\alpha^2 \omega^2 \frac{C_{in}}{\alpha}} \approx \frac{L_G}{\alpha}$$

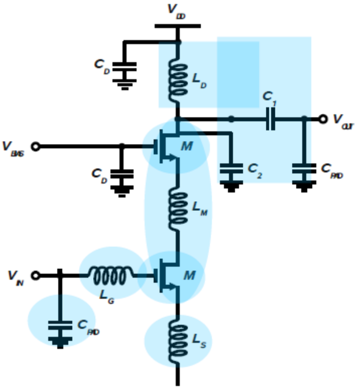
Step 4: Output matching: $L_D^{'} = \frac{L_D}{\alpha}$, $C_D^{'} = \frac{C_D}{\alpha}$.

Note that method only applies to CMOS LNAs, not HBT LNAs.

mmWave LNA Design (1)

- In CMOS, C_{gd} can be $\approx 50\%$ of C_{gs}, and the f_T of the cascode stage is at least 33% smaller than that of the transistor.
- Thus, CMOS cascode LNA stage requires bandwidth extension techniques in order to achieve acceptable gain at mmWave frequencies.
- One approach is to place a shunt inductor to the AC ground (no DC path) at the middle node between the CS and CG transistors.
  - However, this resonance is narrowband.

mmWave LNA Design (2)



mmWave LNA Design (3)

- Another technique is to form an artificial transmission line (TL) by introducing a series inductor between the CS and CG transistors.
  - An added benefit of this approach is that it improves NF of the cascode stage at mmWave.
- The characteristic impedance of this artificial transmission line is

$$Z_{01} = \sqrt{\frac{L_{M1}}{C_{gs2} + C_{sb2}}}$$

- The 3dB bandwdith when matched at both ends becomes

$$f_{3dB} = \frac{1}{\pi\sqrt{L_{M1}(C_{sb2} + C_{gs2})}}$$

mmWave LNA Design (4)

- The design of the MOS cascode with artificial interstage TL proceeds from the output of the cascode.
  - First, the impedance $Z_{M2,in}$ of the common-gate transistor M_2 is calculated based on its load resistance at resonance.
  - Next, the value of L_{M1} is chosen so that the impedance of the TL satisfies the condition

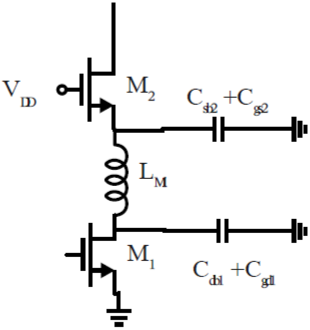
$$Z_{01} = Z_{M2,in} = \frac{1}{g_{m2} + \frac{\omega L_{D1} Q}{2(1+g_{m2} r_{o2})}}$$

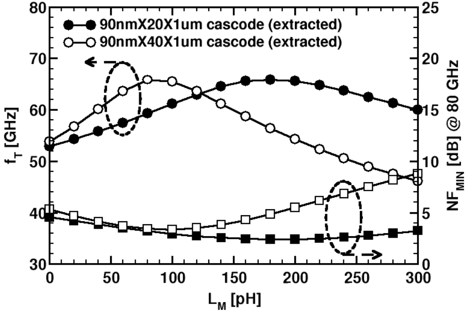
  - The $1/2$ factor in the second term originates from the assumption that the cascode stage of loaded with an impedance that is matches to L_{D1} at resonance.
  - In other words, the loaded Q of the inductor L_{D1} under matched conditions is at best 50% of the unloaded Q.

Design Methodology for mmWave LNAs (1)

- **Step 1:** Set the bias to optimum NF_{min} current density, J_{OPT} to minimize transistor NF.
- **Step 2:** Choose optical W_f to minimize NF_{min}.
- **Step 3:** Find the best L_M value for the cascode biased at J_{OPT} by plotting the f_T of the cascode versus L_M. Note that L_M scales with $W^{-1}(N_f^{-1})$, This step is best carried out by simulation.
- **Step 4:** With all devices biased at J_{OPT}, scale the number of fingers (N_f), and L_M to match the optimal noise impedance, R_{SOPT}, to the source impedance Z_0.

Design Methodology for mmWave LNAs (2)

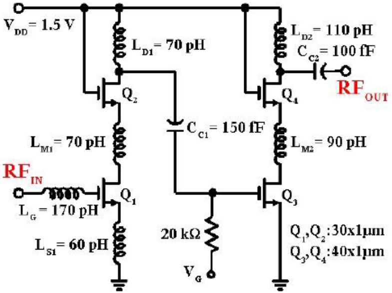


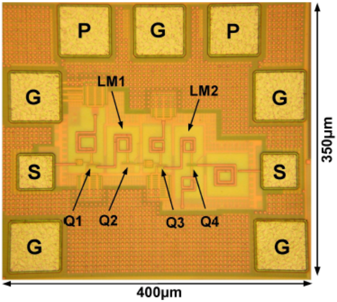


Design Methodology for mmWave LNAs (3)

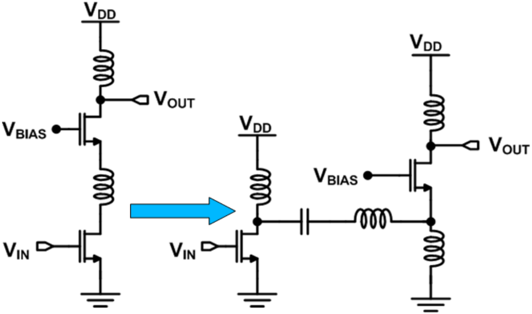
- **Step 5:** After layout and parasitic extraction, with f_T from Step 4, find $L_S = (Z_0 - R_s - R_g)/\omega_T$. Note that ω_T corresponds to the cascode stage with L_M, not just to the transistor, and after extraction of layout parasitics.
- **Step 6:** Add L_G to tune out $Im\{Z_{in}\}$ and $Im\{Z_{SOPT}\}$.
- **Step 7:** Add output matching network to maximize gain.

Example: 90-nm CMOS Cascode LNAs





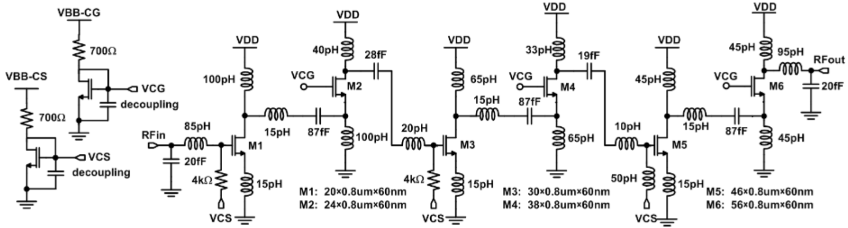
Single-Transistor Stack Topologies



- AC-coupled cascode, 1V operation in GP CMOS, insensitive to V_{THN}, yet:
  - 2X the DC current
  - 2nd resonant tank reduces bandwidth,
  - Extra lossy inductor and MIM cap =¿ higher loss, larger area

140GHz 65nm CMOS LNA

- 6-stage AC-coupled cascode amplifier
- 63mW at 1.2V
- 20% stage scaling
- $300\mu m \times 500\mu m$ including pads



Other LNA Concepts (Read in the Textbook)

- Power-constrained CMOS LNA design
- Low-current CMOS inverter LNAs
- Common-gate LNAs
- G_m-boosting and noise-canceling LNAs
- Transformer feedback LNAs
- Differential LNAs Design Methodology
- Impact of PVT variations on LNA design

References

- S. Voinigescu, "High-Frequency Integrated Circuits," The Cambridge RF and Microwave Engineering Series, 1st ed., 2013.