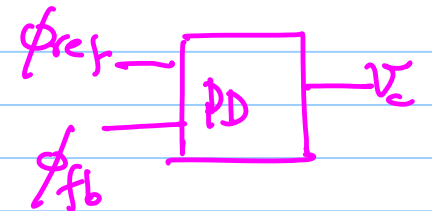
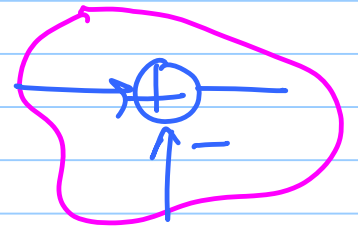


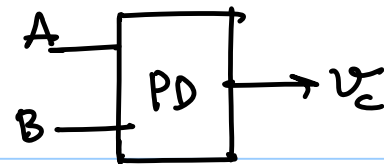
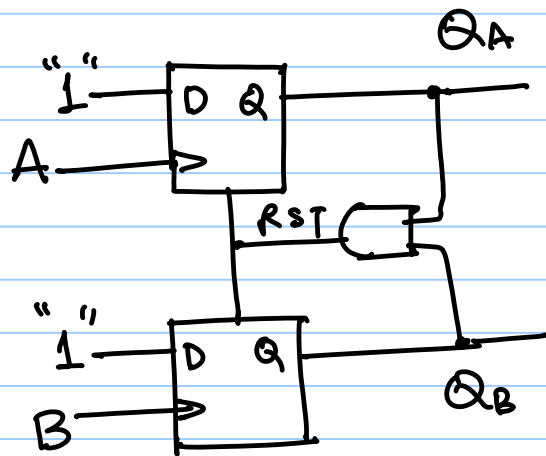
ECE 504 - Lecture 4

Note Title

8/31/2016

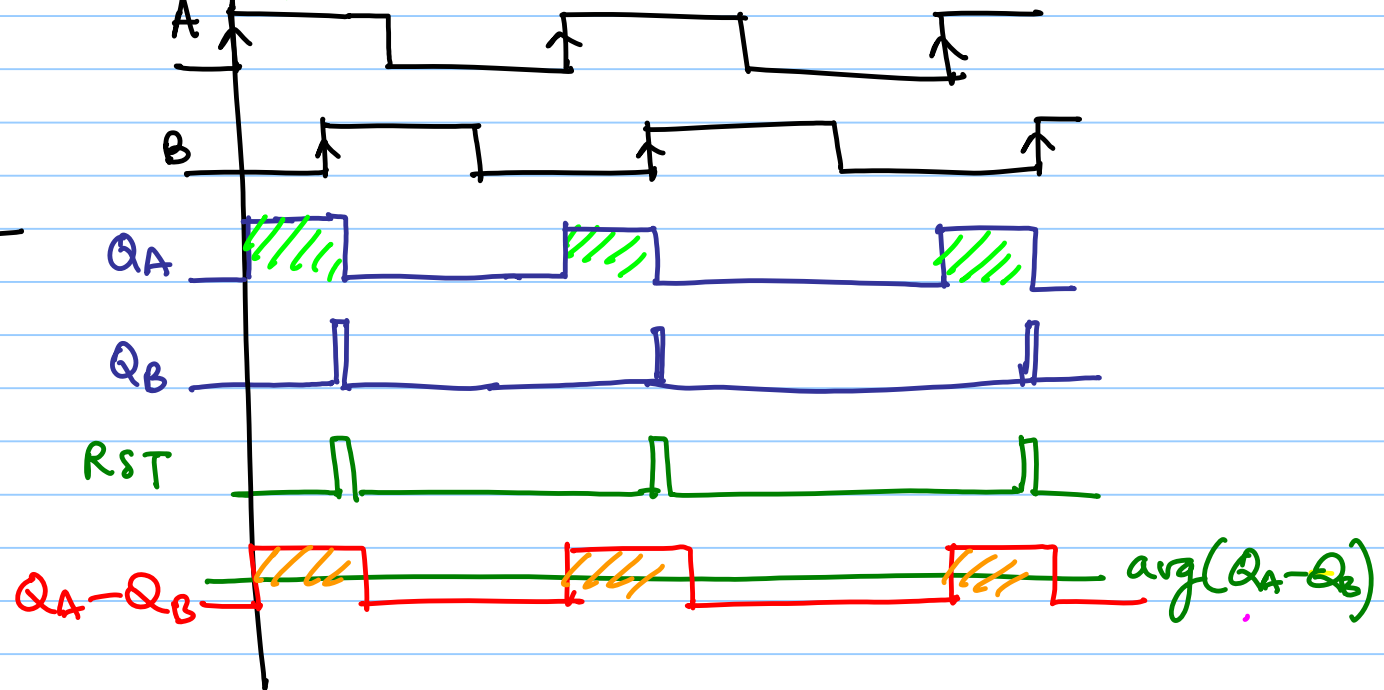


Phase Detector

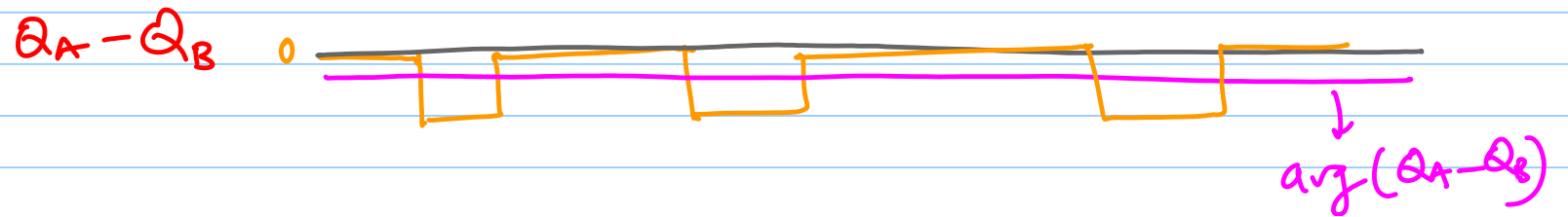
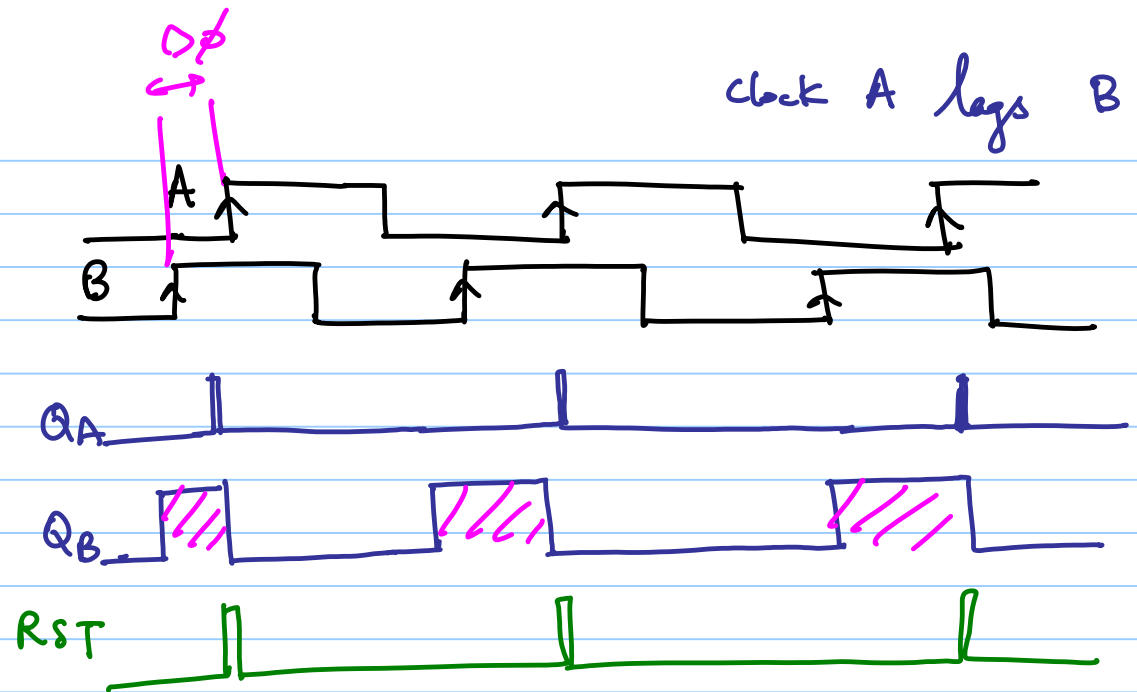


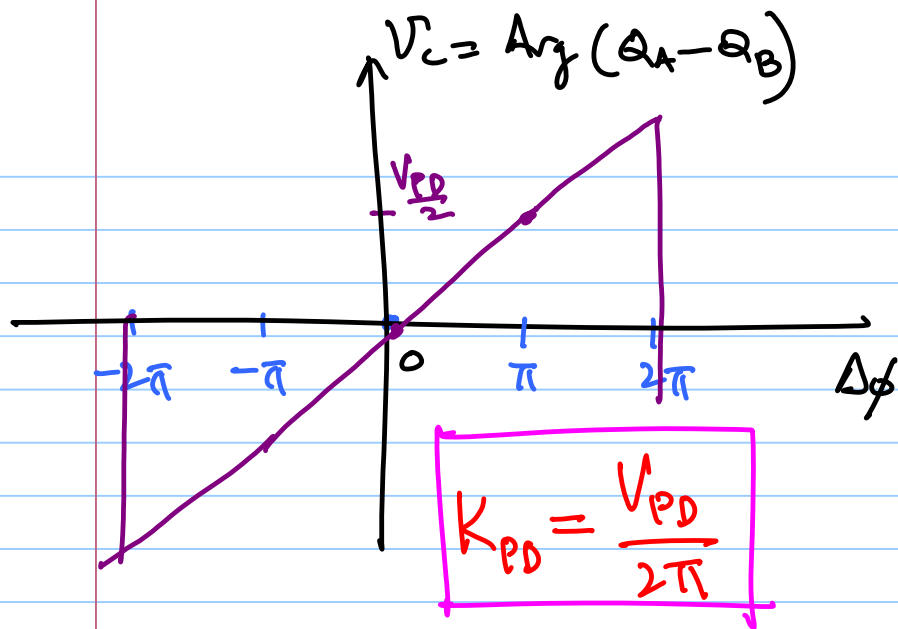
clock A leads B

$\Delta\phi$

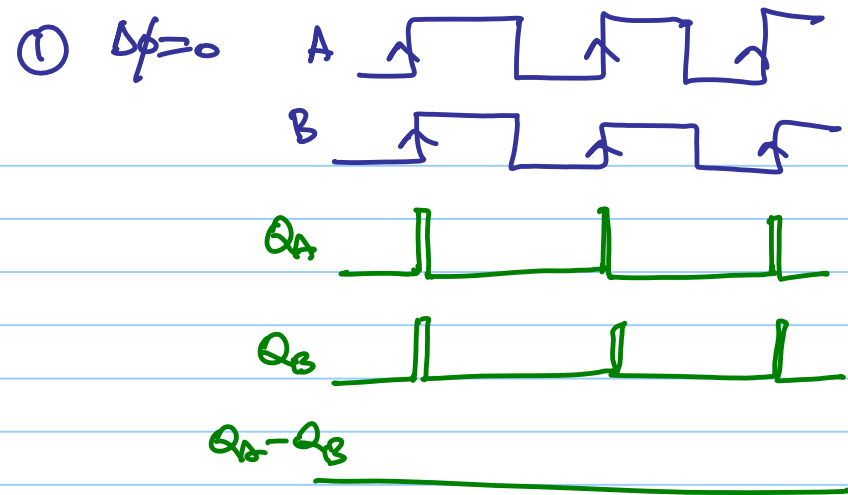


output is
 $\arg(Q_A - Q_B)$

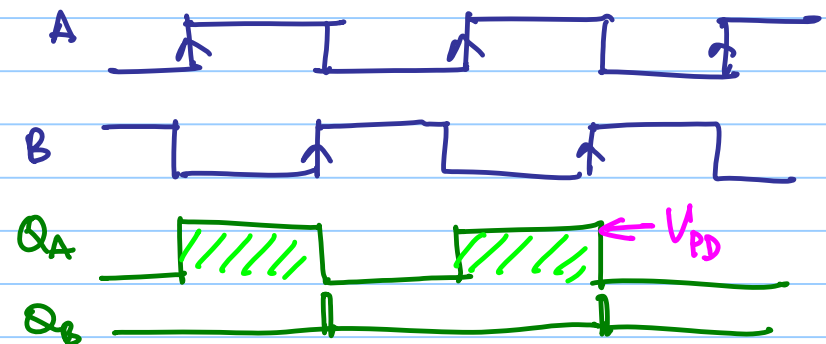


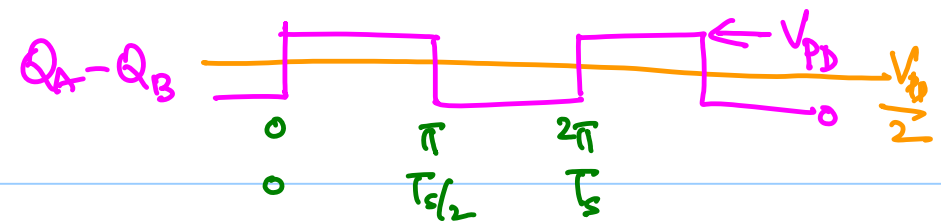


$V_{PD} \Rightarrow$ supply voltage or logic "1" for the FF

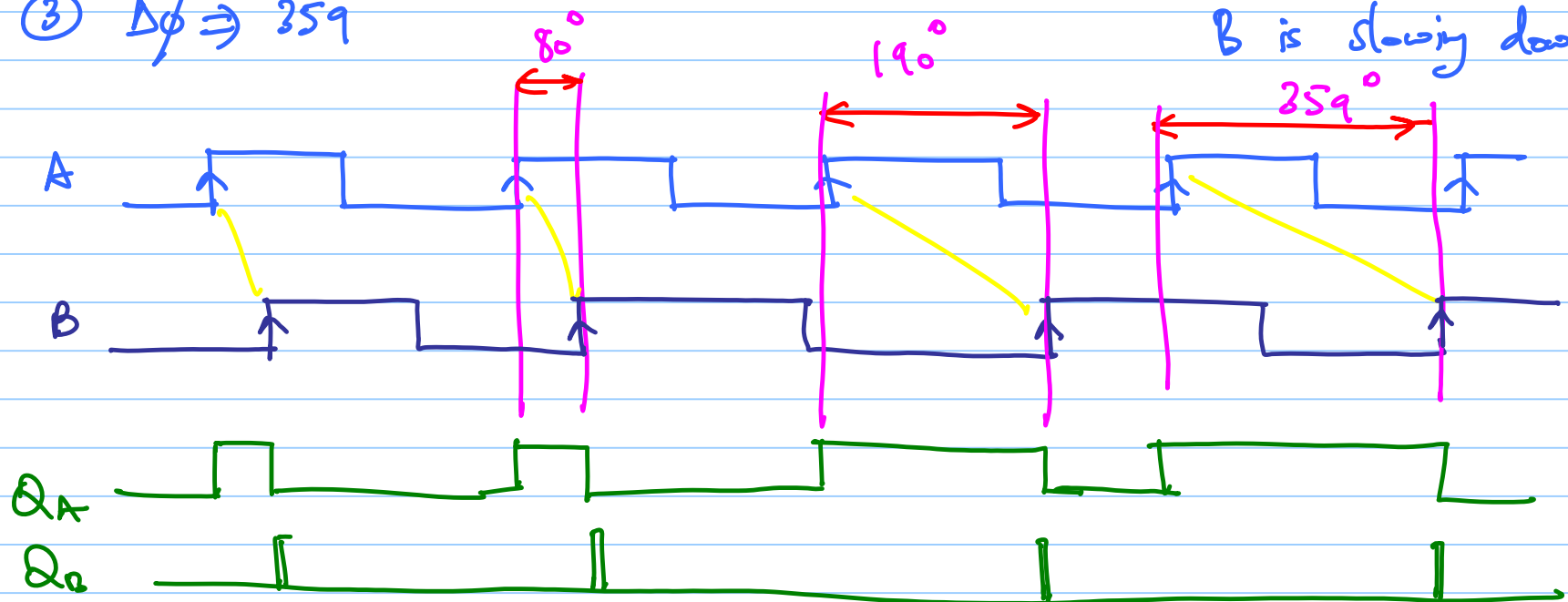


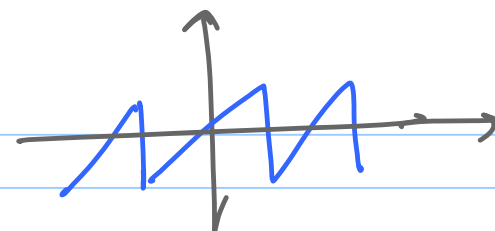
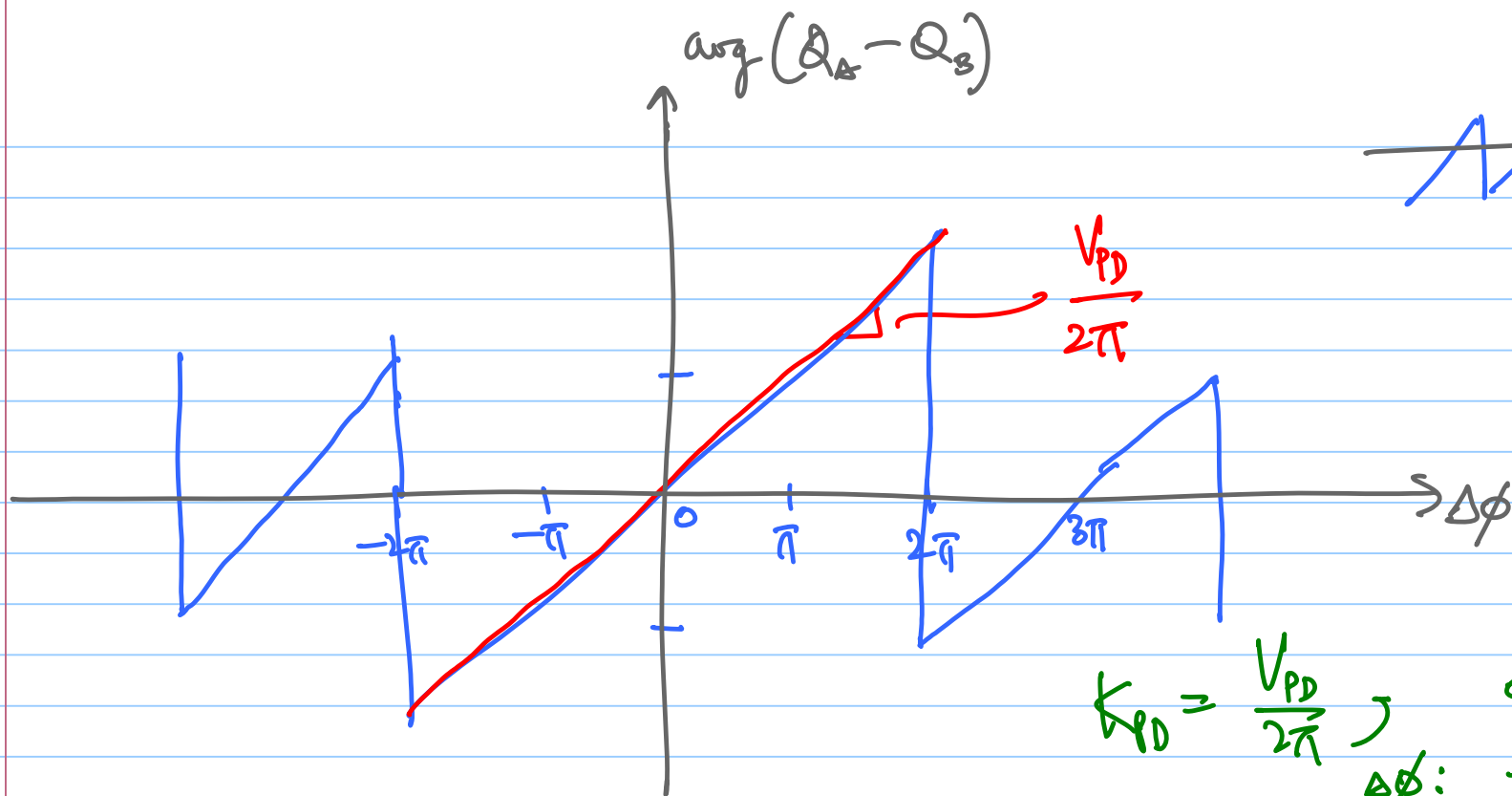
② $\Delta\phi = \pm\pi$



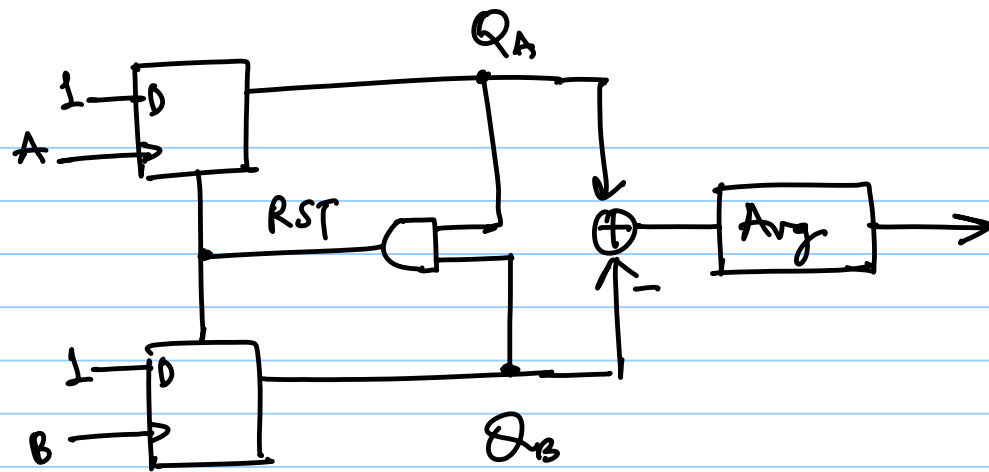


③ $\Delta\phi \Rightarrow 359^\circ$





$$K_{PD} = \frac{V_{PD}}{2\pi}, \quad \text{extended range } \Delta\phi: -2\pi \text{ to } 2\pi$$



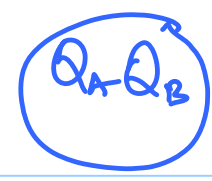
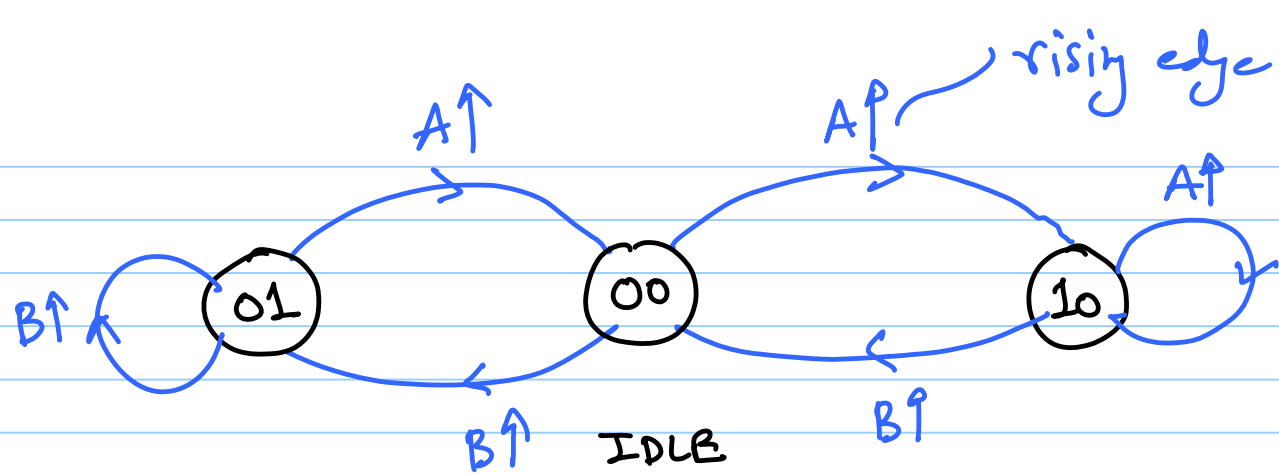
in radians

$$\frac{\Delta\phi}{2\pi} \cdot V_{PD}$$

$$K_{PD} = \frac{V_{PD}}{2\pi}$$

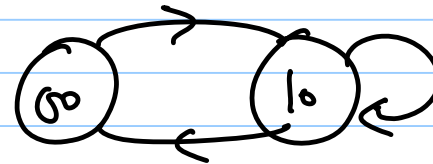
Two ffs [QA QB] state
 2-bit State
 Machine
 ↳ only 3 valid states

QA	QB	
0	0	✓
0	1	✓
1	0	✓
1	1	X



Tri-state Phase-frequency detector
(PFD)

let $f_A > f_B \Rightarrow$ more $A \uparrow$ than $B \uparrow$ transitions



$$\Rightarrow \text{avg}(\phi_A - \phi_B) > 0$$

$\Rightarrow V_C > 0 \Rightarrow V_{CO}$ will speed up
& B will catch up

for $f_A < f_B \Rightarrow$ opposite will happen

$\hookrightarrow$ always moves in the right direction to catch up
with the reference frequency

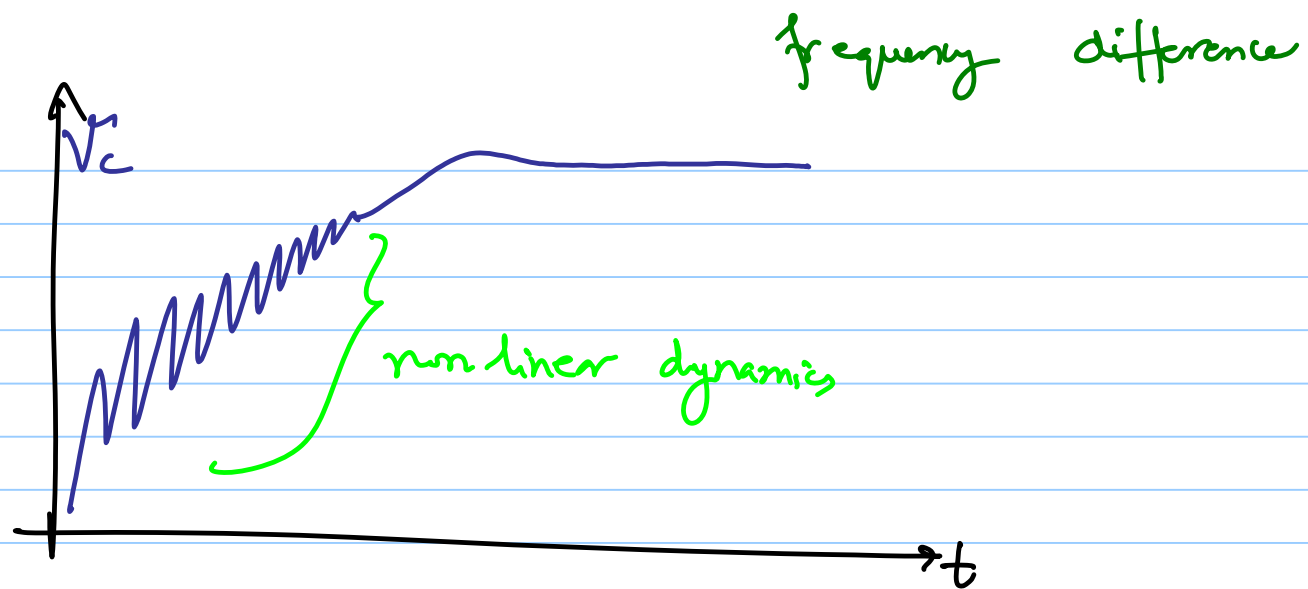
↳ This PFD also provides frequency difference detection.

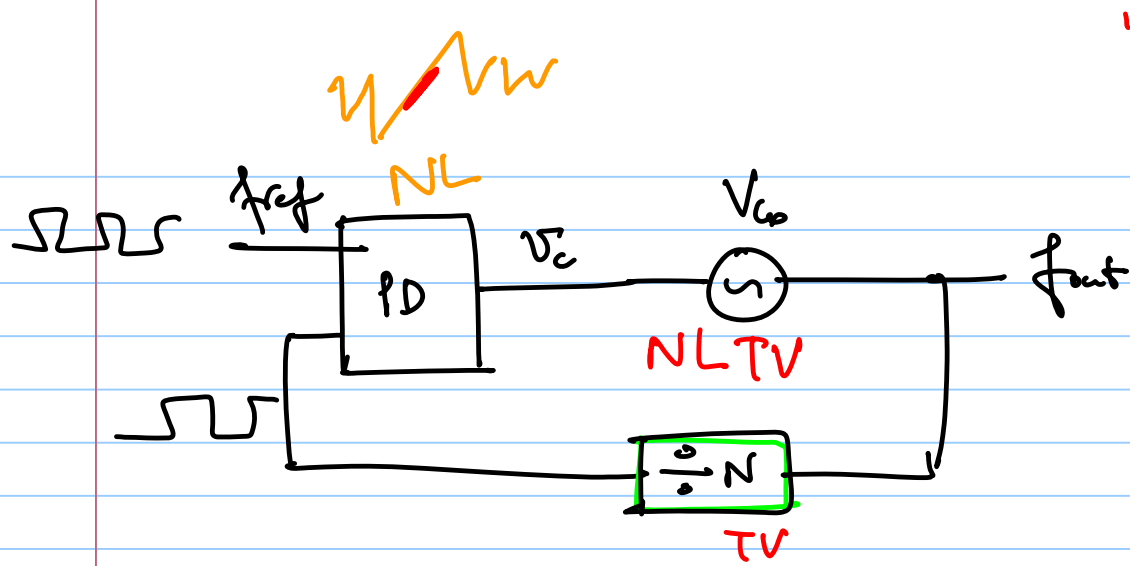
"Locking" → for what frequency range the PLL remains locked

"Capture" → apply some frequency and see if the PLL can lock

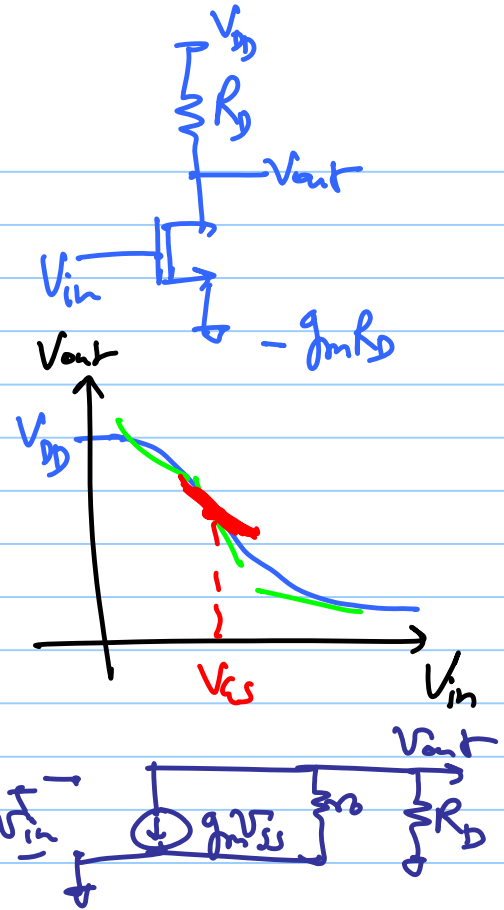
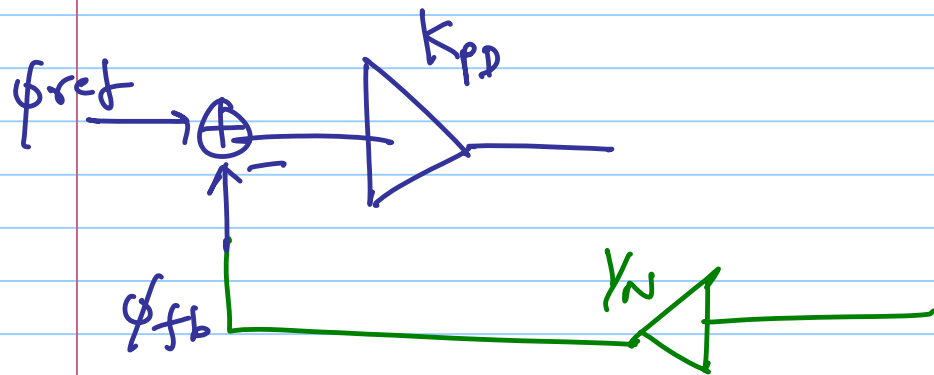
* PFD facilitates a faster capture

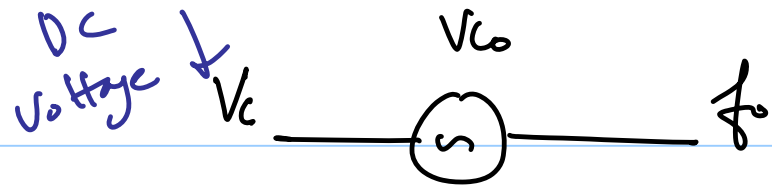
XOR PD $\Rightarrow$ the output avg is zero $\Rightarrow$ takes time to lock
when starting with large





"LTI"

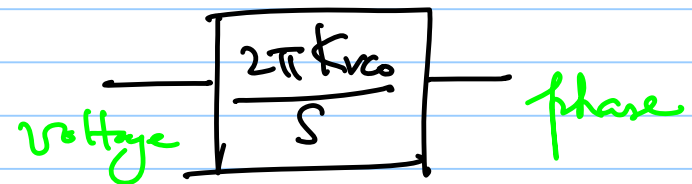
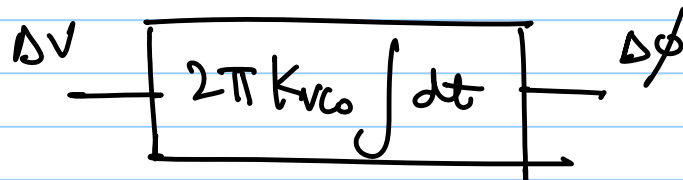




$$\cos(2\pi f_0 t + 2\pi K_{vco} \int V_c dt)$$



$$\cos(2\pi f_0 t + 2\pi K_{vco} \int V_c dt + \underbrace{2\pi K_{vco} \int \Delta V dt}_{\Delta\phi})$$



incremental phase-domain equivalent model

