ECE 504 - Lecture 28

Note Title 12/1/2016

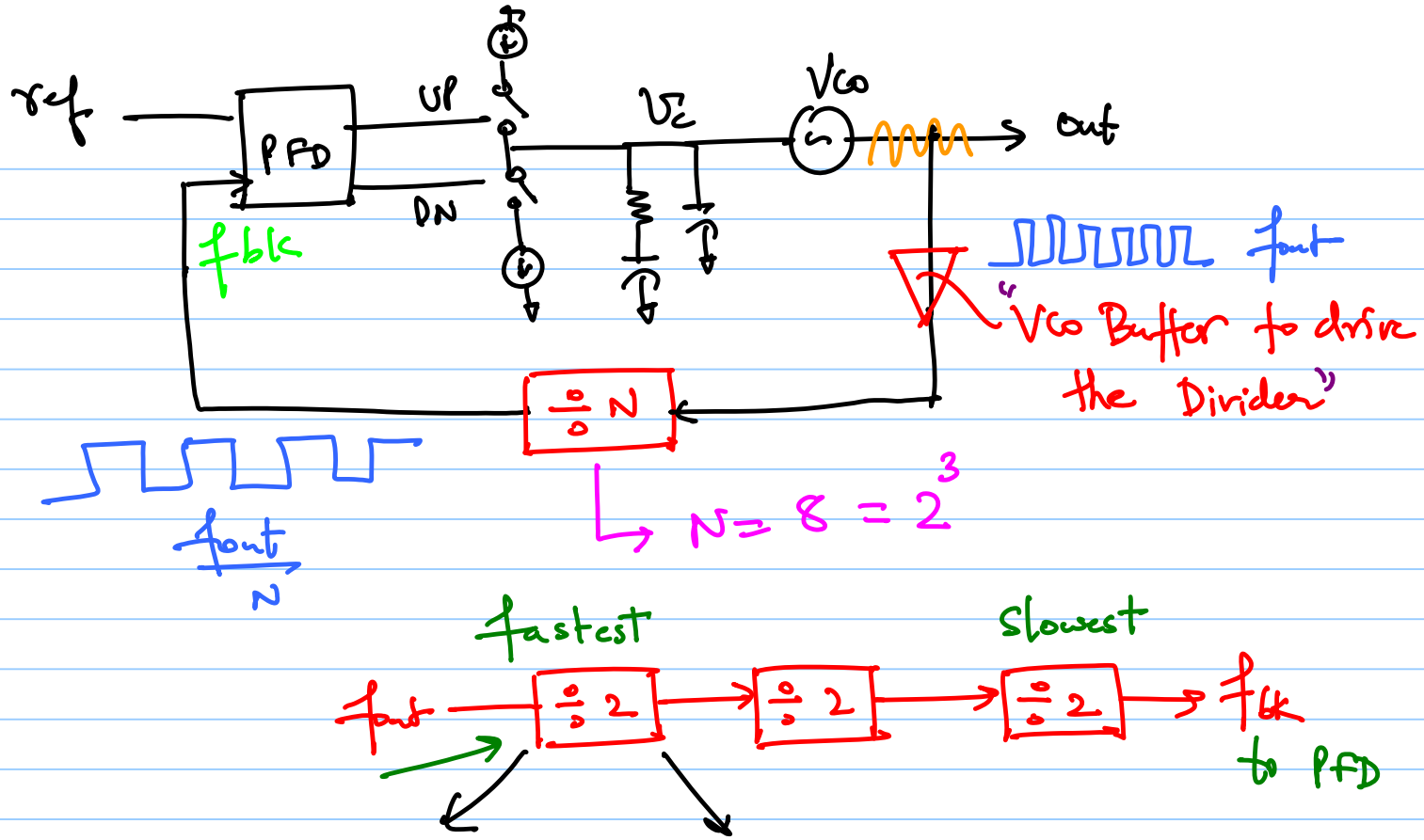
CDR → Dual Loop Architectures.

PLL → VCOs

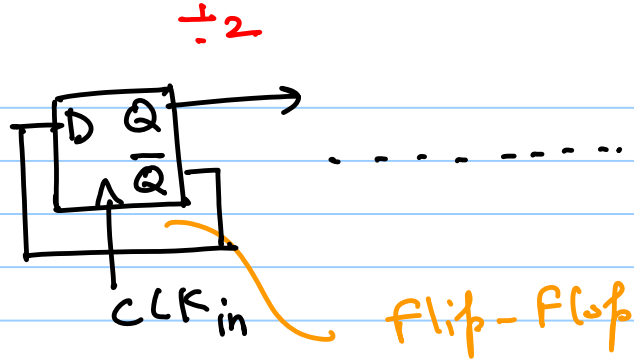
PFDs

Loop filters

"Divider"


ref
PFD
UP
DN
f_{blk}
V_c
VCO
out
f_{out}
"VCO Buffer to drive the Divider"
÷ N
f_{out}
N
N = 8 = 2^3
fastest
Slowest
f_{out}
÷ 2
÷ 2
÷ 2
f_{blk}
to PFD

M
2



flip-flop

→ CMOS flop-flop (Digital Course)

→ Dynamic flip-flops

→ CML → Current Mode Logic type Latch/ff design ← High-speed

If the PLL is single-ended output

↳ CLK_{out} and not $\overline{CLK_{out}}$

CLK, $\overline{CLK}$

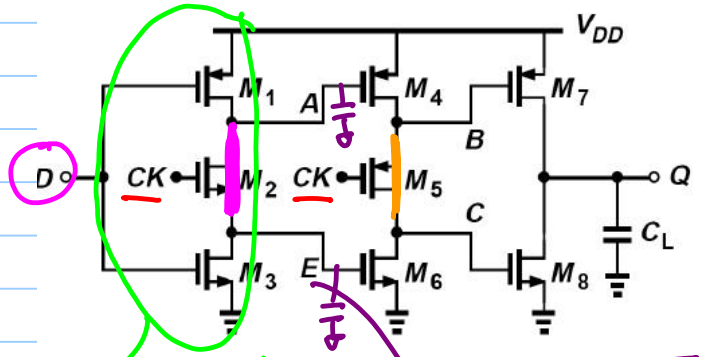
↳ Need to generate $\overline{CLK}$ if we want to implement CMOS static type FF.

↳ Complementary Phase are Reqd.

TSPC type Latch

↳ TSPC ⇒ True Single phase Clock.

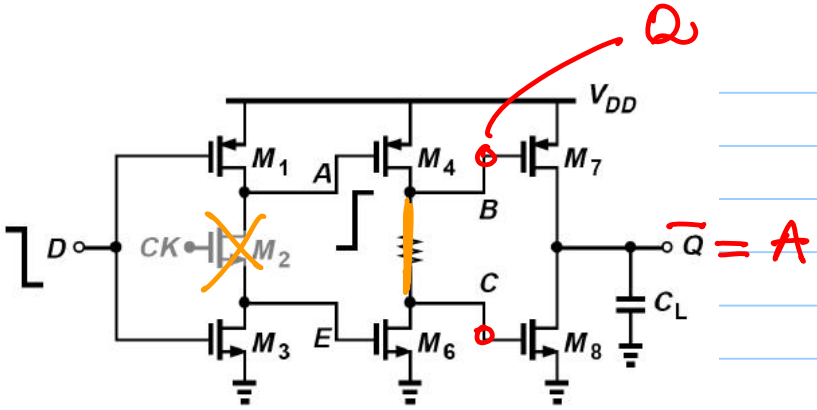
TSPC FF



CMOS Inverter

A & E = $\overline{D}$

CK = 1

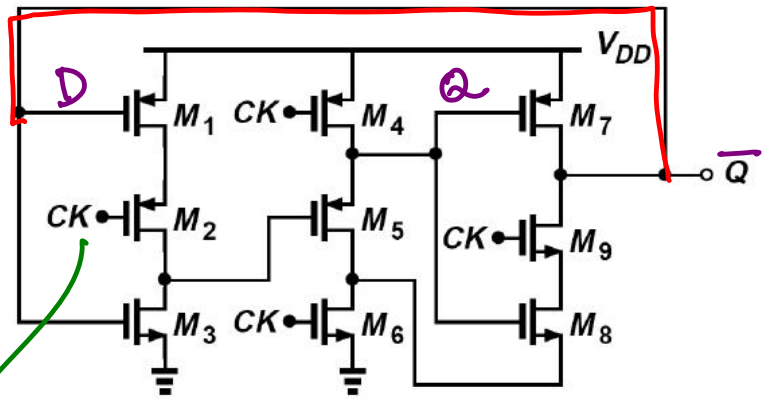


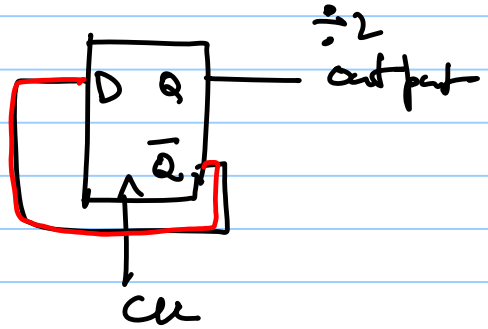
CK = 0

B & C = $\overline{A}$ or $\overline{E}$ = D

Dynamic FF

↳ States are dynamically stored on a Capacitor





Needs rail-2-rail clock swing.

÷2 Circuit

TSPC style logic

* Use TSIC Divider in the project

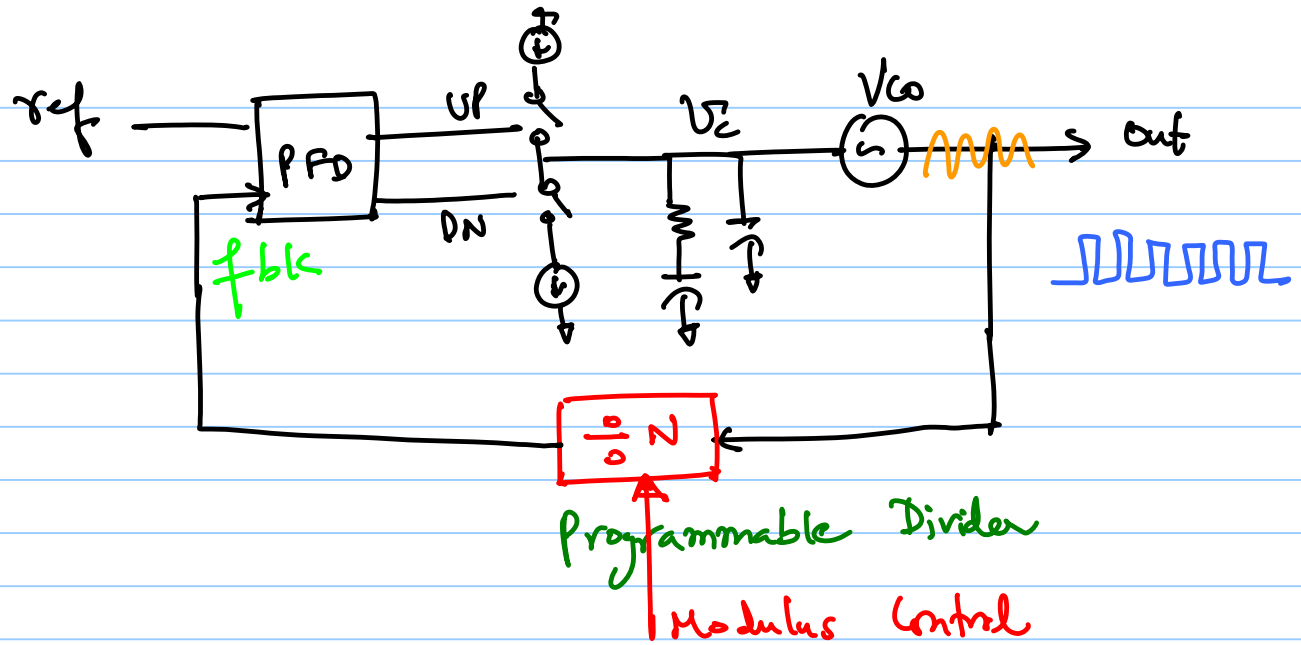
$N = 2^M$, "Modulus"

2, 4, 8, 16 . . . .

3, 51 ,

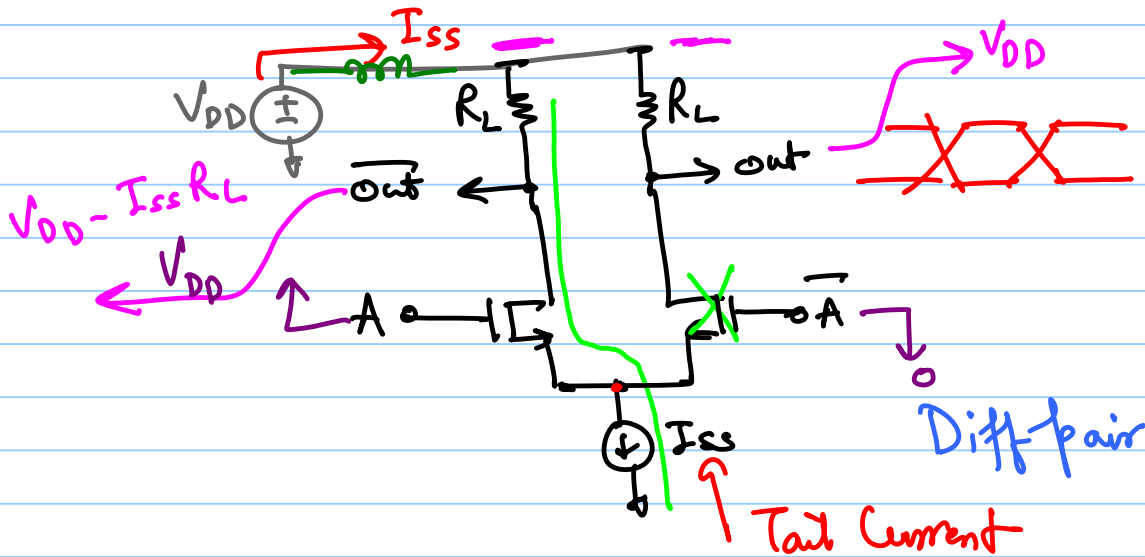
↳ "Integer Modulus"

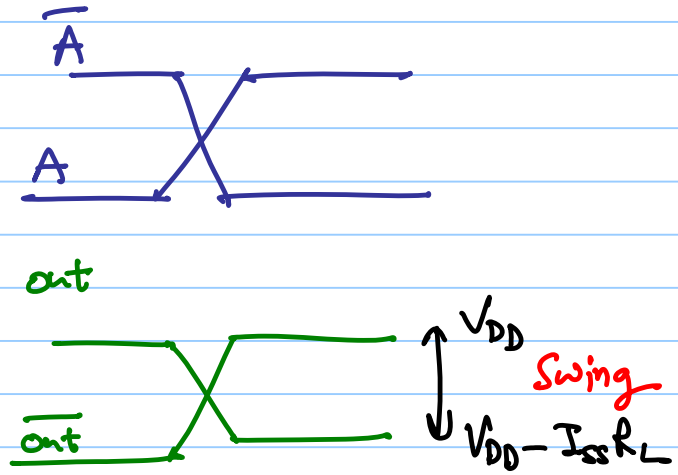
↳ fractional Divider Ratio


ref
PFD
UP
DN
fblk
Vc
Vco
out
÷ N
Programmable Divider
Modulus Control

CML type logic

↳ Current Mode Logic

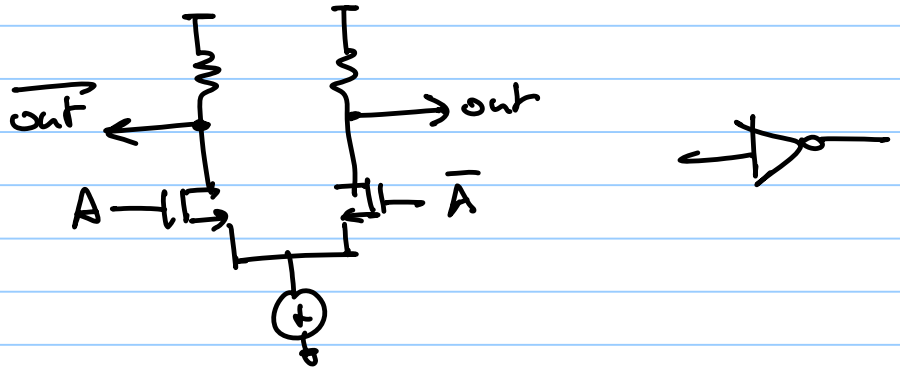




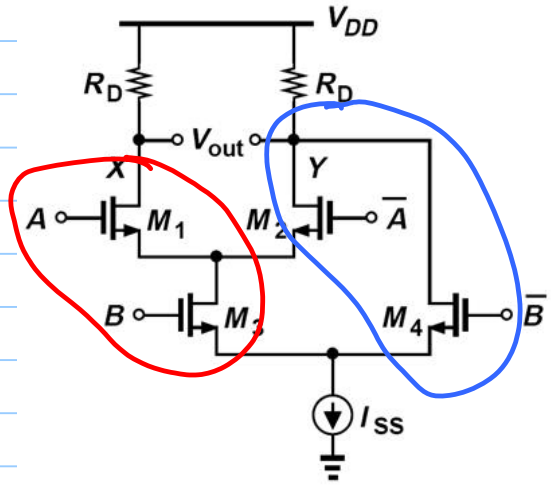
~ 300mV swing

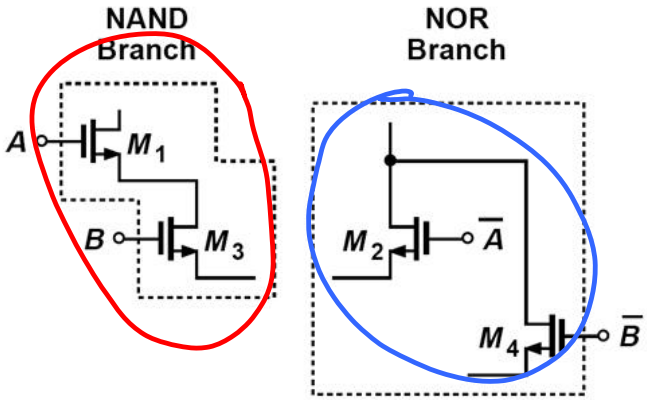
No V_{DD} contamination

↳ Allows us to design at very high speeds

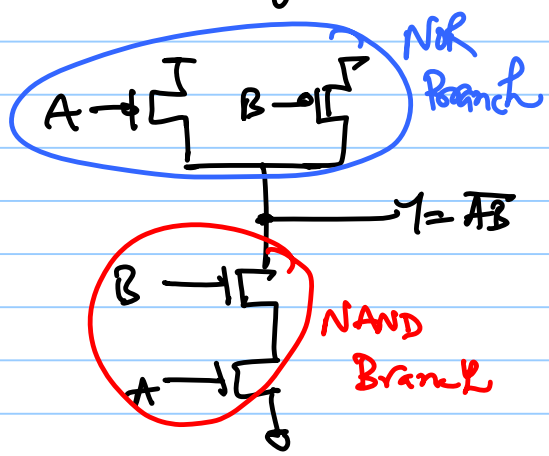

$\overline{out}$
out
A
$\bar{A}$

CML NAND Gate



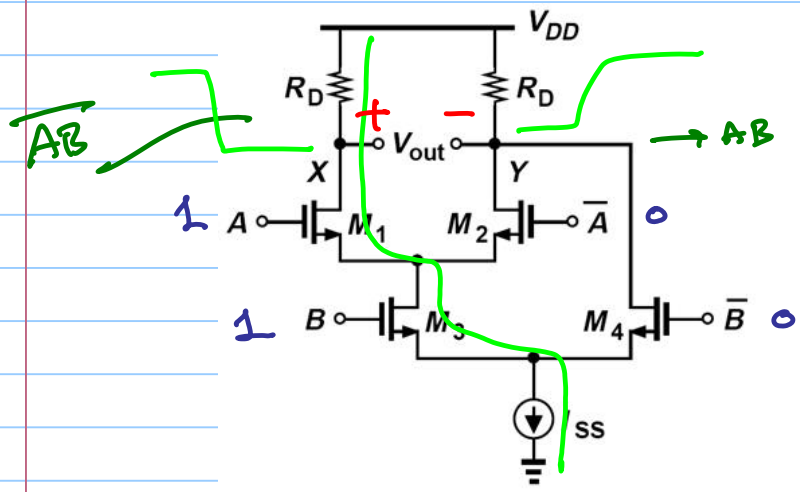


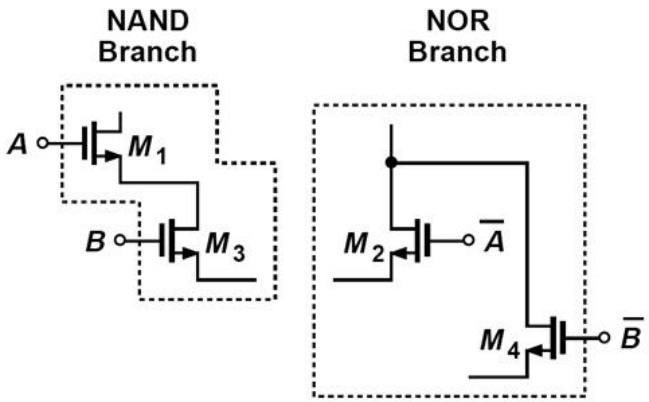
CMOS NAND Gate

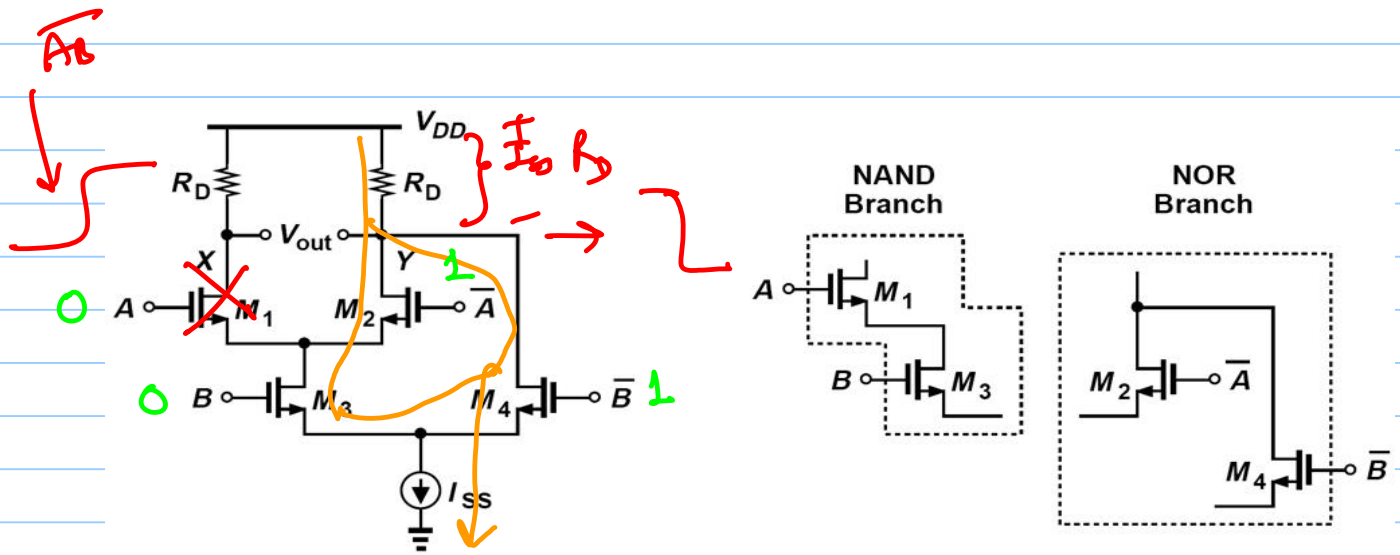


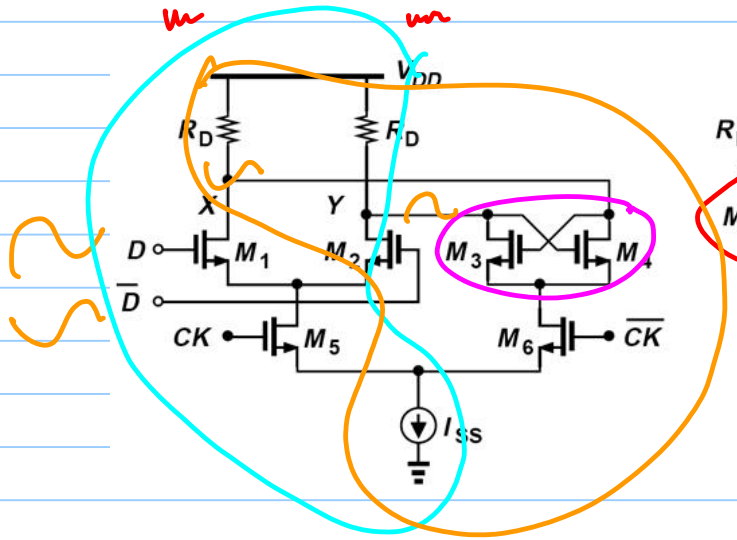
$Y = \overline{AB}$

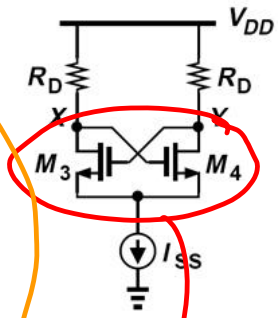
AND / NAND Gate

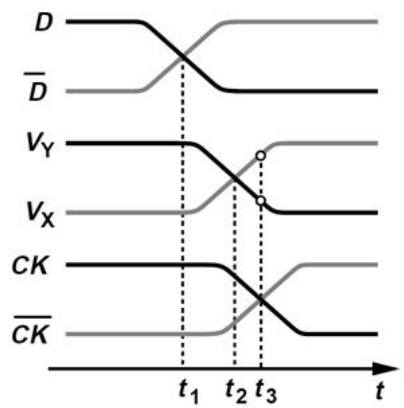




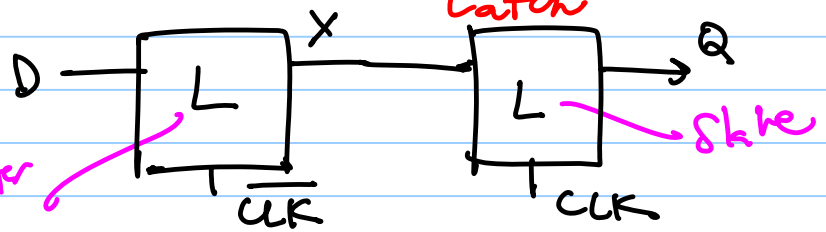

V_{DD}
R_D
R_D
V_{out}
X
Y
A
M_1
M_2
$\overline{A}$
B
M_3
M_4
$\overline{B}$
I_{SS}
NAND Branch
A
M_1
B
M_3
NOR Branch
M_2
$\overline{A}$
M_4
$\overline{B}$



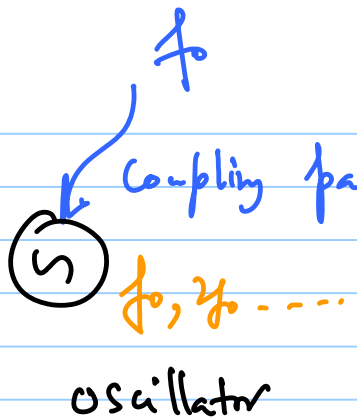




Cross-coupled Latch



CML flip flop



"injection locking"

Project Due → Deadline on the Website ✓✓

Final Exam → Take Home / Open Book