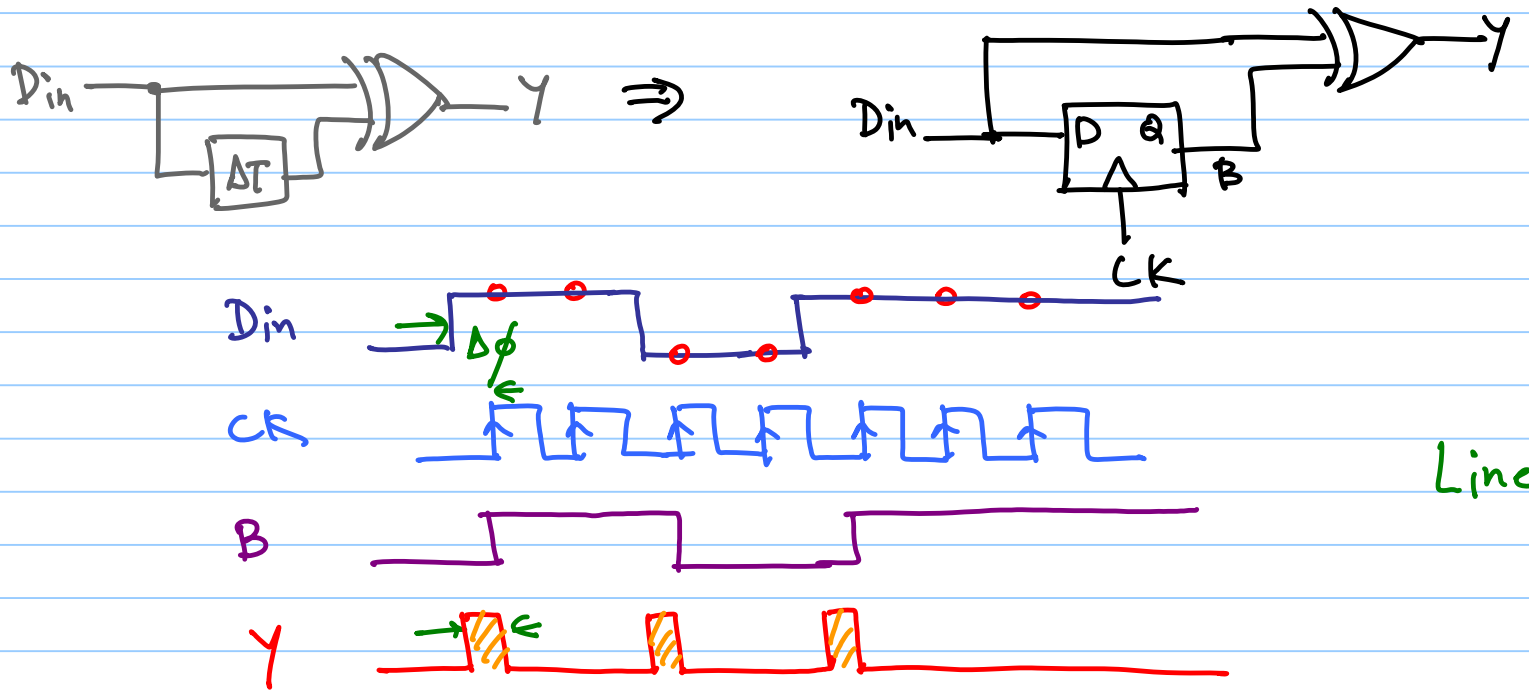
ECE 504 - Lecture 25

Note Title 11/28/2016

Hogge PD:

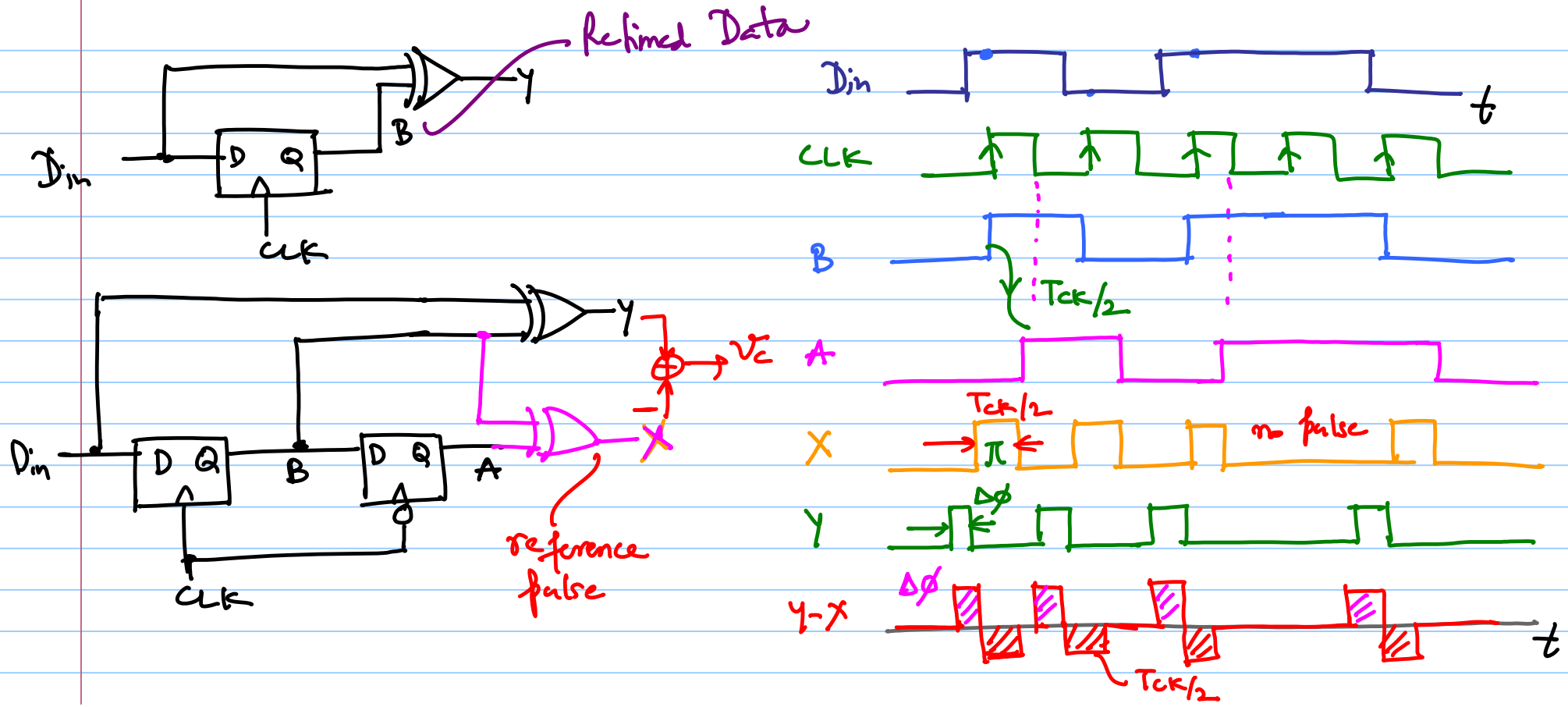


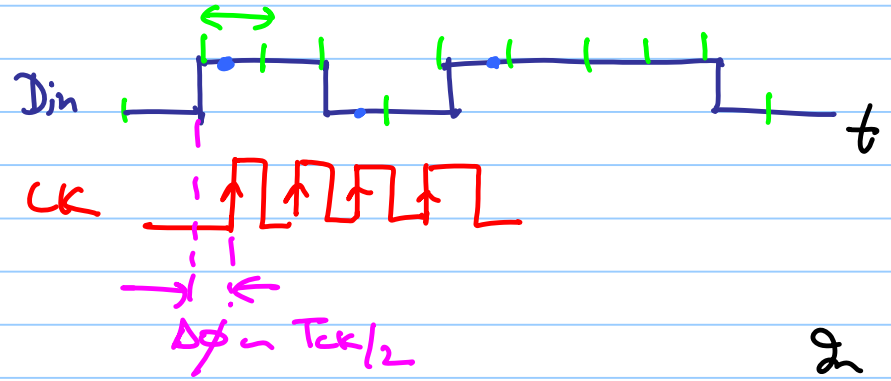
Linear PD

Issue: Average value of $Y \rightarrow V_c$ is a function of data density, fails to uniquely represent the $\Delta\phi$ between data & clk

↳ two different phase errors for different data density could have the same V_c output

↳ need to eliminate dependence on data density.


Retimed Data
Din
D Q
B
Y
CLK
Din
D Q
B
D Q
A
Y
X
Vc
reference pulse
CLK
Din
t
CLK
B
Tck/2
A
Tck/2
X
π
no pulse
Δφ
Y
Δφ
Y-X
Tck/2
t



Hogge PD (1985)

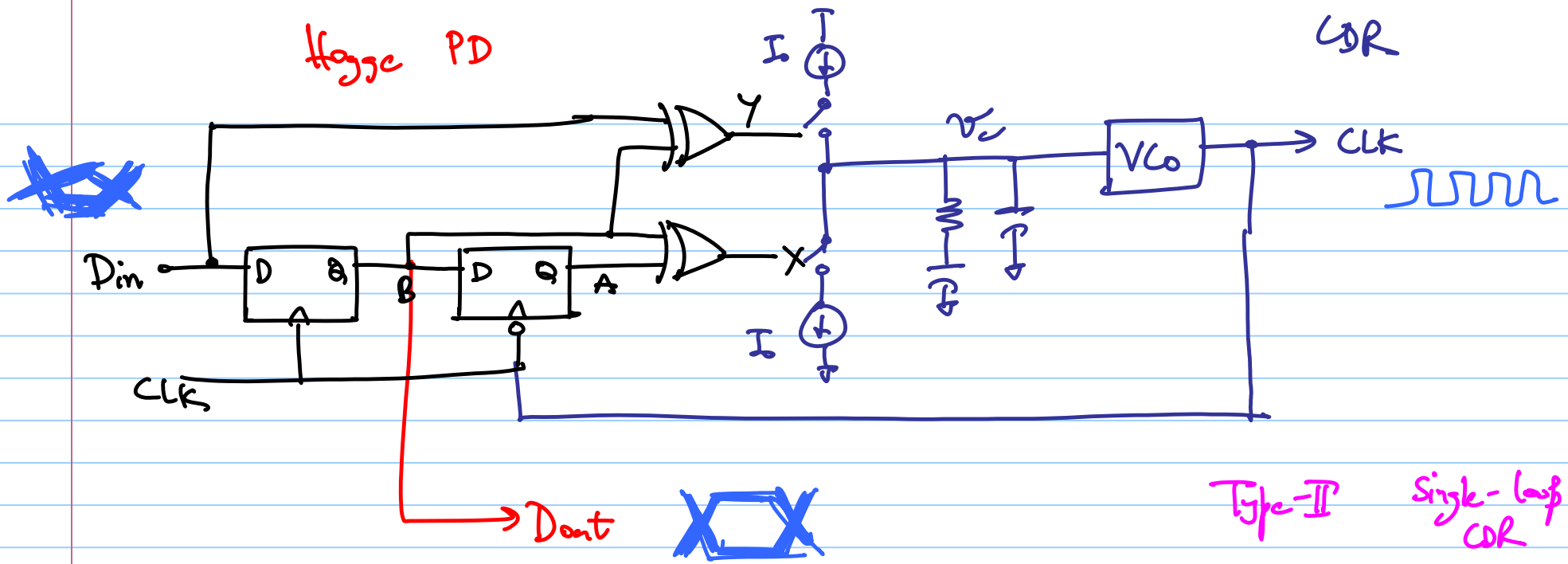
In locked condition Y & X produce equal widths

$\Rightarrow$ avg $(Y-X) = 0$

Since pulse width of $X = T_{ck}/2$

$\Rightarrow$ PW of Y is also forced to be $T_{ck}/2$

$\Rightarrow$ Clock aligns to the center of the data when locked.


Hogge PD
CDR
Din
D
Q
B
A
CLK
Y
X
I
I
v_c
VCO
CLK
Dout
Type-II
Single-loop CDR

① finite delay in ff's → t_{cq}

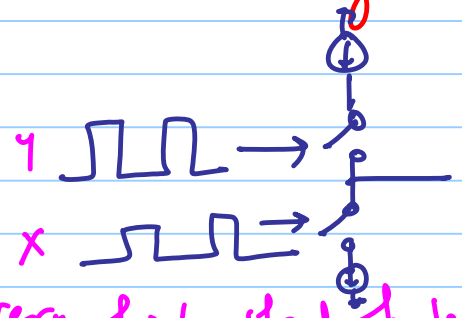
↳ changes pulse width of Y by $\Delta T = t_{cq}$

↳ phase error

↳ at high speeds ΔT could be a large fraction of T_{CK}

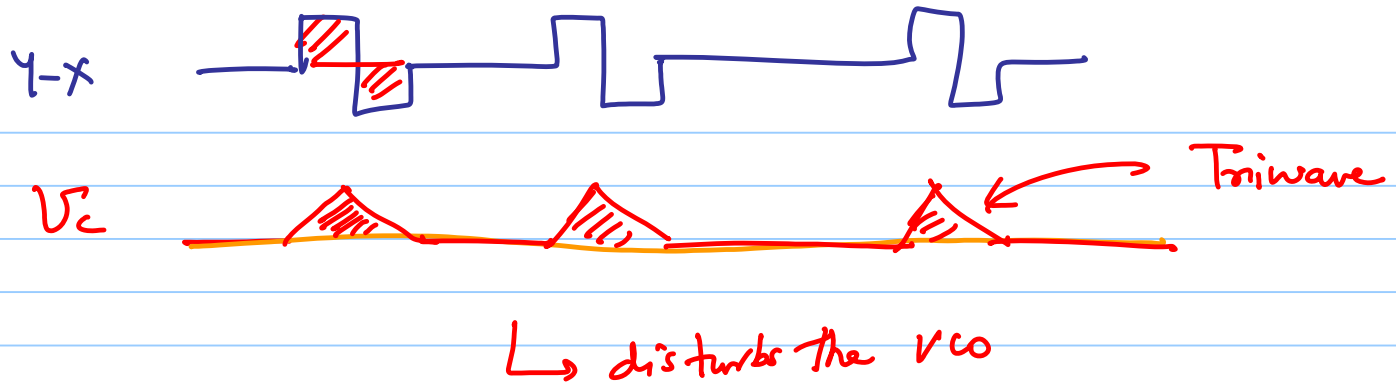
↳ degrades jitter tolerance

② At X + Y



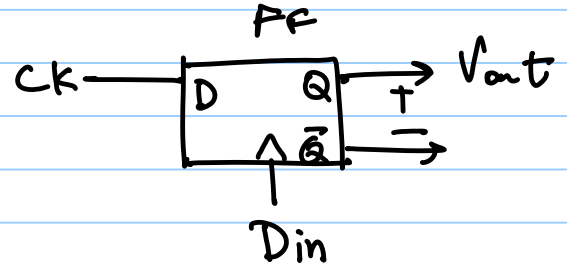
very high speed pulses → Dead zone issues

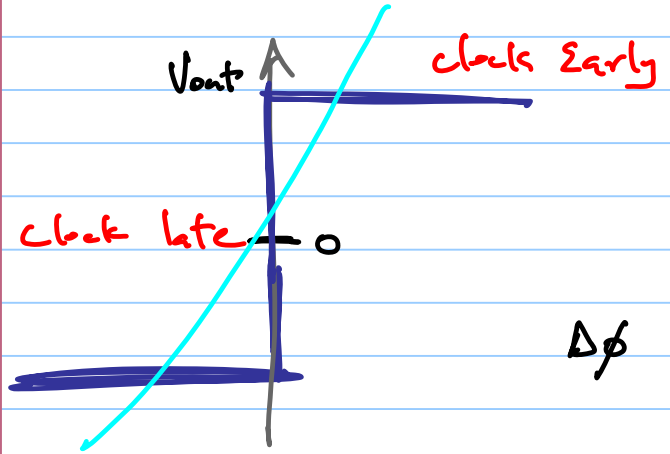
③

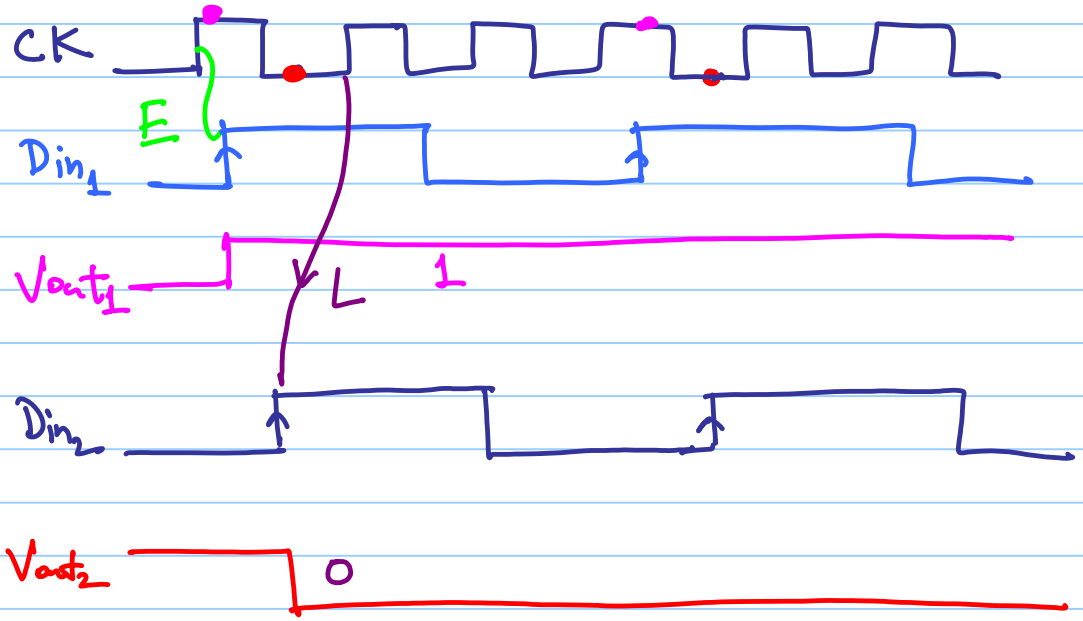


↳ disturbs the VCO

Binary PD :

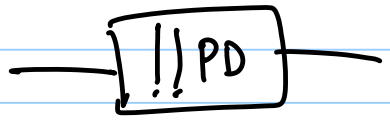

FF
CK
D
Q
$\bar{Q}$
T
Vout
Din


Vout
clock Early
clock late
0
Δφ

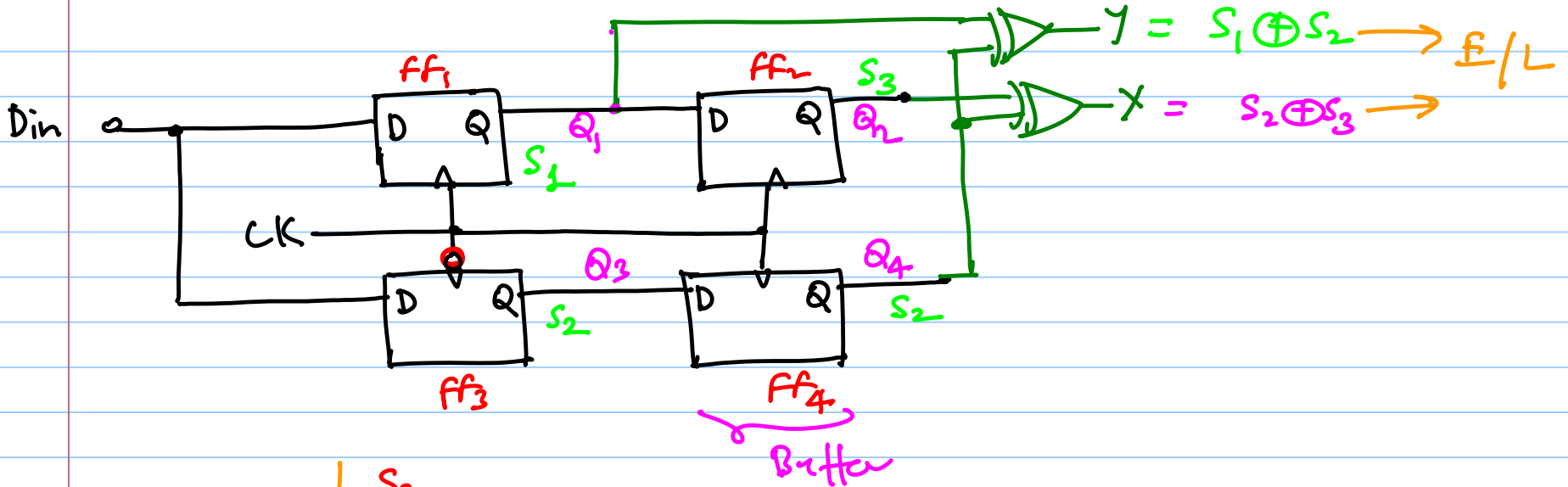

CK
E
Din_1
$Vout_1$
L
1
Din_2
$Vout_2$
0

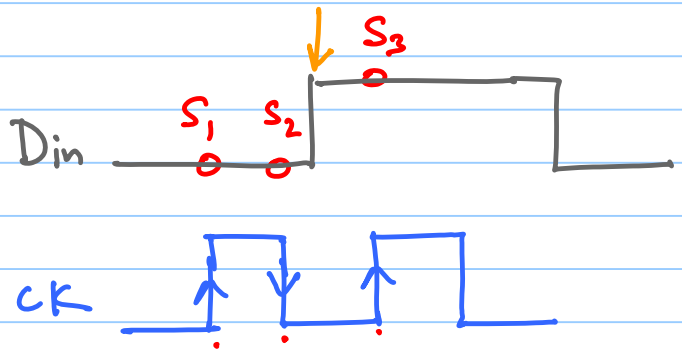
Binary PD

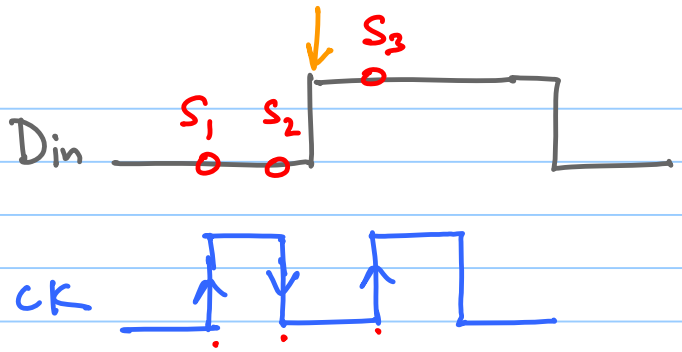
Bang-Bang PD



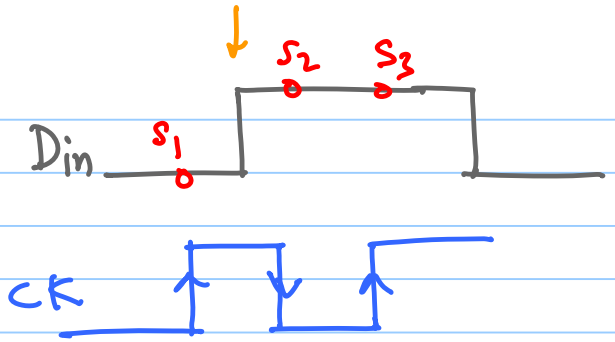
Alexander (!!) PD







clock early



clock late

If
a) $S_1 \oplus S_2 = 1$ && $S_2 \oplus S_3 = 0$ ⇒ clock is late
b) $S_1 \oplus S_2 = 0$ && $S_2 \oplus S_3 = 1$ ⇒ clock is early
c) If $S_1 \oplus S_2$ == $S_2 \oplus S_3$ ⇒ no data transition occured