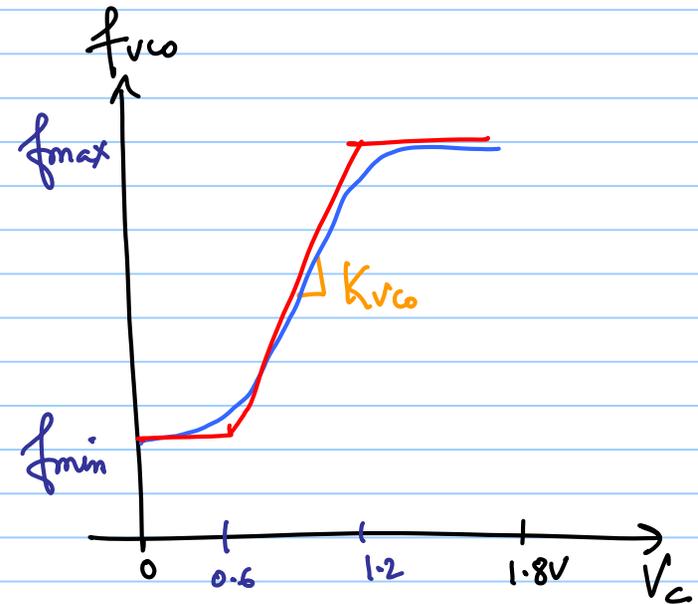
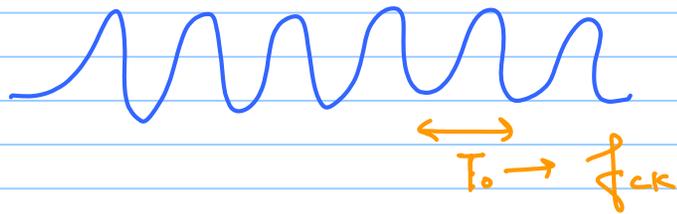


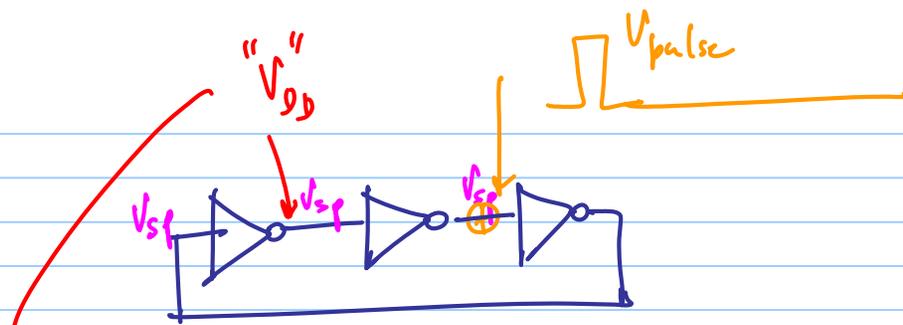
ECE 504 - Lecture 22

Note Title

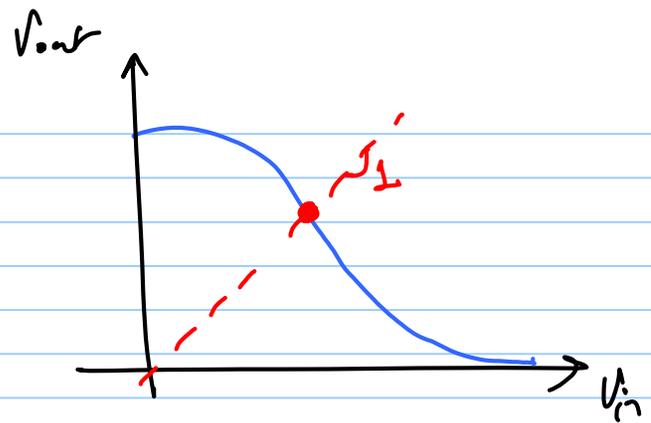
11/9/2016

$$V_c = 0.6, 0.7, 0.8$$





ADG \rightarrow set initial condition



$$S_{V_R} = 4KTR$$

$$\int_{\phi_{out}}^{V_R} \propto K_{vco}^2 \cdot R$$

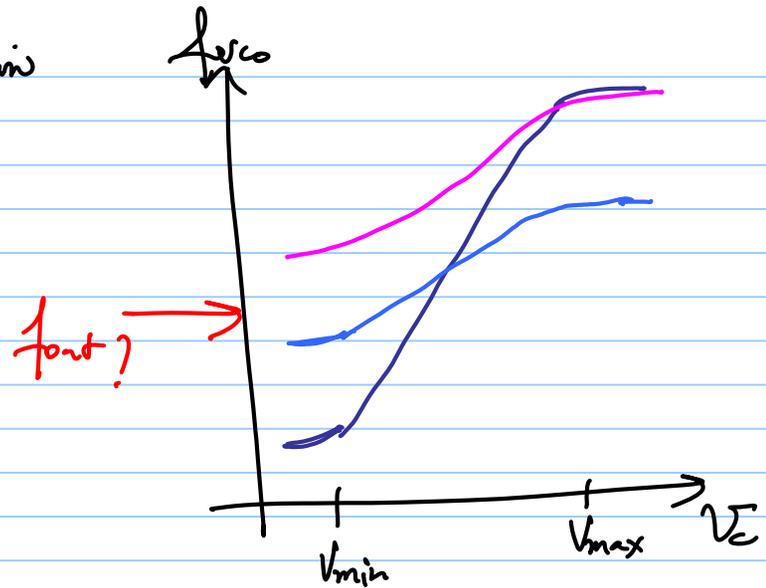
↳ Large $K_{vco} \Rightarrow$ more noise contribution from R

↳ Reduce R

$$\omega_z = \frac{1}{RC}, \quad C \uparrow$$

Tradeoffs in reducing VCO gain

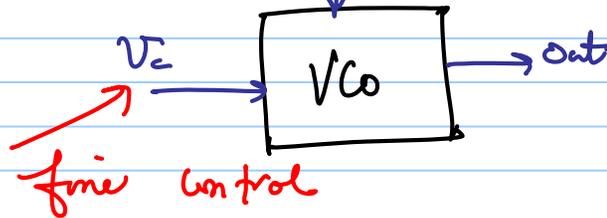
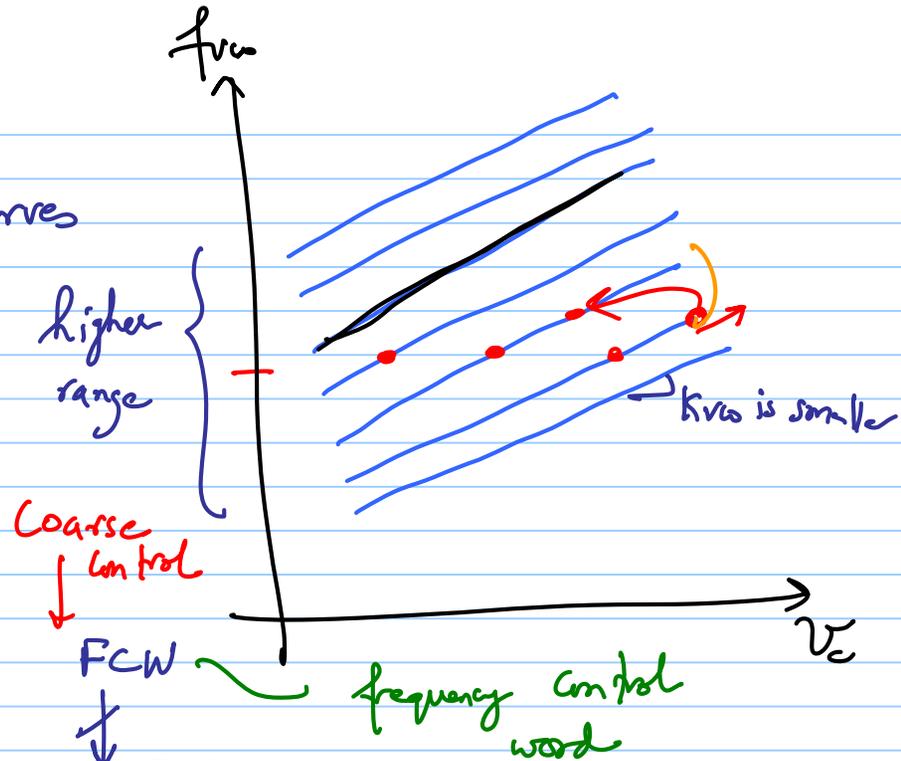
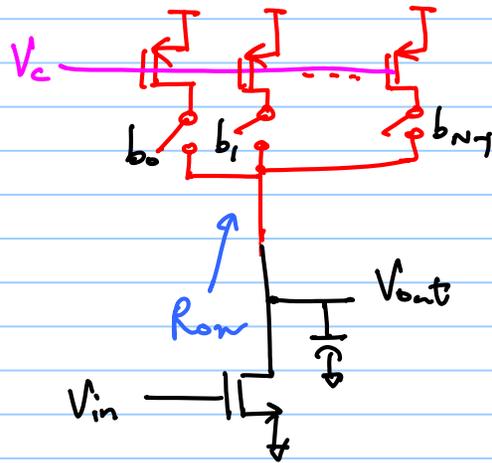
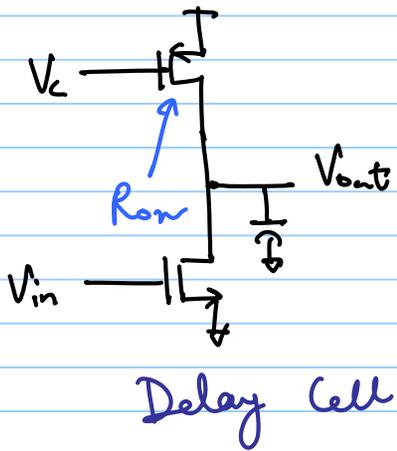
- (-) Reduced VCO operating range
- (+) Better phase noise performance for the overall PLL
- (+) Smaller C_1 & C_2
- (+) Better spur performance



We want large VCO operating range to cover PVT variation

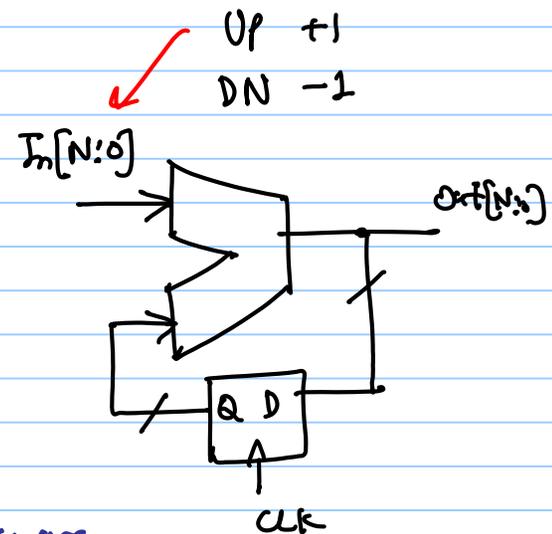
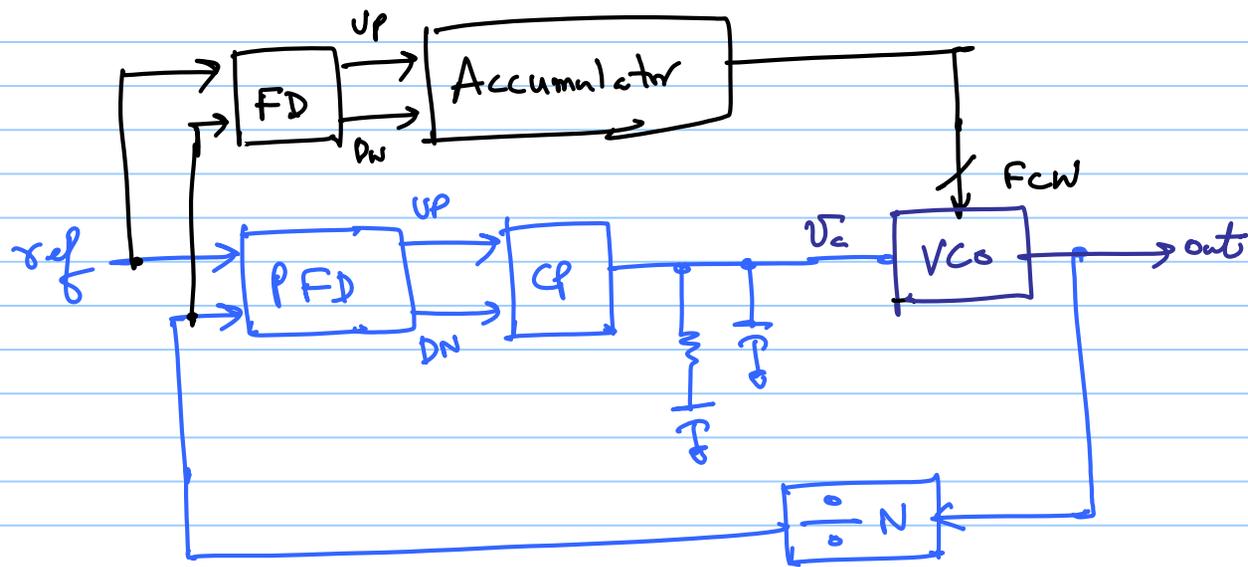
* Each curve has low k_{vco}

* goal is to select one of these curves

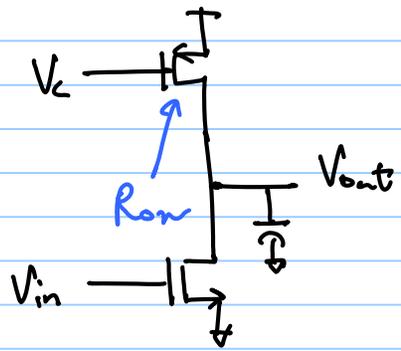


$$f_{out} \approx \frac{1}{T} = \frac{1}{RC} = \frac{G}{C} = \frac{\sum_{i=0}^{N-1} b_i f_i}{C}$$

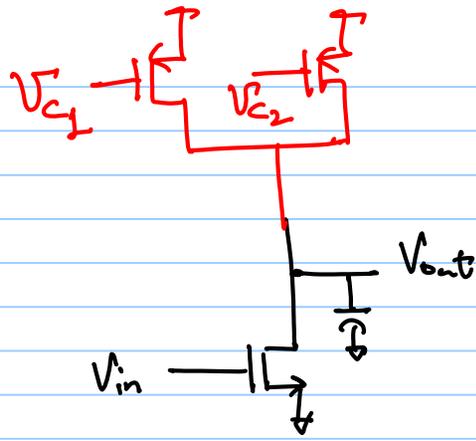
$$b_i \in \{0, 1\}$$



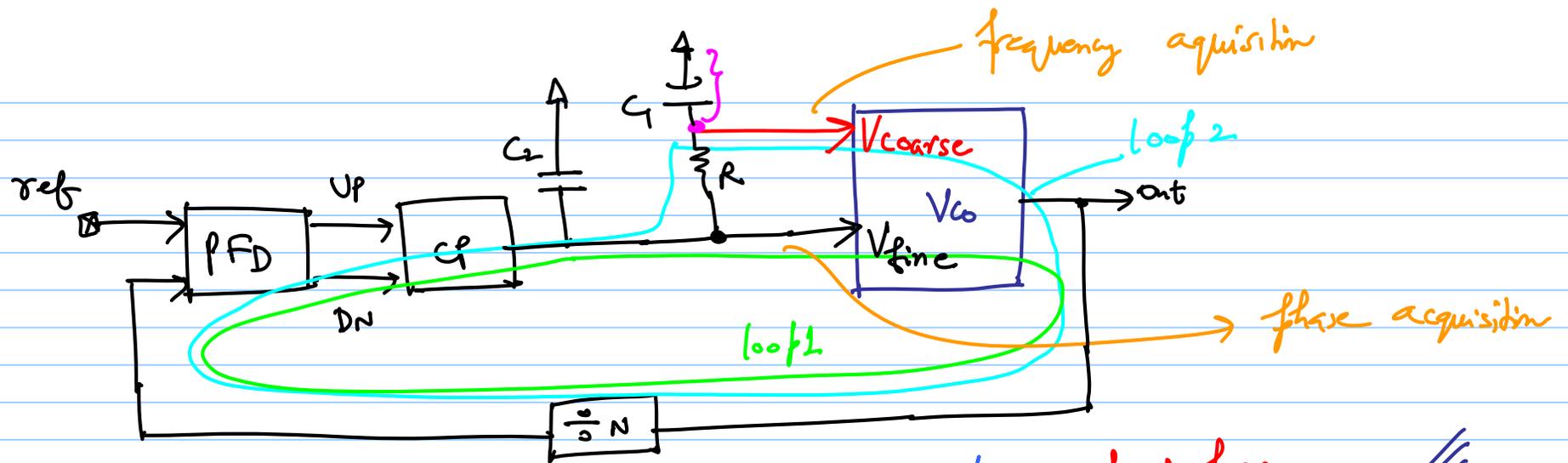
↳ Jitter due to abrupt jump from one curve to another



Delay Cell



* Split-tuned with continuous tuning



* V_{CO} is controlled using two voltages

- V_{coarse} port has high gain
 - high gain $V_{coarse} \rightarrow$ works similar to a PLL
- V_{fine} port
 - low gain V_{fine} port \rightarrow lower $k_{vco} \rightarrow$ better total phase noise performance

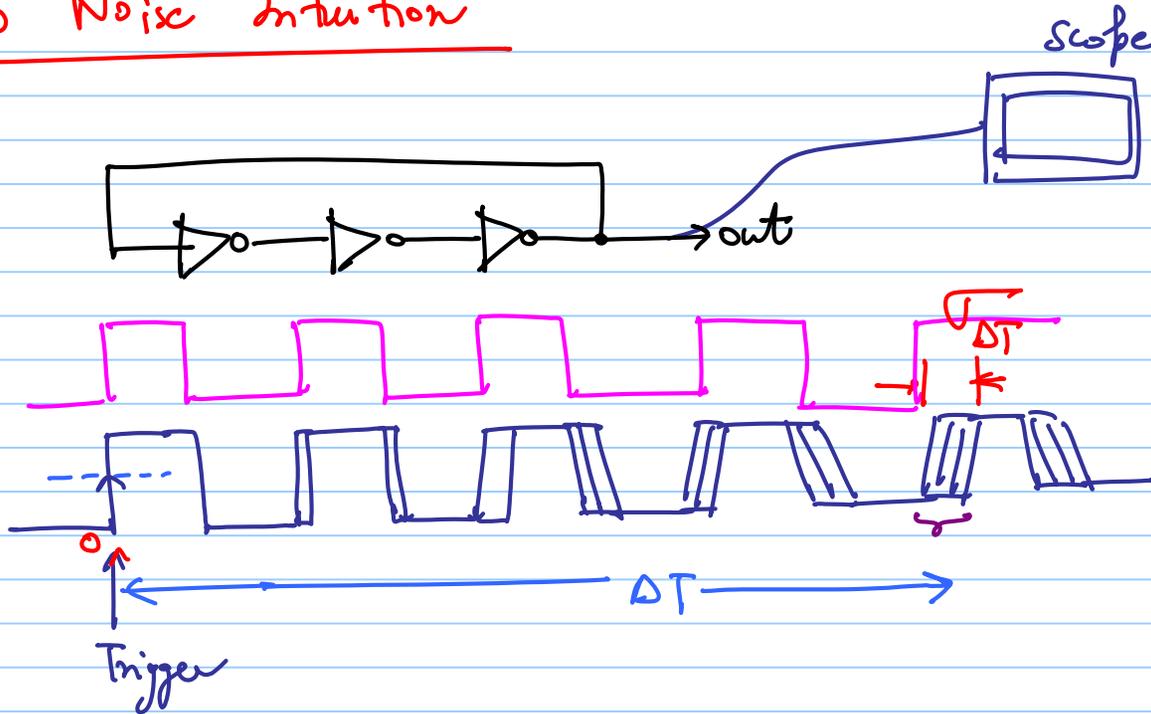
↳ Two coupled-feedback loops

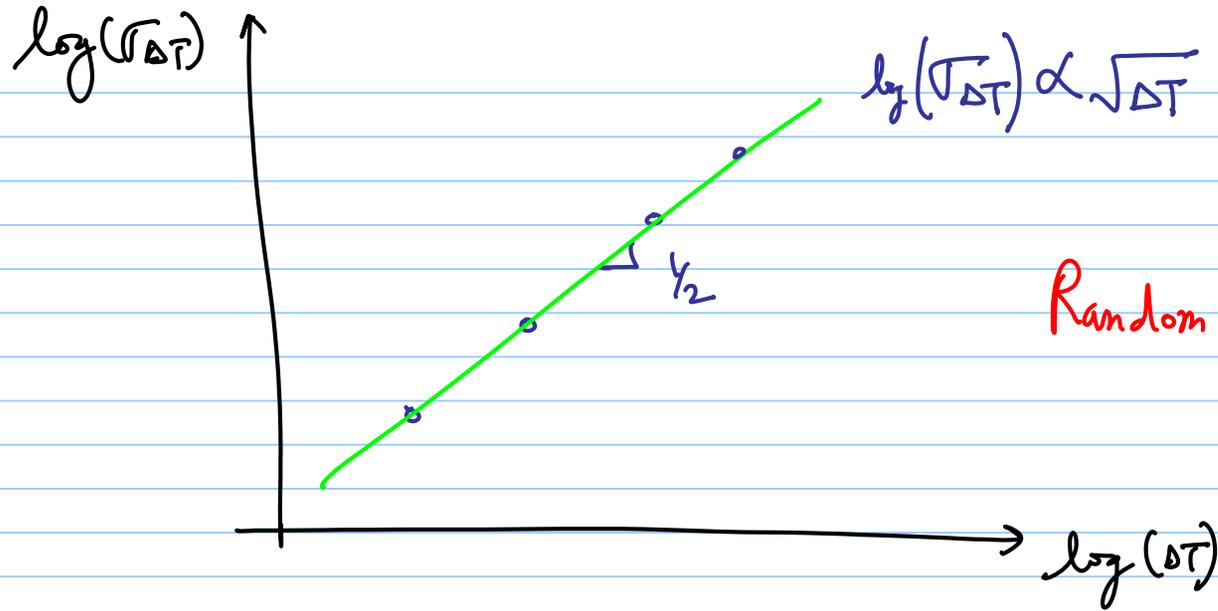
↳ potential instability

↳ Need low gain path to determine loop dynamics (fast)

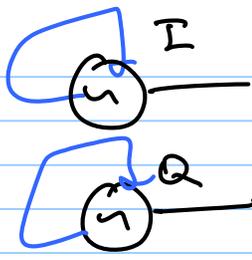
[See Scanned Notes on analytical details]

VCO Noise Intuition

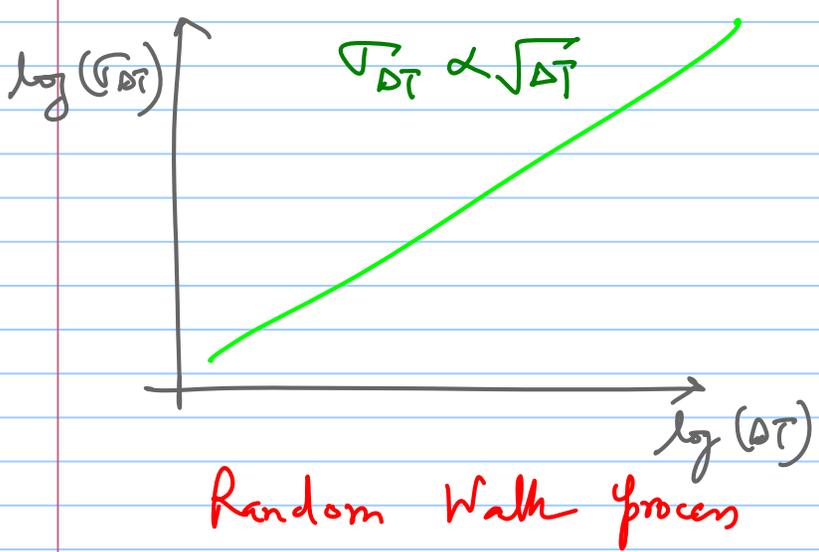




Accumulated jitter depends upon the # of edge transitions
 ↳ NOT the number of steps in the VCO



Open-loop VCO



Closed-loop VCO (PLL)

