ECE 4/504 PLL AND HIGH-SPEED LINK DESIGN

COURSE INTRODUCTION

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COURSE OUTLINE

Instructor : Dr. Vishal Saxena
Office BEL 318, Phone: 208-885-6870
Email: vsaxena AT uidaho DOT edu

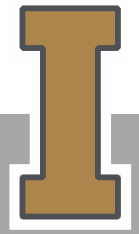
Time : Mon/Wed, 3:30-4:45 PM

Course dates : Aug 22 – Dec 16, 2016

Location : JEB 25

Office Hours : Mon/Wed 2:00-3:00 PM (or by appointment)

Website : http://lumerink.com/courses/ece504/f16/ECE504.htm



COURSE TOPICS

- Design and analysis of
  - Phase-locked Loops (PLLs)
    - VCOs, phase-noise analysis, integer and fractional architectures, injection locking
  - Delay-locked Loops (DLLs)
  - Clock and data recovery circuits (CDR)
- High-speed Link design
  - Channel modeling, Driver Circuits, Equalizers (if time permits)
- Overview of optical interconnects

PREREQ: ECE 410. Knowledge of Analog and Digital circuits.

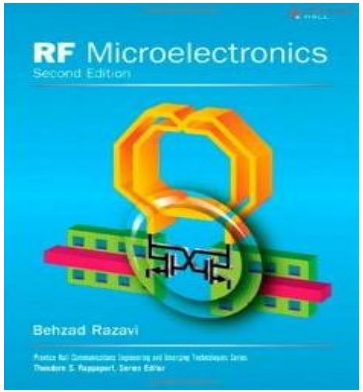
REFERENCES

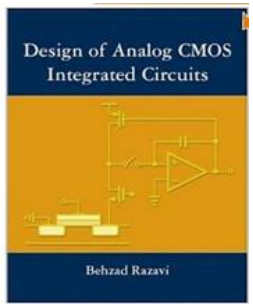
No single textbook. Lecture notes and handouts will be posted.

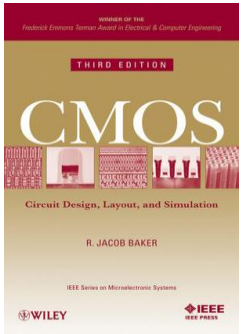
Following references are useful :

- RF Microelectronics, B. Razavi, 2nd Ed., Prentice Hall, 2012 (Chapters 9-11)
- Design of Analog CMOS Integrated Circuits, B. Razavi, McGraw-Hill, 2002 (Chapters 14-15)
- CMOS Circuit Design, Layout and Simulation – R. J. Baker, 3nd Edition, Wiley-IEEE, 2010 (Chapter 16)

For detailed references and handouts see this page.







COURSE PEDAGOGY AND GRADING

Combination of lecture notes and slides

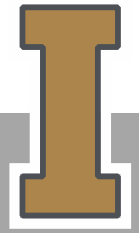
- Lecture notes to be posted online
- Additional slides, Matlab code etc. will also be posted on the site

Workload (Grading)

- Homeworks (25%)
- Midterm Exam (25%)
- Project 1 (25%)
- Project 2 or Final (25%)

Cadence is used for design-based HWs and Projects

- Usage details will be posted on the site



COURSE POLICIES

- Late work is highly discouraged (see policy on the course page)
- Neither the final exam nor final project will be returned at the end of the semester
- No internet surfing in class on any device
- Plagiarism and outsourcing (!) of work is not acceptable (See UoI Policy).
- See detailed policies on the course site