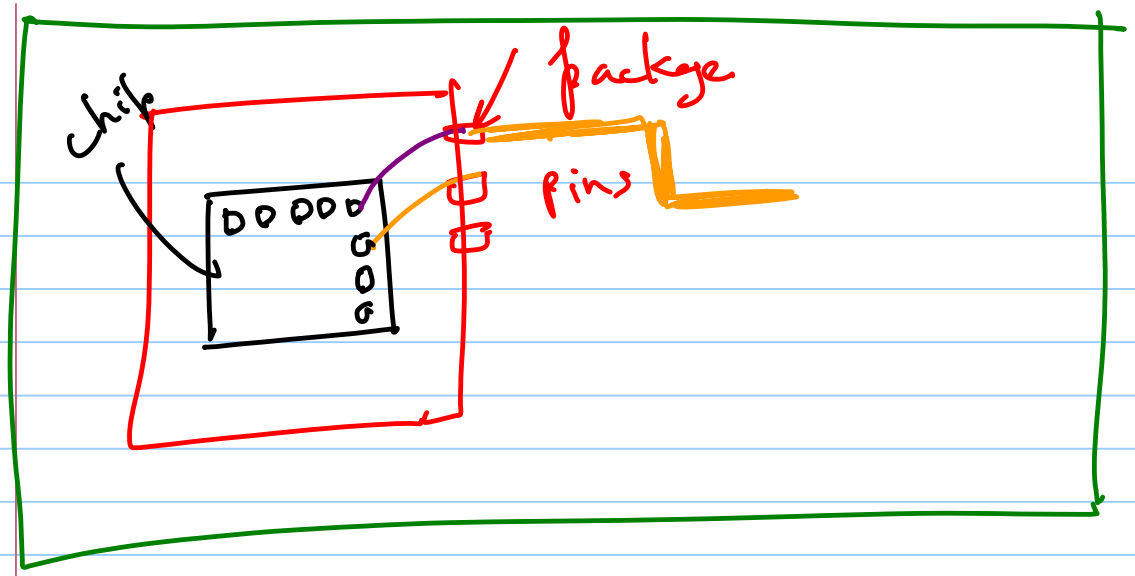
ECE 504/404 : Lecture 1

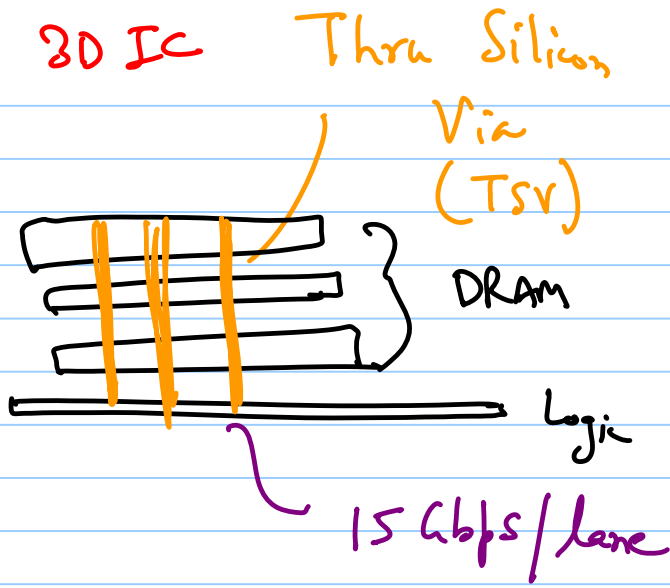
Note Title 8/22/2016

Phase locked loops (PLL)

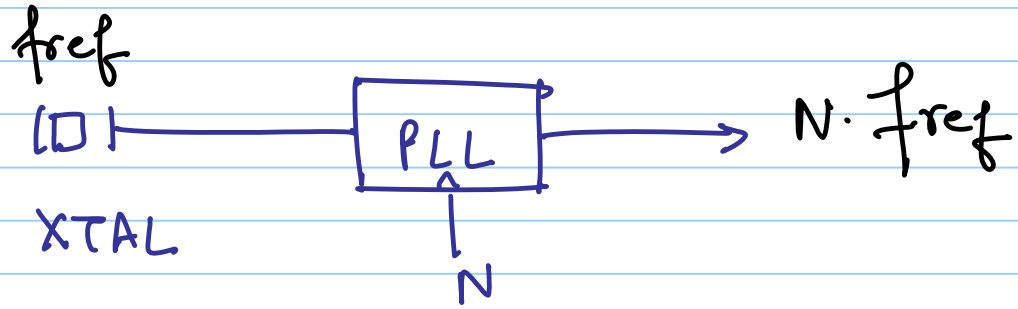
* invented about 80 years ago
* Applications:
  * FM TX/RX
  * spread spectrum clocking
  * Memory interfaces, µP, FPGAs, ASICs
    → Hybrid Memory Cube (HMC)
  * optical fiber communications
  * RF synthesizer

* XBox
* Displays
* Deep Learning ASICs


chip
package
pins
PCB


3D IC
Thru Silicon Via (TSV)
DRAM
Logic
15 Gbps/lane

① Frequency Synthesis

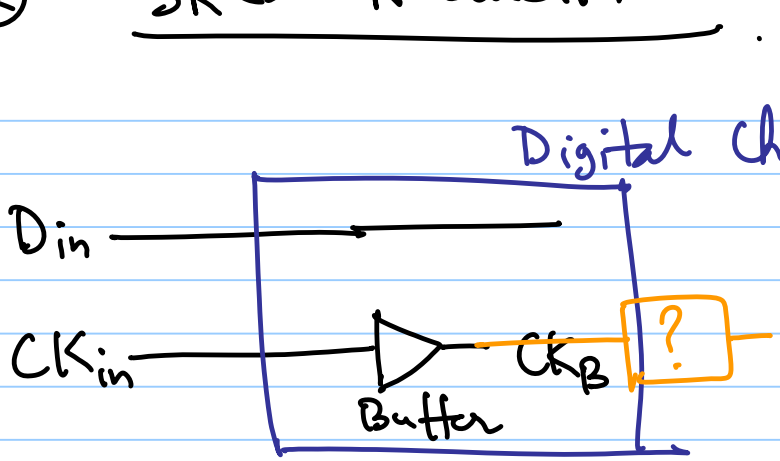


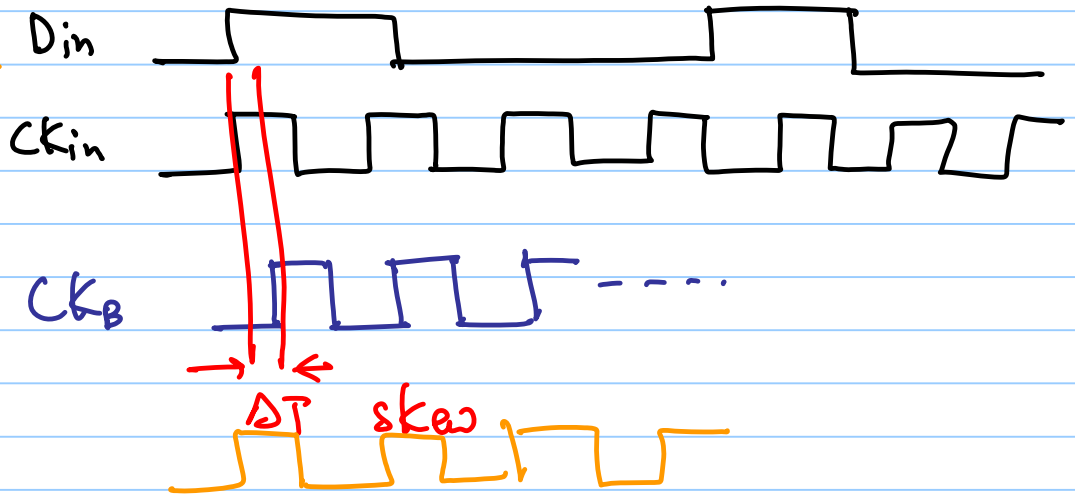
N can be integer as well as a fraction

$N \sim \frac{N_1}{N_2}$

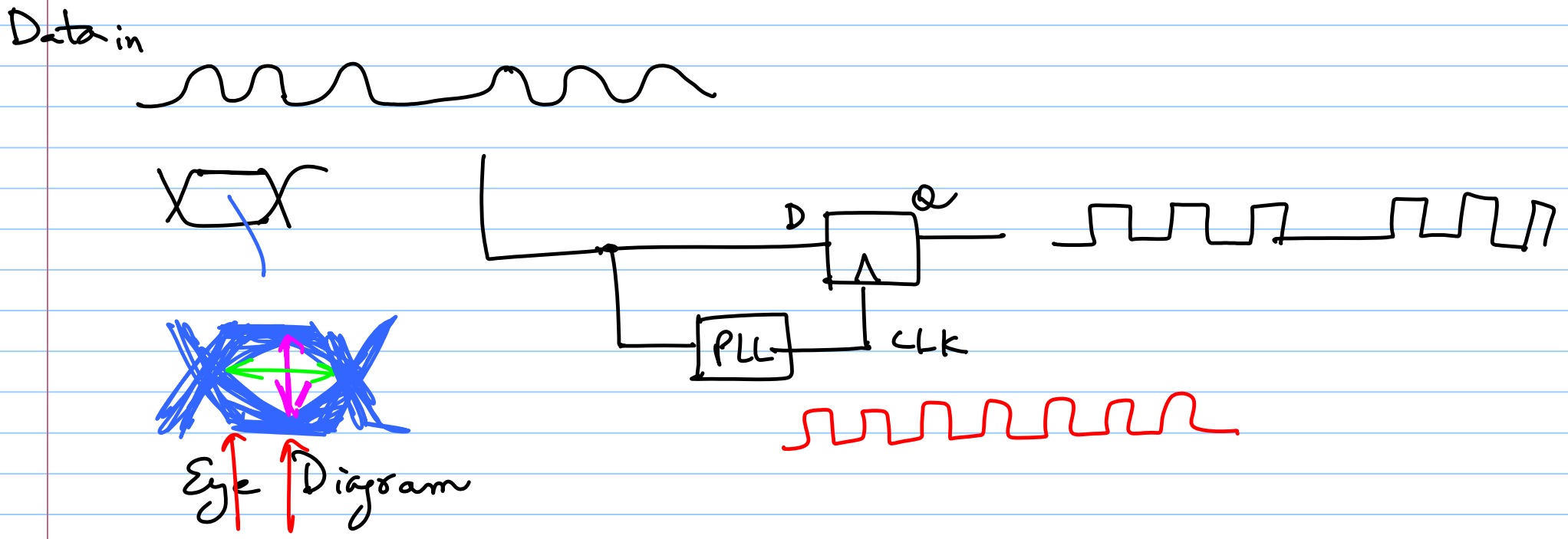
e.g. GSM, 900 to 925 MHz in steps of 30 kHz

② Skew Reduction

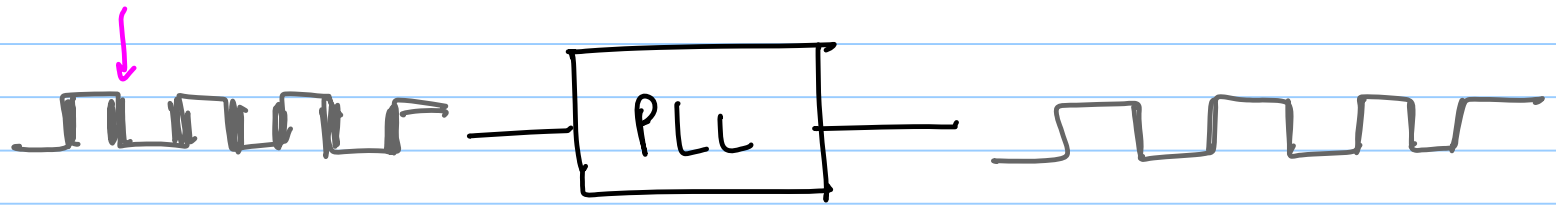




③ Clock Recovery



④ Jitter reduction

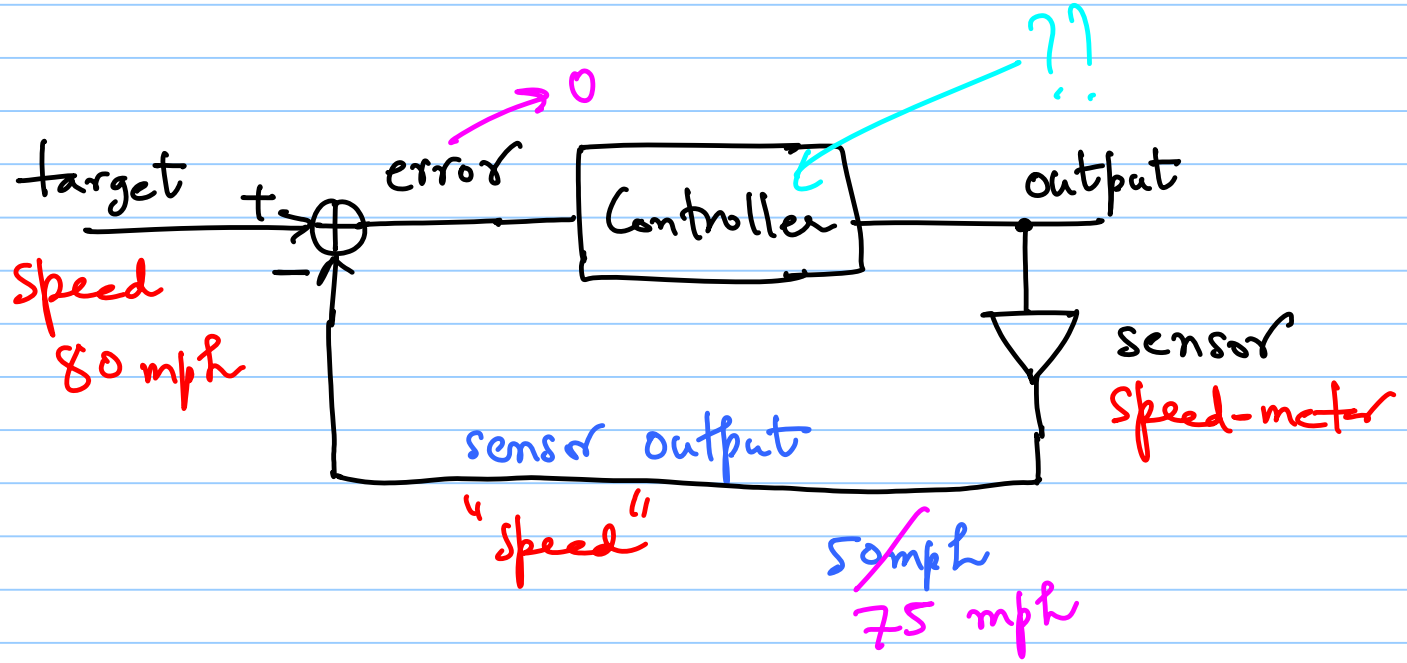


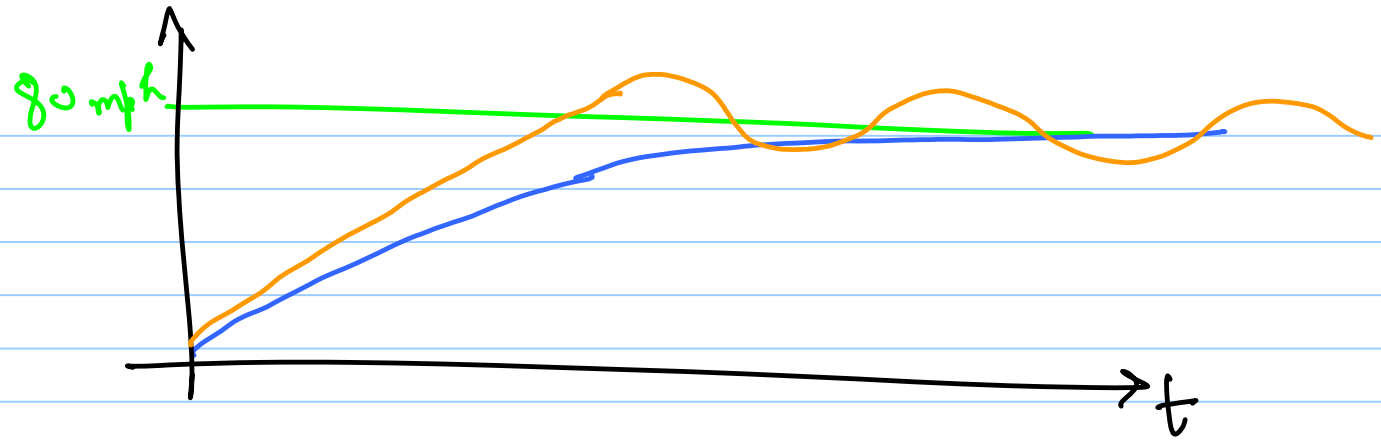
Jittery input

A PLL suppresses fast jitter components in the input

⑤ Modulation / Demodulation in Wireless System
↳ FM Receiver

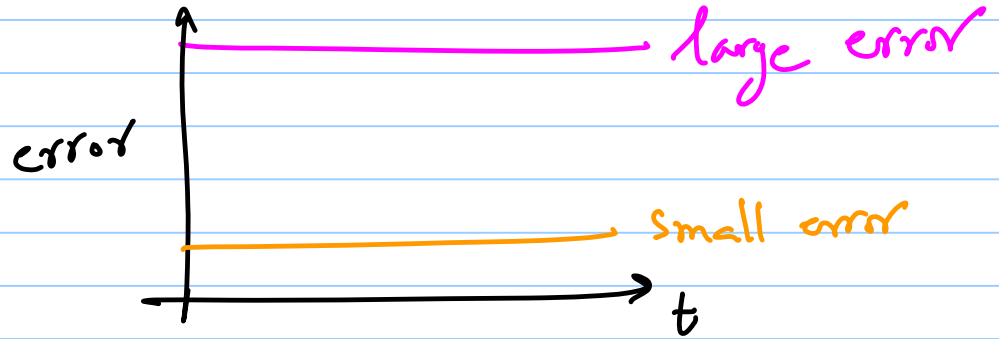
Negative feedback loops :

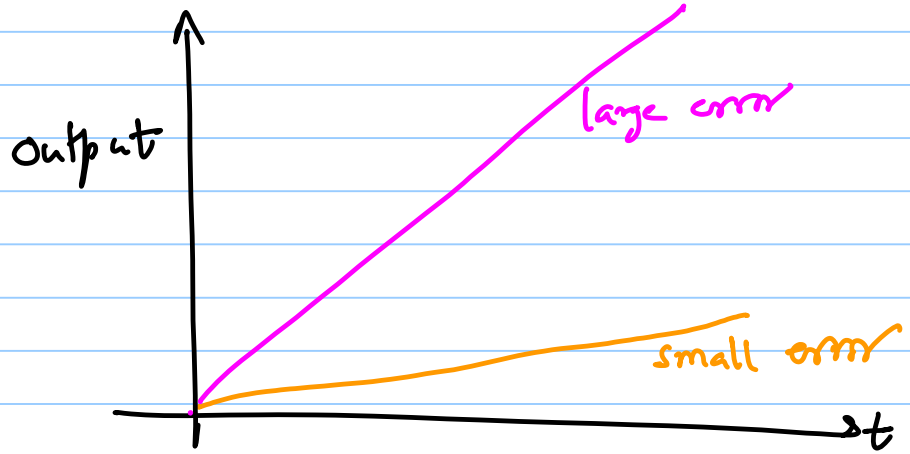



80 mph
t

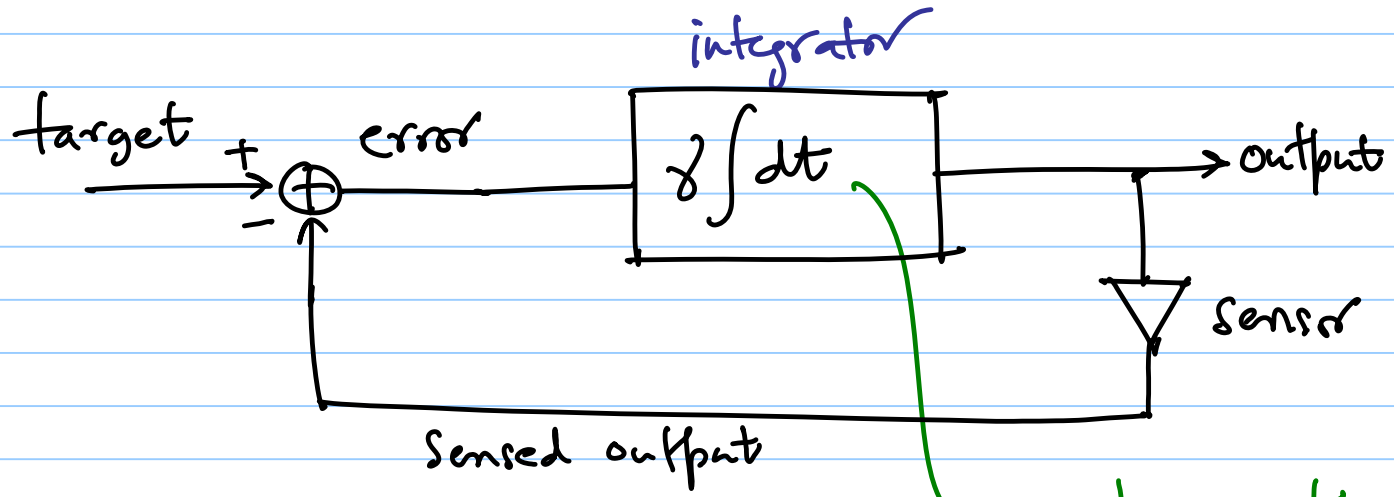
What is the nature of the controller?

* Lets say the output sensor is stuck (open-loop system)
  ↳ error is constant



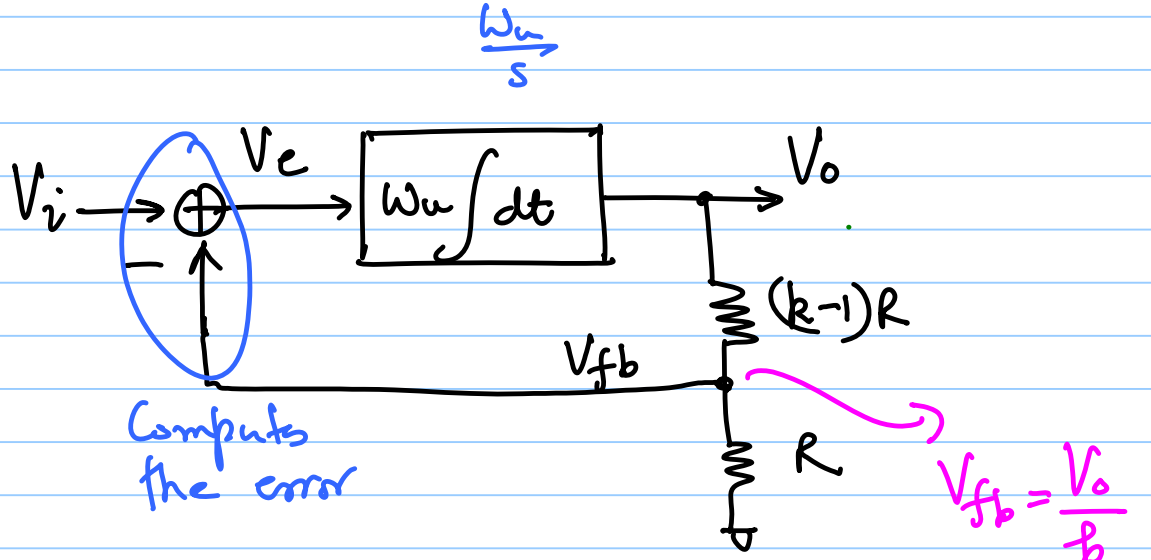


Use an integrator as the controller



Change the output until the error goes to zero.

Example: Negative feedback Amplifier



$$V_e = V_i - \frac{V_o}{k} \to 0$$

$$V_o = kV_i$$