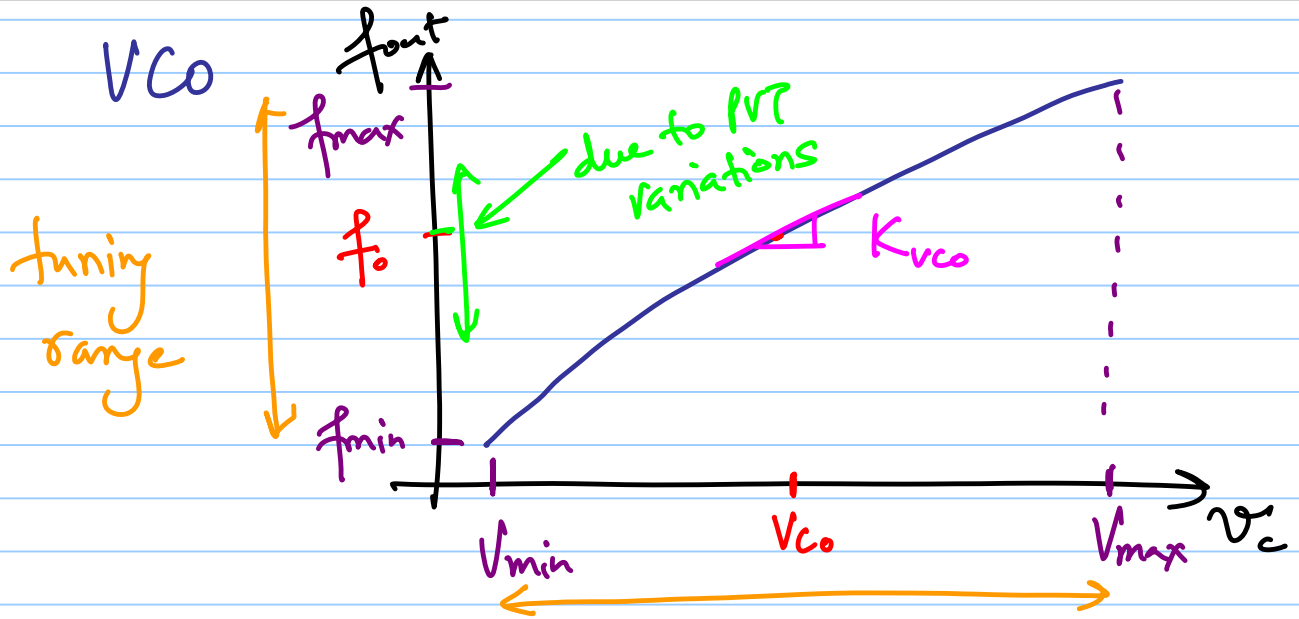
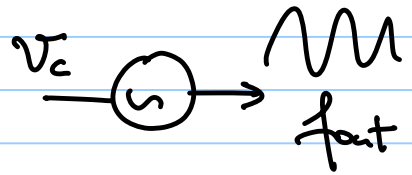
ECE 504 - Lecture 16

Note Title 10/17/2016





$$f_{out} = f_0 + 2\pi K_{VCO} \cdot v_c$$

$$\phi_{out} = 2\pi K_{VCO} \int_{-\infty}^{t} v_c \cdot dt$$

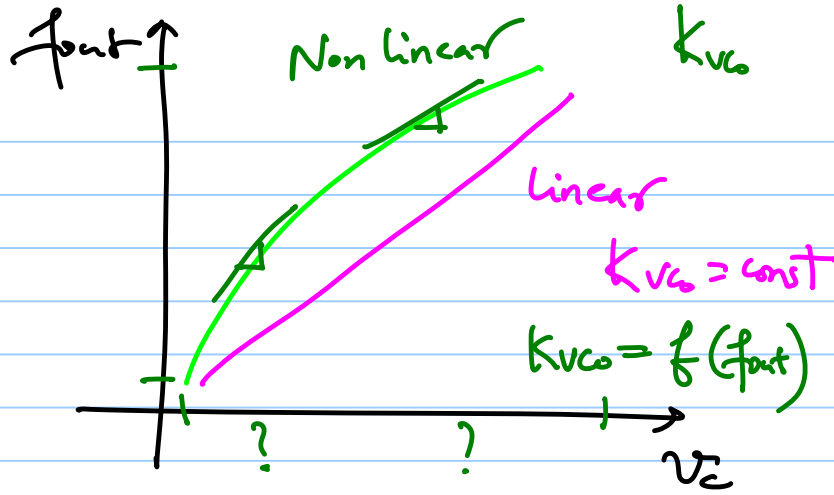
$$\Rightarrow \quad \phi_{out}(s) = \frac{2\pi K_{VCO}}{s} \cdot V_c(s)$$

Performance Metrics

* Tuning range
  - ↳ Need wide-enough tuning range to cover PVT variations
  - ↳ Wide operating range (Dijital ASIC clock generators
    - 5X tuning range
      - ↳ $\frac{f_{max}}{f_{min}} \sim 5X$

PVT variation
- ↳ f_0 varies

* Tuning linearity
  - ↳ affects loop dynamics
    - ↳ BW ($\omega_{u,loop}$) & ϕ_M
  - ↳ 2x - 3x variation in K_{VCO}
    - ↳ can "linearize" the VCO (Trade-offs)



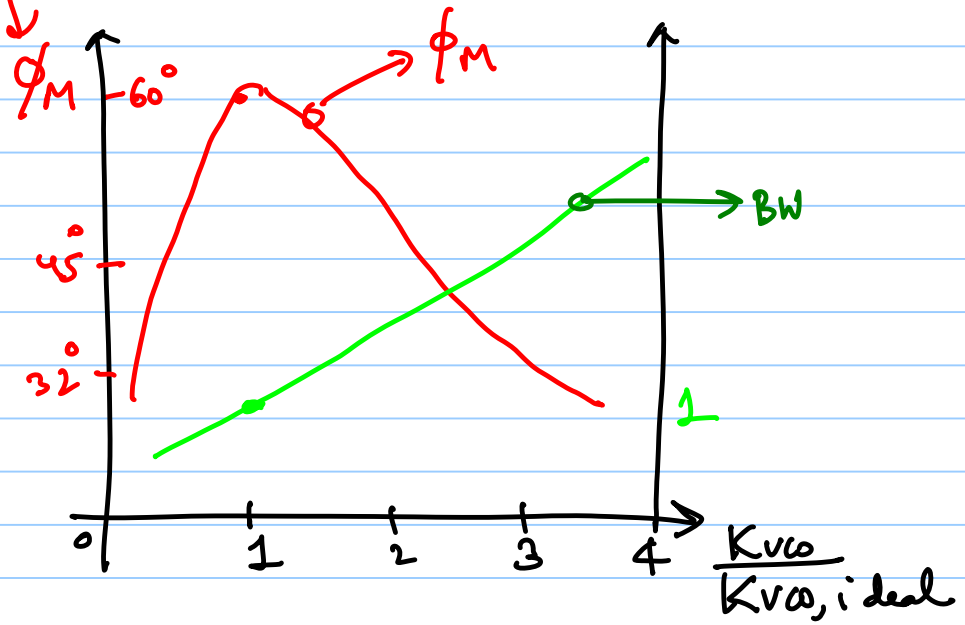
K_{VCO} has variation

* Non-linear VCO characteristics
  - ↳ behavior depends upon the operating frequency
    - ↳ settling time, ϕ_N noise performance

↳ can even cause instability (ϕ_M degrade)

↳ May want to linearize the VCO's characteristics

phase margin



* Power:

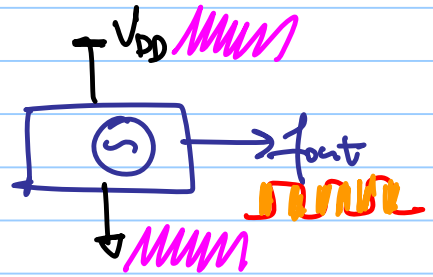
↳ Meet jitter specifications with lowest power

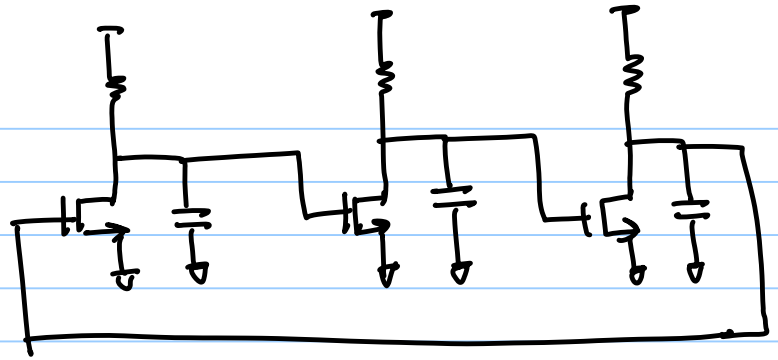
* Noise/Jitter: Later

* Power Supply Rejection (PSRR)

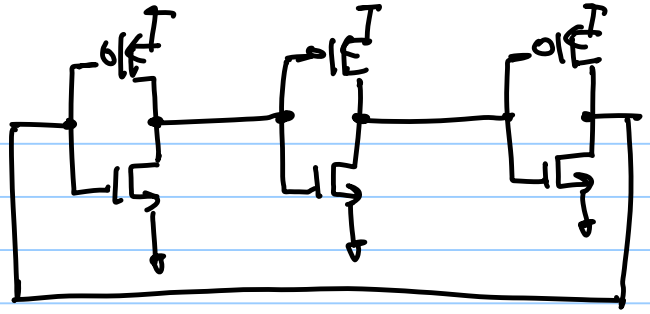
↳ Critical in digital ASIC PLLs

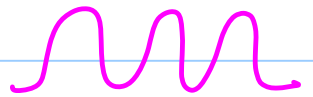
↳ Typically limits jitter performance





vs





V_{DD}

few 100 mV

0

"small-swing"

↳ PSRR

rail-to-rail

V_{DD}

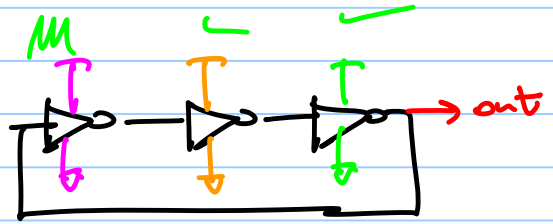
0

"Large-swing"

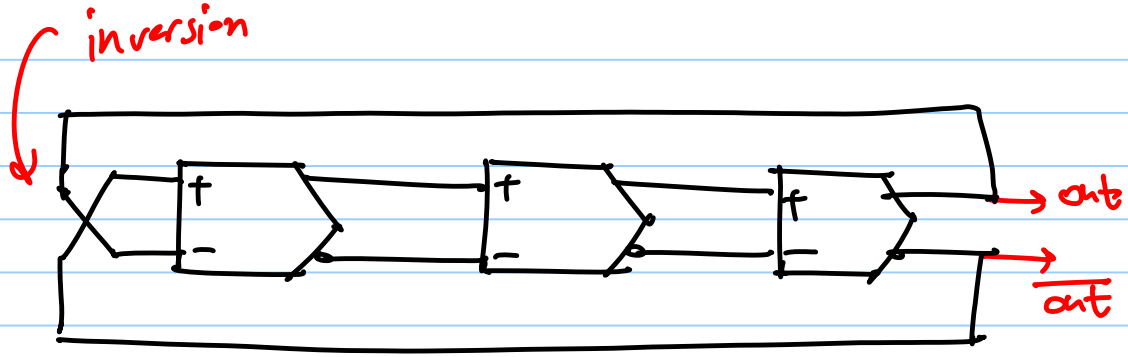
$$P_d = CV^2f$$

$$C_{par} \times V_{DD}^2 \times f_{CLK}$$

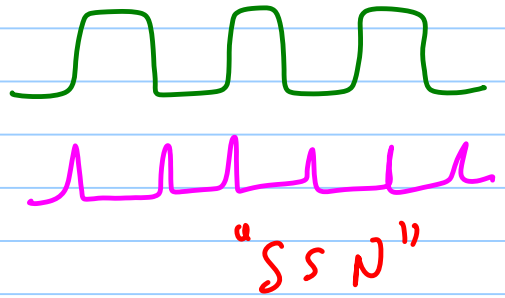
power $\propto V_{swing}^2$



vs

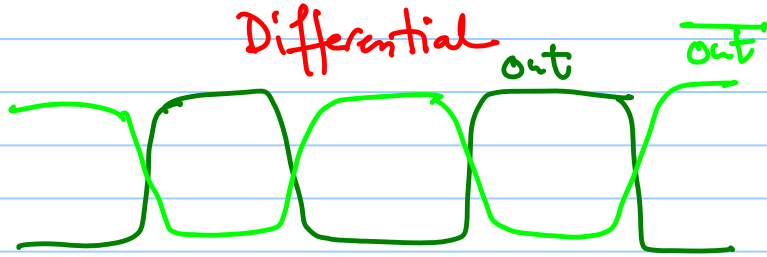


Single-ended

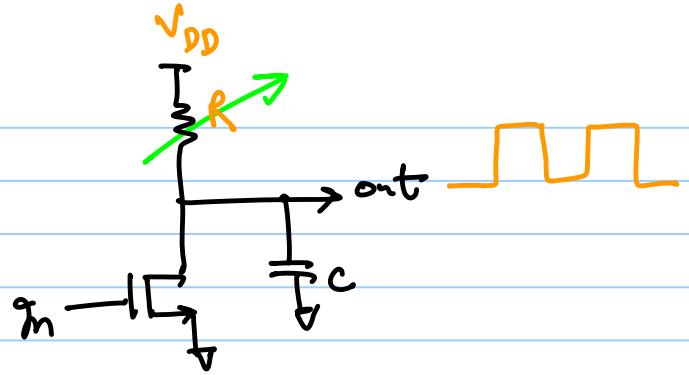


"SSN"

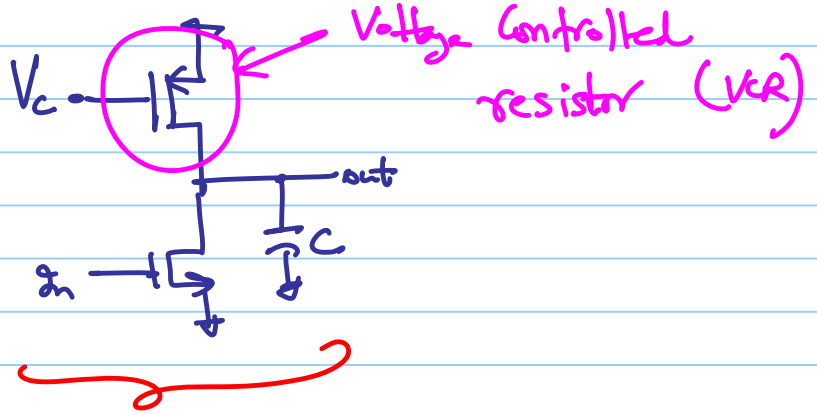
Differential



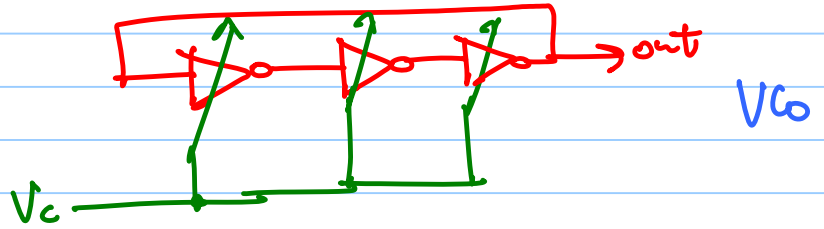
rejects common-mode disturbances
- ↳ Power supply noise
- ↳ Coupling



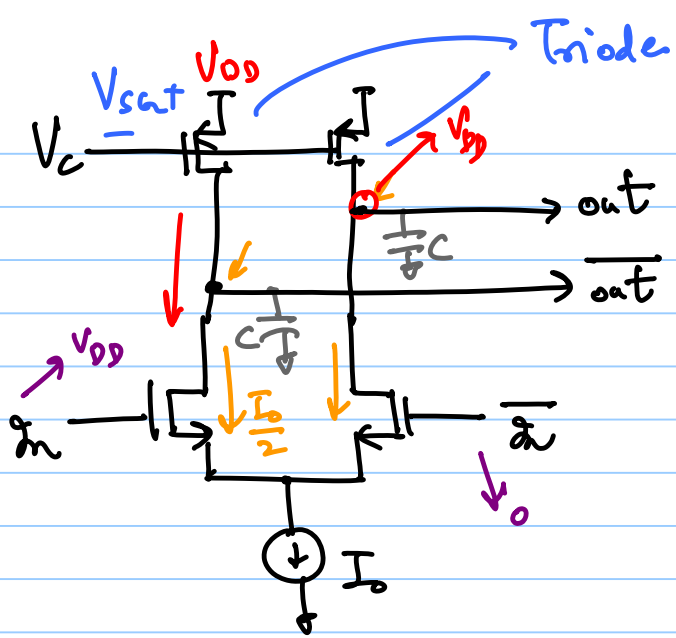
Small-swing Ring VCO

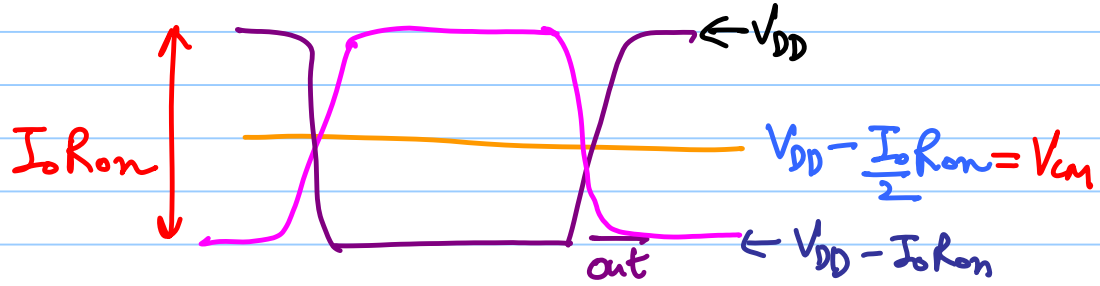


Delay Cell



VCO





Swing ⇒ $I_o R_{on}$

$$\tau = R_{on} C = \frac{C}{K_p \frac{W}{L} (V_{SG} - |V_{THP}|)}$$

$K_p = \mu_p C_{ox}$

$$= \frac{C}{K_p \cdot \frac{W}{L} (V_{DD} - V_c - |V_{THP}|)}$$

$$f_{out} \propto \frac{1}{\tau} = \frac{K_P \times \frac{W}{L} \times (V_{DD} - V_c - |V_{THP}|)}{C}$$

* Valid only when PMOS load transistors are in Triode

Triode: $V_{SD} < V_{SG} - |V_{THP}|$

$I_o R_{on} < V_{DD} - V_c - |V_{THP}|$

$\propto$ swing

$\propto f_{out}$

$$I_o \cdot \frac{1}{K_P \frac{W}{L} (V_{DD} - V_c - |V_{THP}|)} < (V_{DD} - V_c - |V_{THP}|)$$

↳ constraint to keep the load in Triode

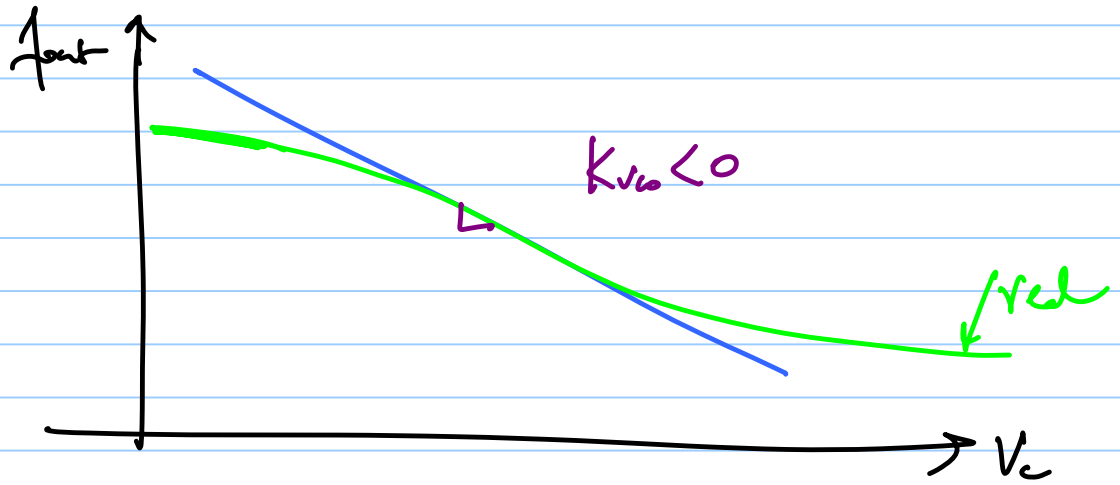
* If the above constraint is not satisfied, the PMOS load enters saturation

↳ VCO characteristics saturate

↳ the output CM-level is undefined

Differential swing $(V_{out+} - V_{out-}) = 2 I_D R_{on} \propto \frac{1}{f_{out}}$

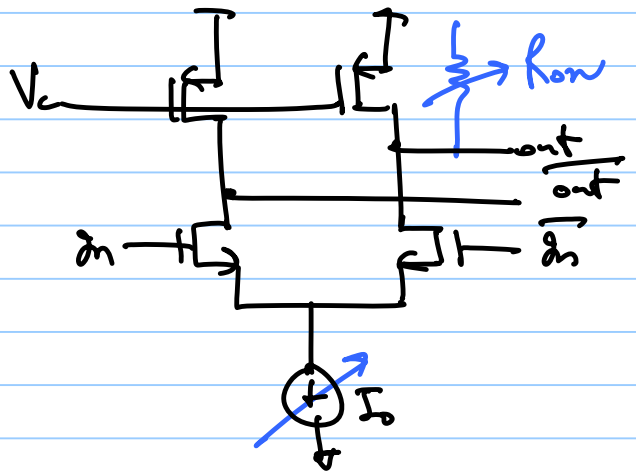
$$f_{out} \propto \frac{1}{T} = \frac{K_P \times \frac{W}{L} \times (V_{DD} - V_C - |V_{THP}|)}{C}$$



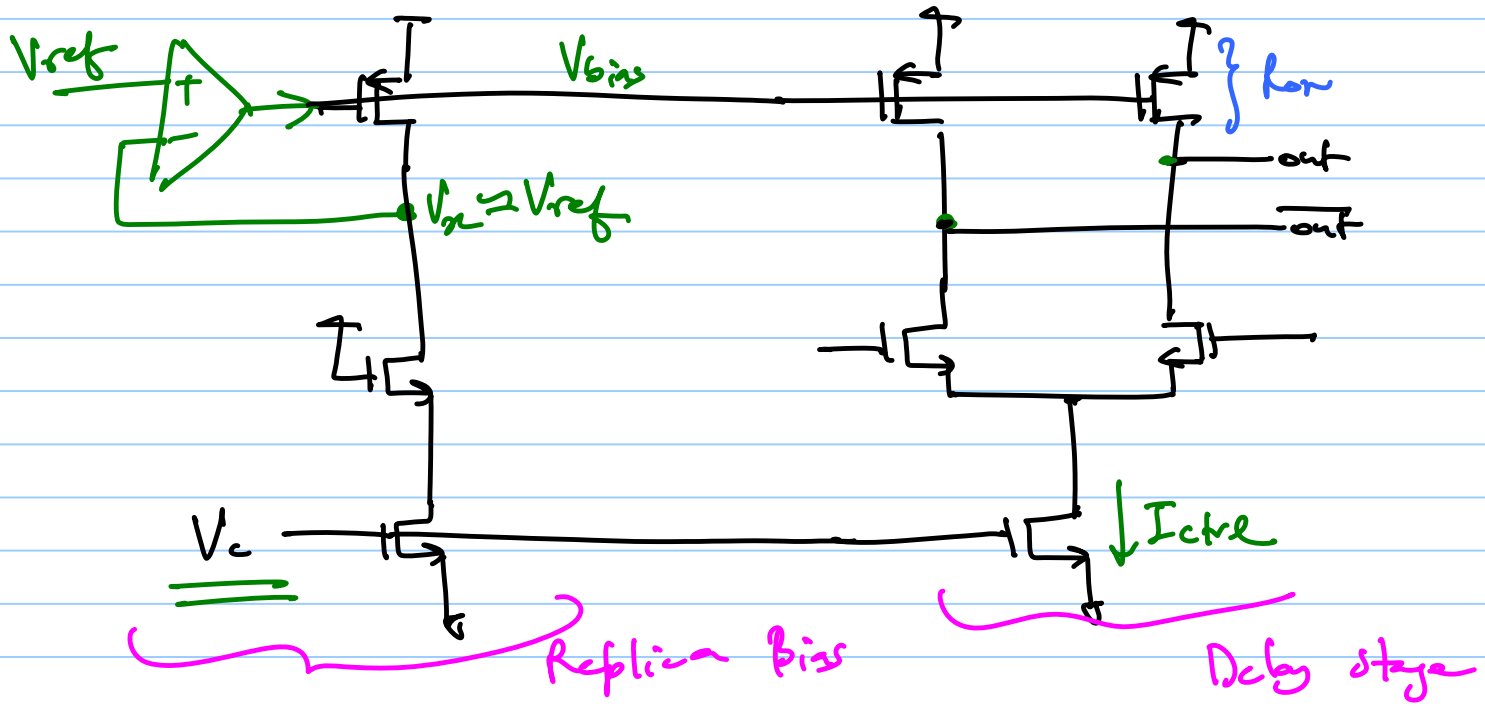
"PSS" analysis in spectreRF

Replica Biasing:

$V_c \rightarrow R_{on}$



* Fix the output CM-level and control the current I_o


Vref
+
−
Vbias
Vx = Vref
Ron
out
out
Vc
↓Ictrl
Replica bias
Delay stage