ECE 504 – Lecture 13

Note Title 10/5/2016

PFD issues

① Dead zone → jitter → t_{RST}

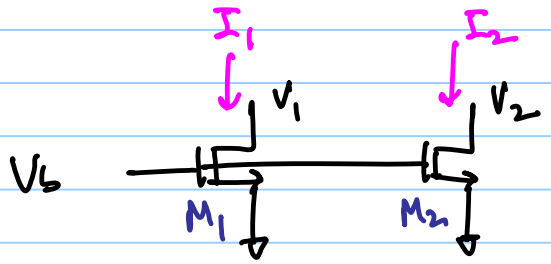
② UP/DN skew → Dummy TG delay

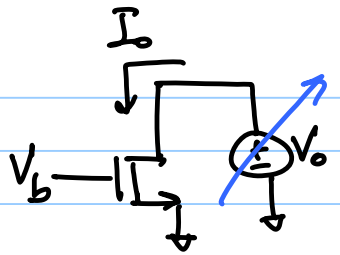
③ Current mismatch →

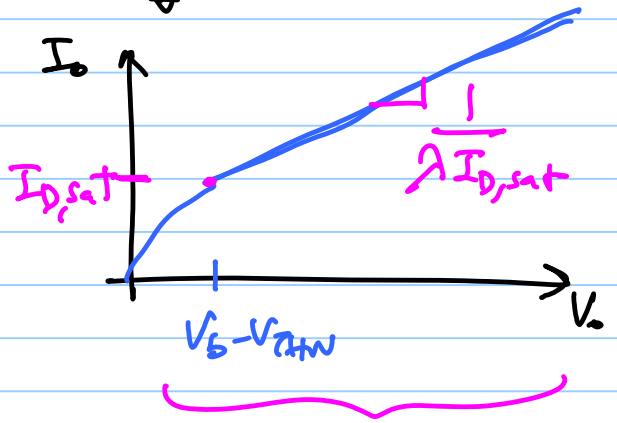
- → static mismatch → I_p & I_n are mismatched
- → dynamic mismatch → current sources turning on & off

④ Charge-sharing

⑤ Channel length Modulation:





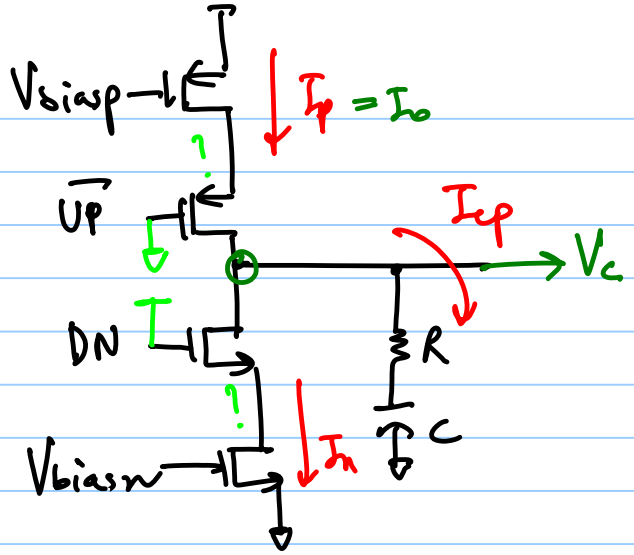


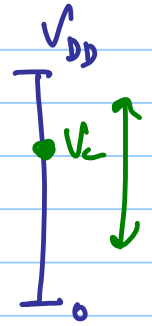
CLM parameter

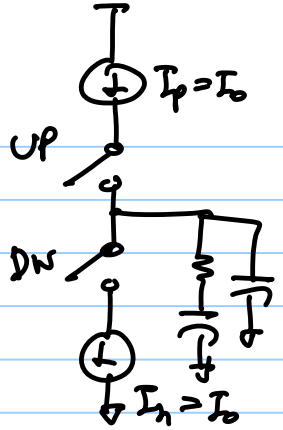
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{THN})^2(1+\lambda V_{DS})$$

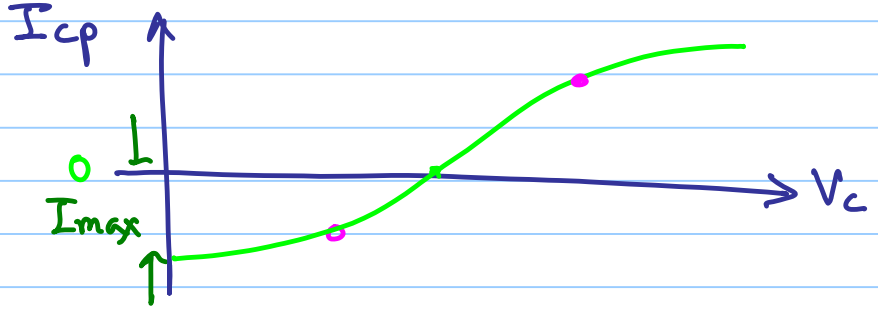
$$\frac{I_2}{I_1} = \frac{(1+\lambda V_2)}{(1+\lambda V_1)}$$

Current mismatch due to Channel length modulation





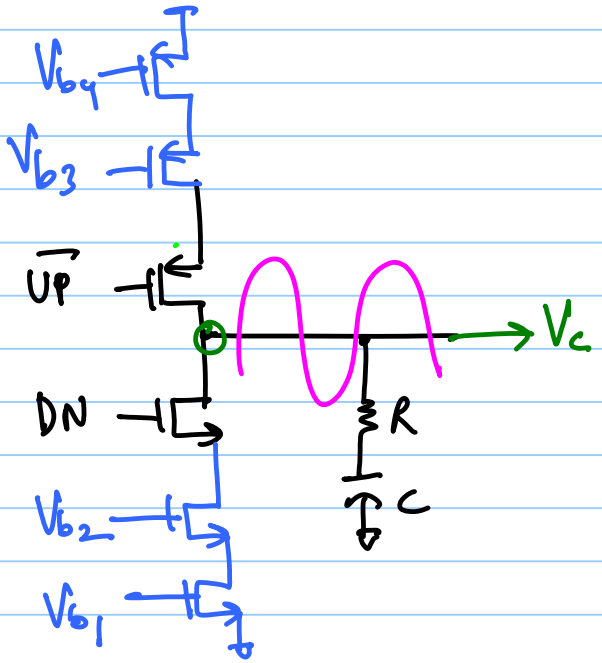


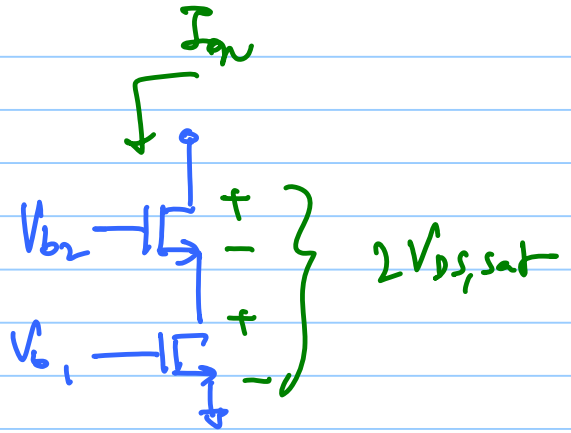


$I_{cp} = I_p - I_n$

$\frac{I_{max}}{I_o} \simeq 35\text{-}48\%$ for a simple current source pair (I_p & I_n)

Cascoded Current Mirror

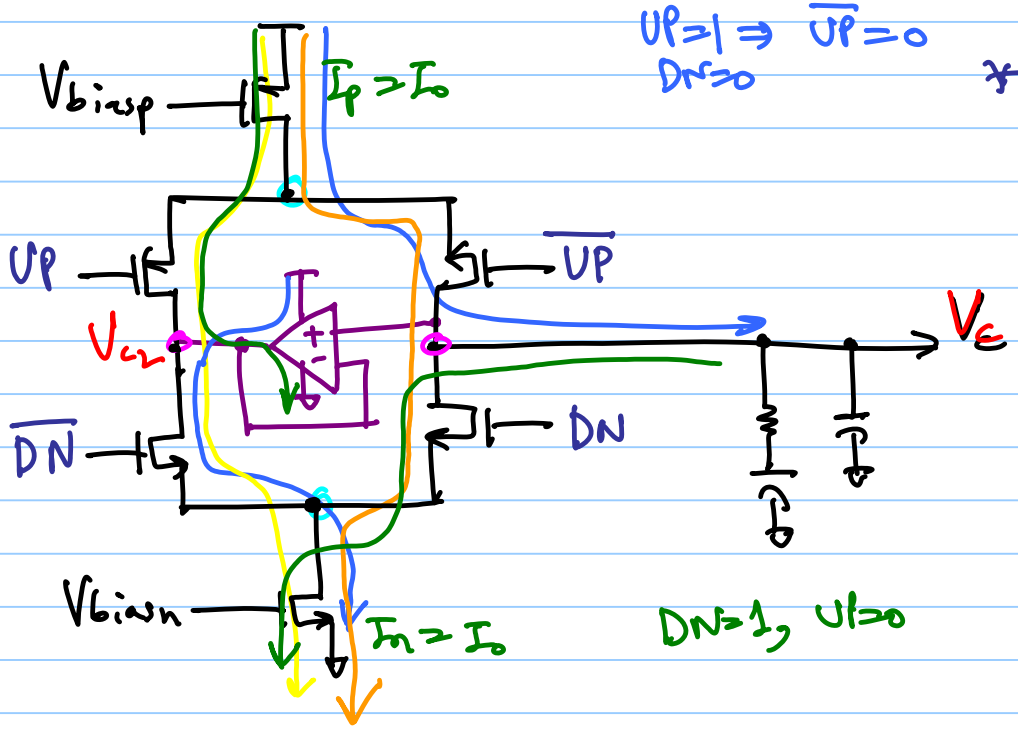




Needs extra Voltage headroom

UP=0, DN=0

UP=1 & DN=1

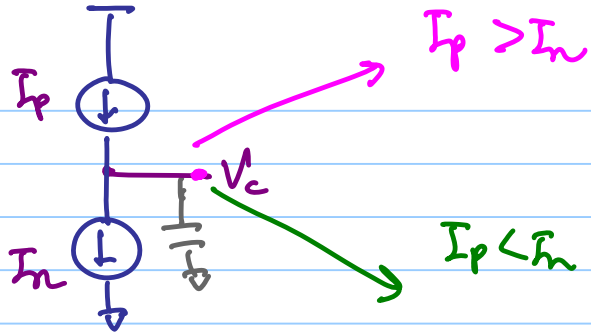


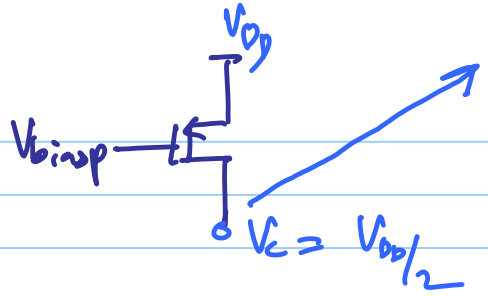
UP=1 ⇒ $\overline{UP}$=0
DN=0

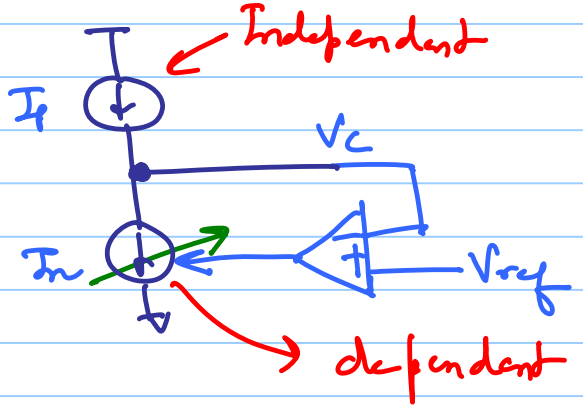
DN=1, UP=0

* Differential Current Steering topology

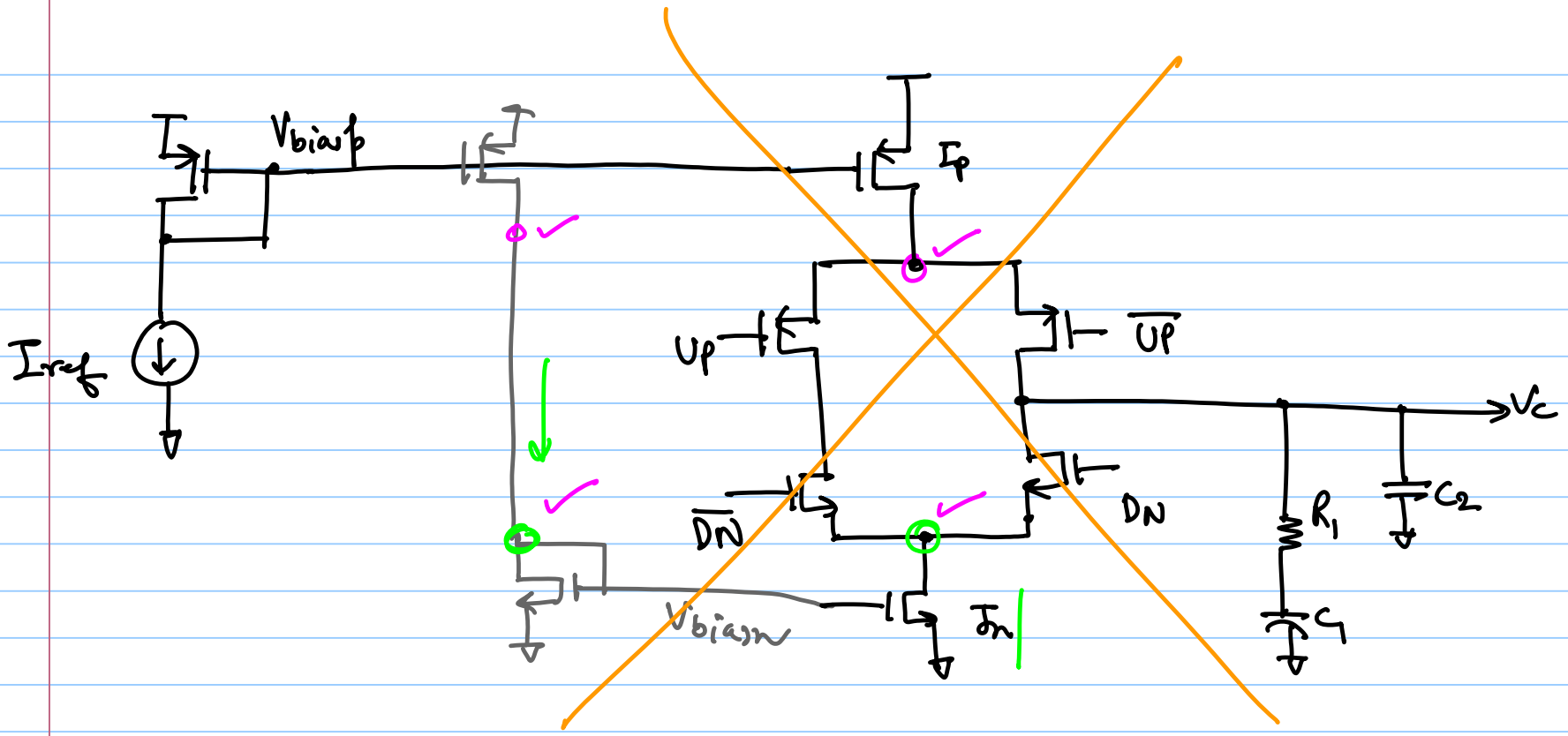
* Keep V_2 to track V_c
  ↳ keeps V_{ds} of the current sources constant
  ↳ reduced transient mismatch



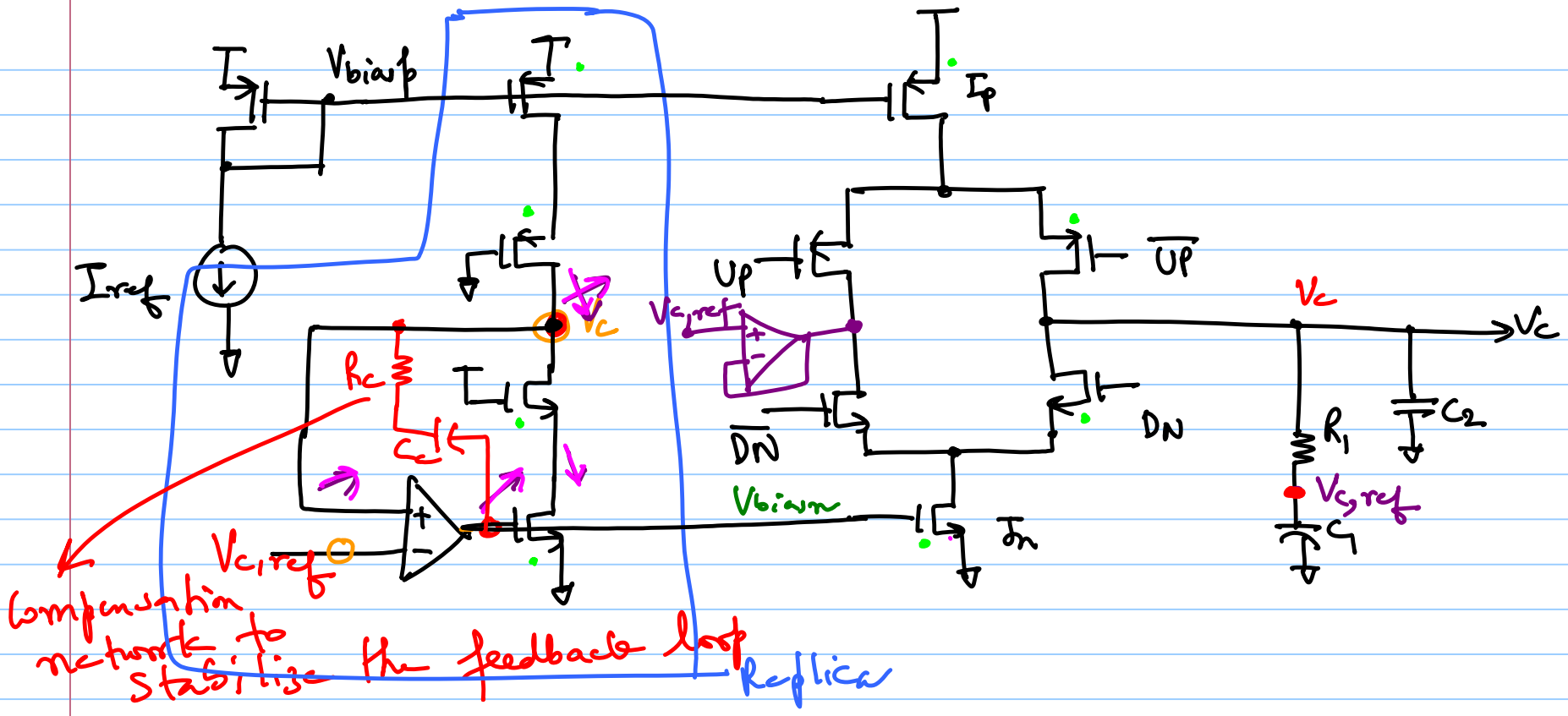




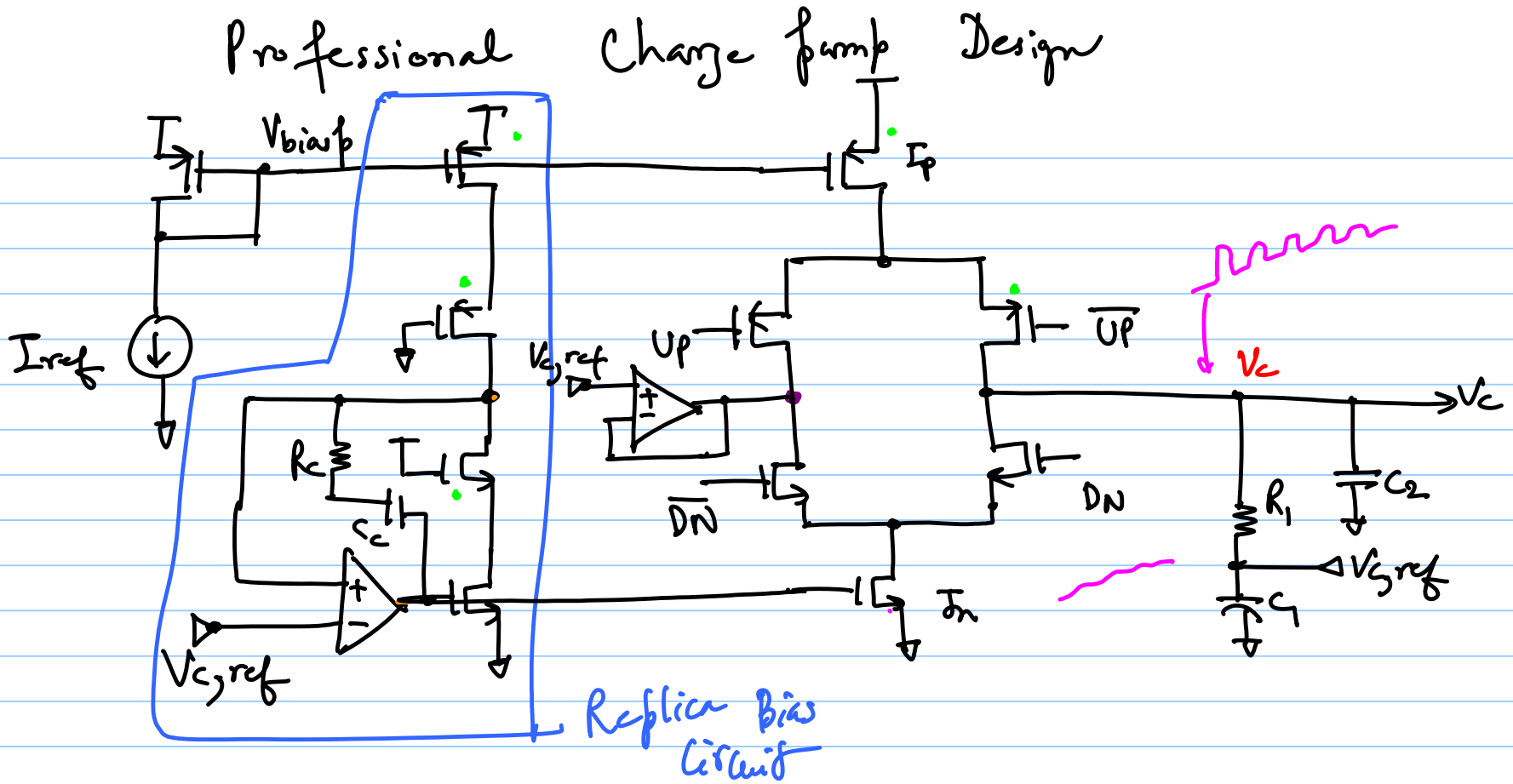
Solution → Make one current source dependent upon another


Vbiasp
Iref
Ip
Up
UP
Vc
DN
DN
R1
C2
C1
Vbiasn
In

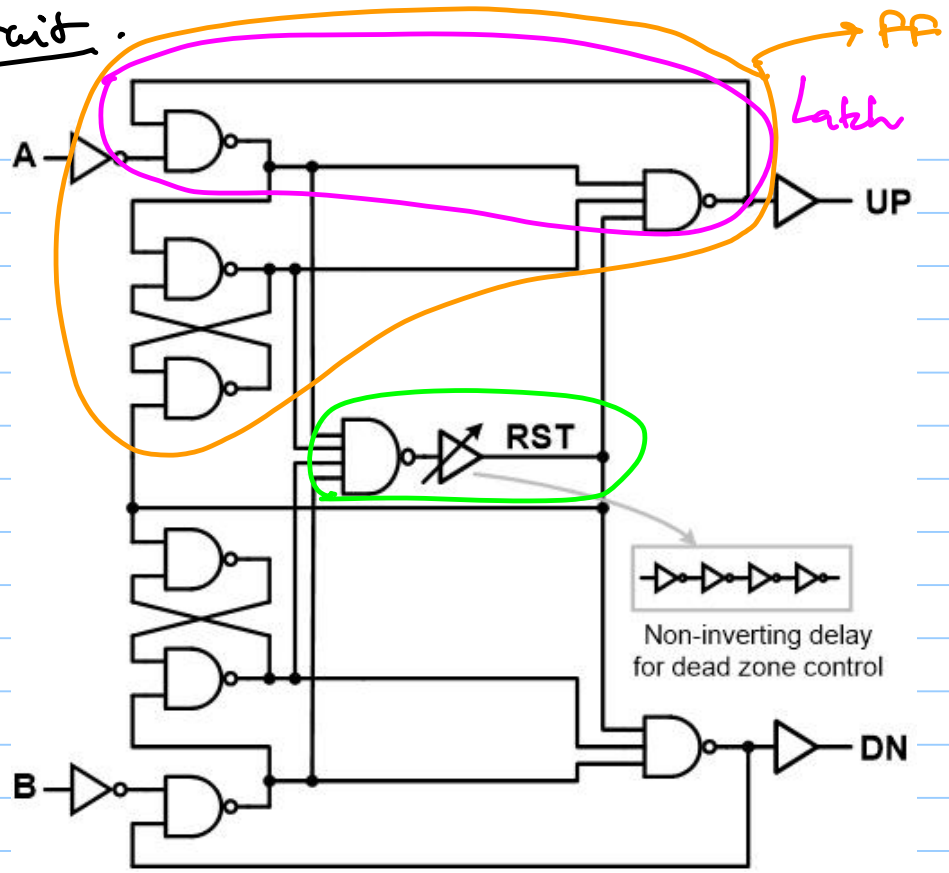
Replica Bias Scheme

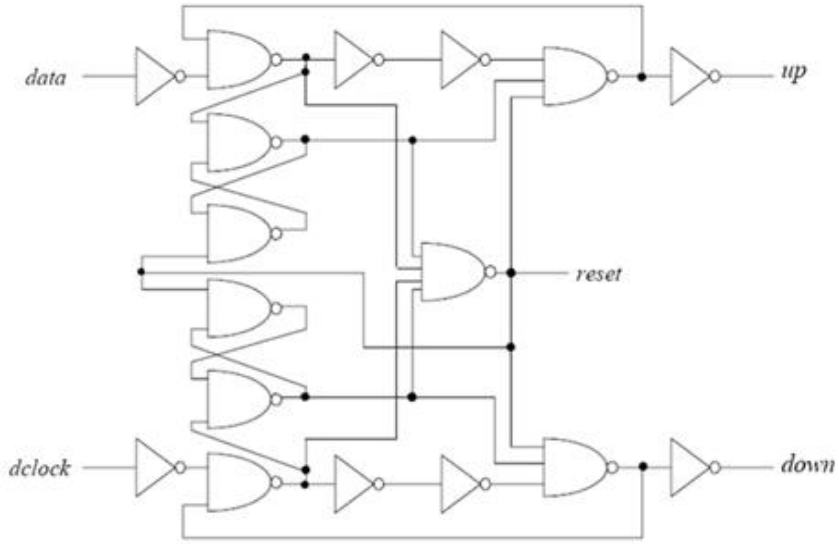


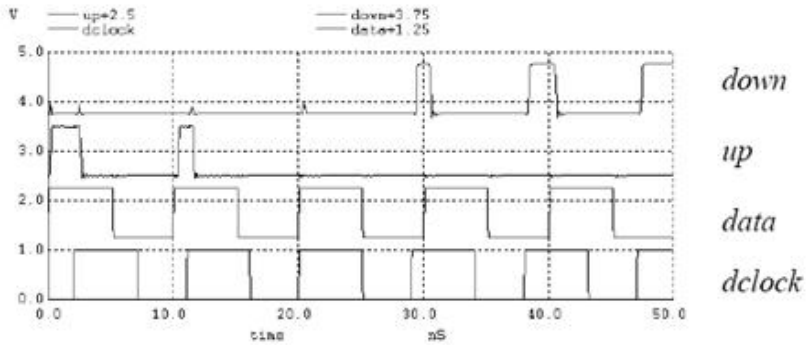
Professional Charge pump Design



PFD Circuit.


FF
Latch
A
UP
RST
Non-inverting delay
for dead zone control
DN
B


data
up
reset
dclock
down


V
up+2.5
dclock
down+3.75
data+1.25
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
time
nS
down
up
data
dclock