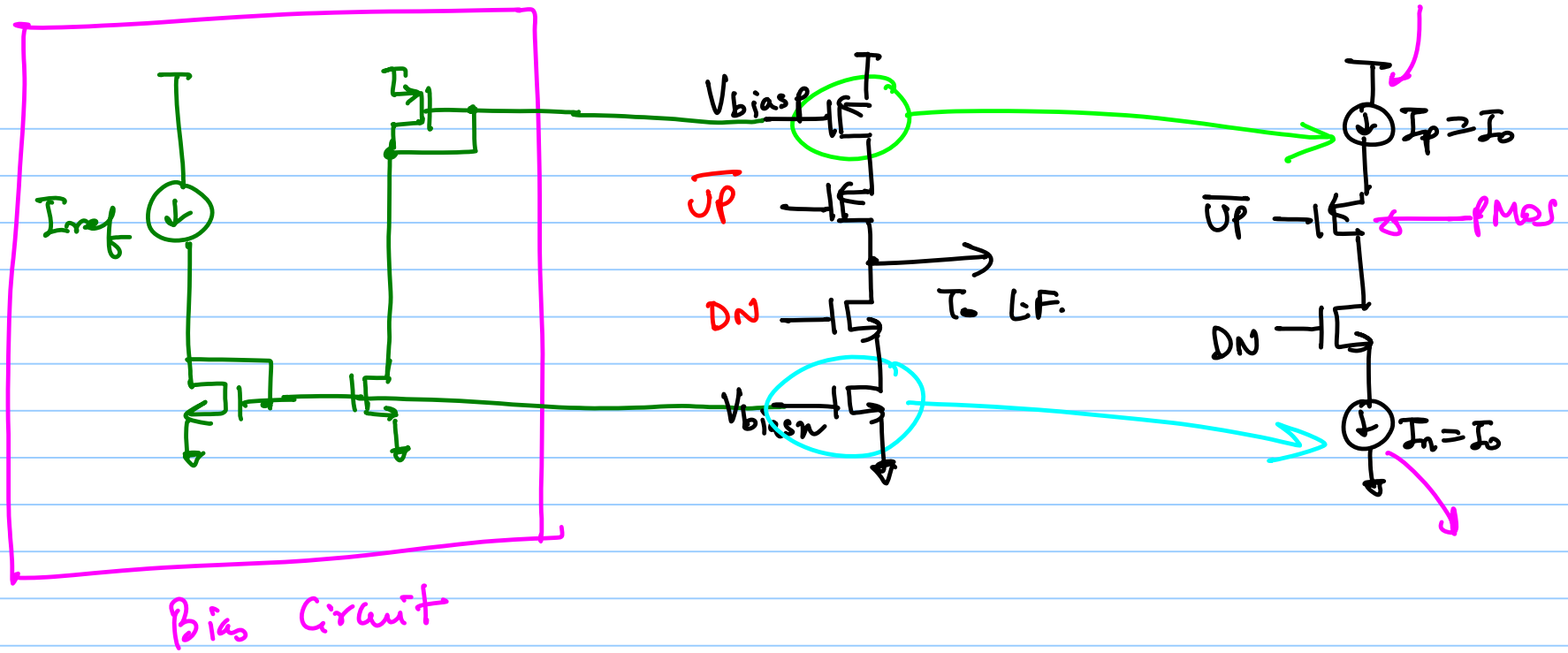
ECE 504 - Lecture 12

Note Title 10/3/2016

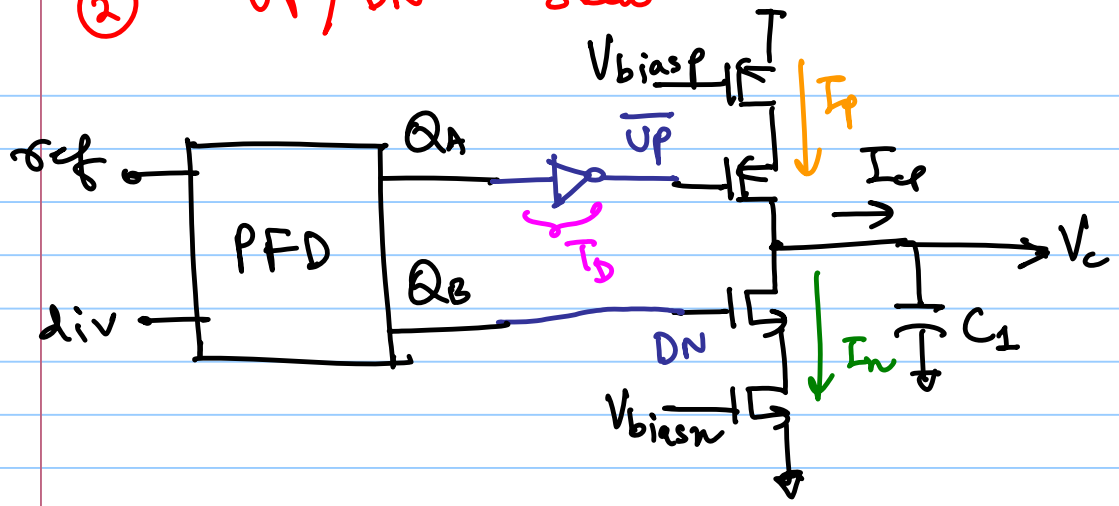
① PFD Dead zone

* Dead zone in the PFD/CP

↳ enforce minimum reset pulse width (T_{rst})

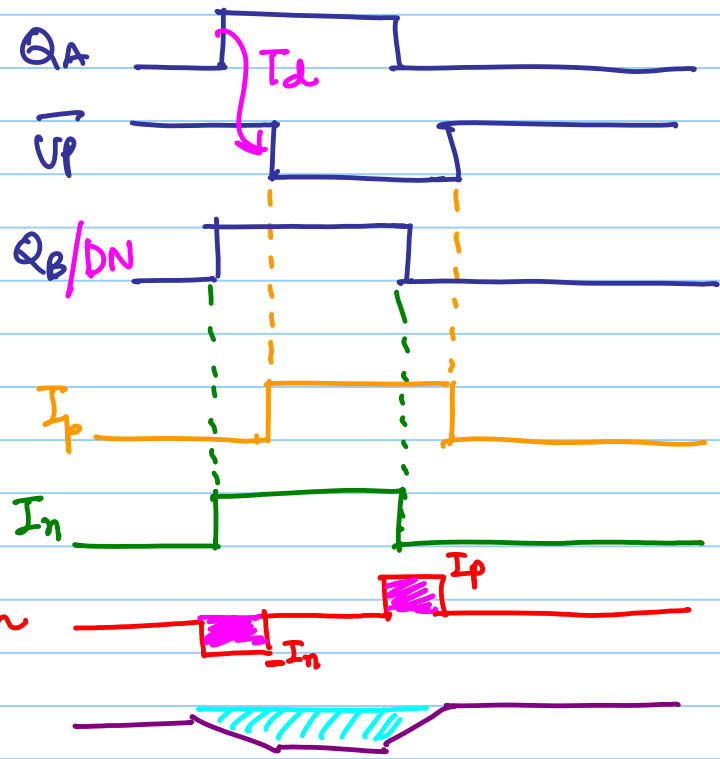

Iref
Vbiasp
UP
DN
Vbiasn
To L.F.
Ip = Io
UP
PMOS
DN
In = Io
Bias Circuit

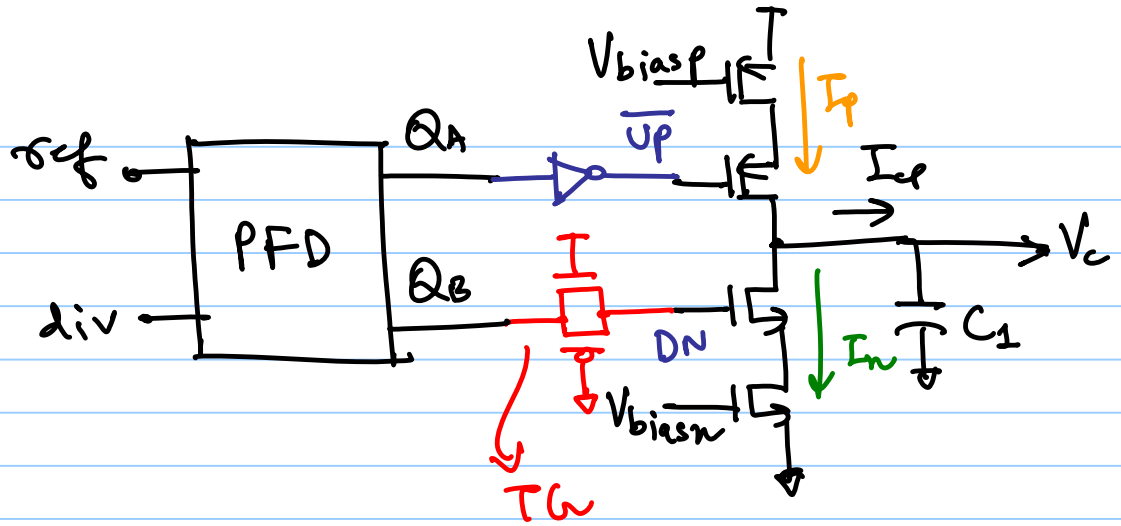
② UP / DN Skew



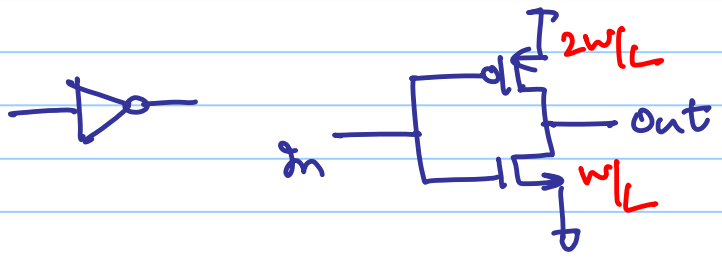
mismatch causes current injection
↳ more periodic disturbance

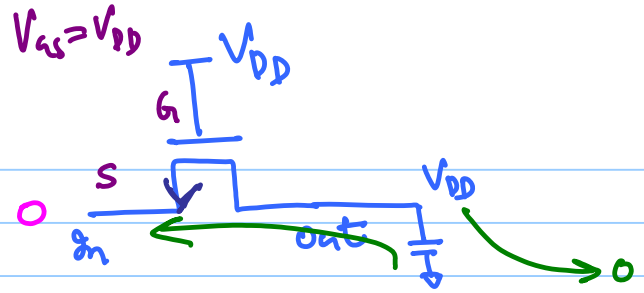
$\Delta\varphi = 0$ (steady-state)

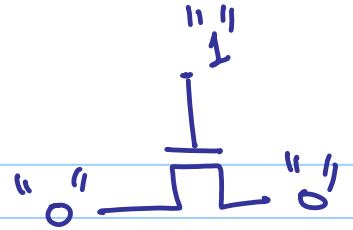


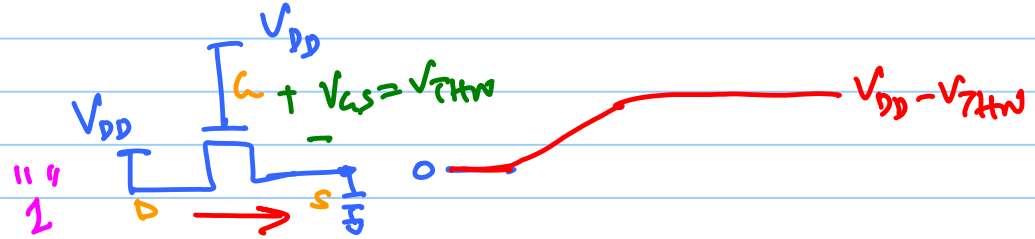


fix- Equalize the delay in UP & DN paths

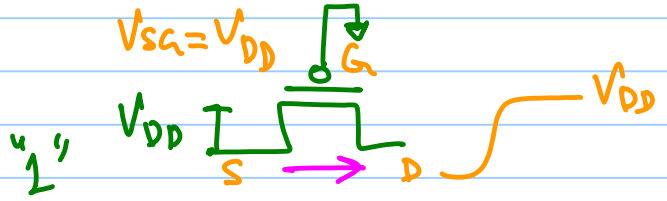


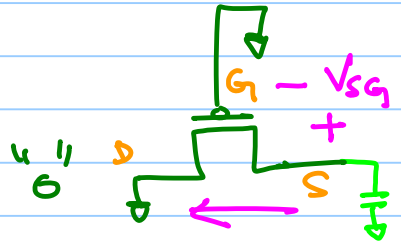




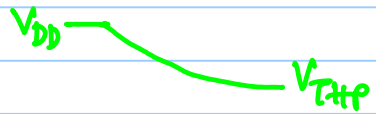


NMOS doesn't pass "1"

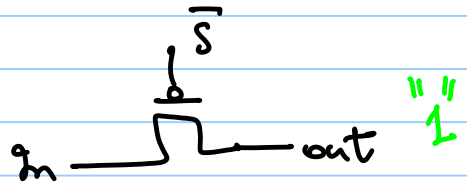




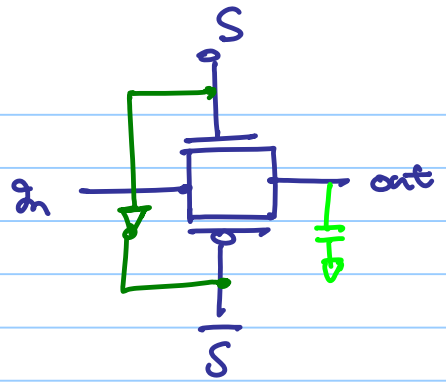
PMOS doesn't pass "0"



"0"

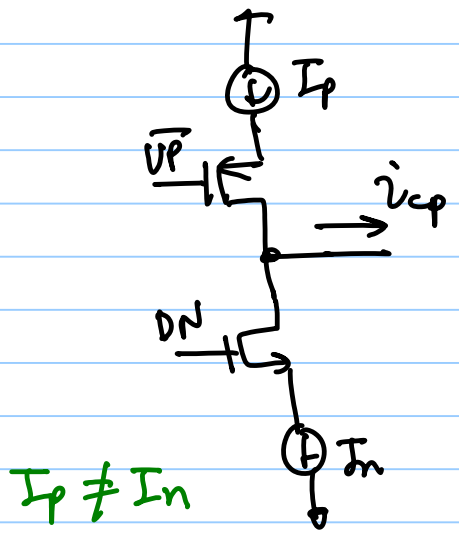


"1"

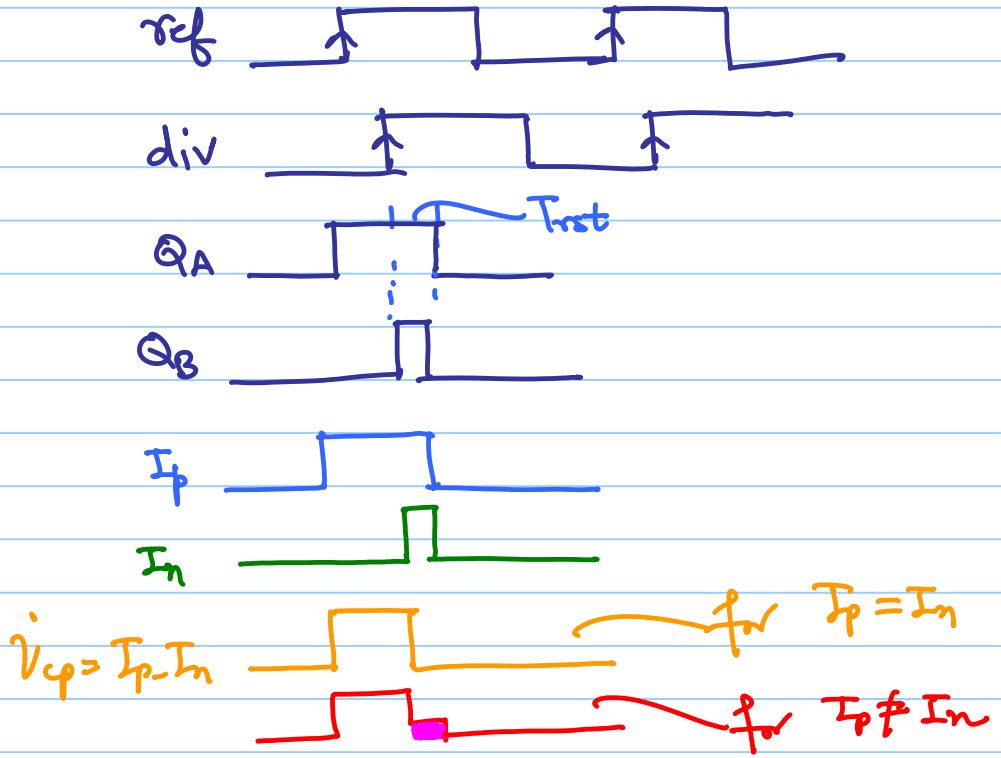


Transmission Gate
"TG"

③ I_p & I_n mismatch



$I_p \neq I_n$

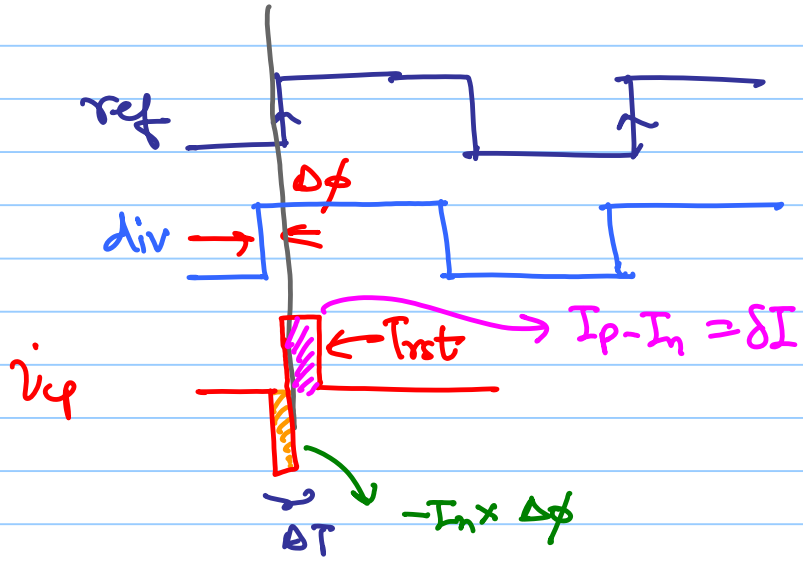


As a result in the steady-state (in closed-loop)

$$T_{rst}\left(I_p - I_n\right) = \Delta T \cdot I_n$$

$$\Delta T = T_{rst}\left(\frac{\delta I}{I_o}\right)$$

$$\Delta\phi = \frac{T_{rst}}{2\pi}\left(\frac{\delta I}{I_o}\right)$$

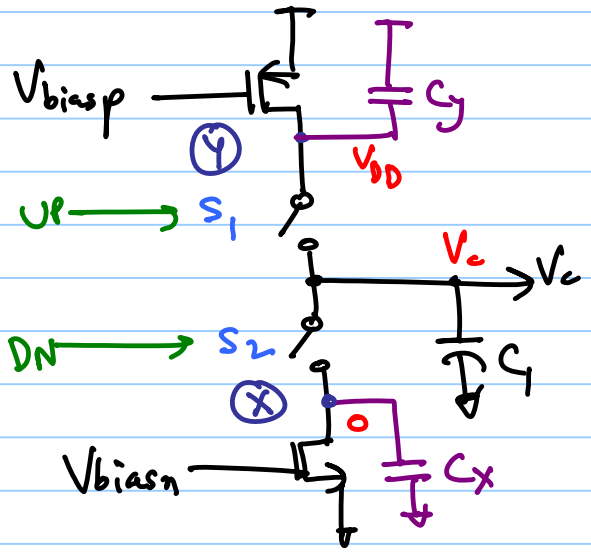


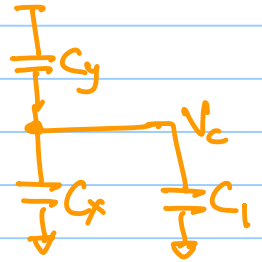
* Current mismatch leads to static phase error proportional to the mismatch.

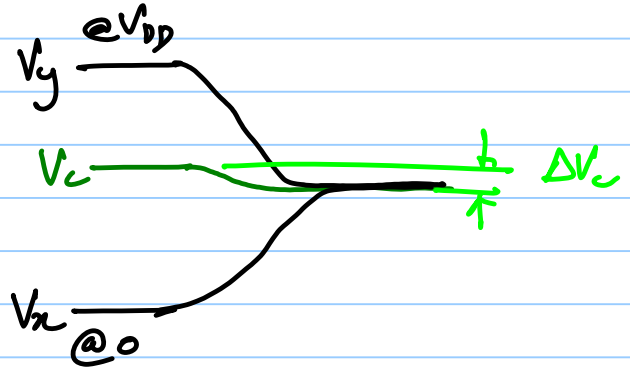
④ Charge Sharing !

Ⓐ Initially S_1 & S_2 are off (open)
$V_x = 0$, $V_y = V_{DD}$

Ⓑ Switches S_1 & S_2 turn on

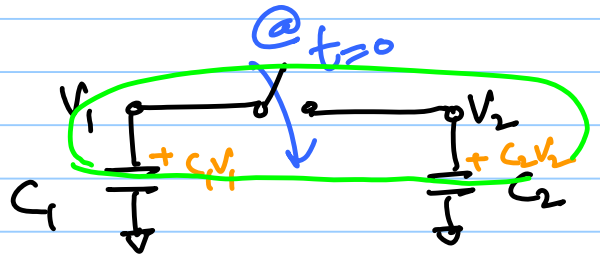


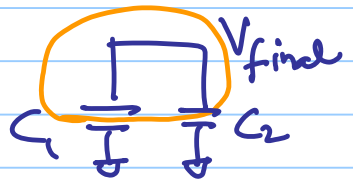


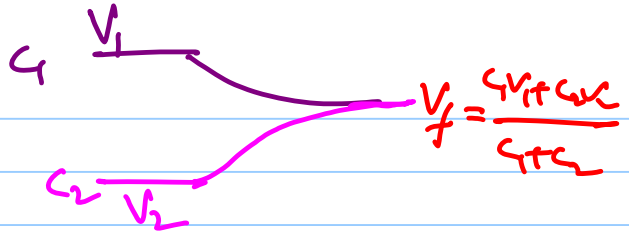


charge sharing between C_x, C_y & C_L

Aside: charge sharing







V_{final}

$C_1V_1 + C_2V_2 = (C_1+C_2)V_f$

$V_f = \frac{C_1V_1 + C_2V_2}{C_1 + C_2}$ ← weighted avg.

for $\Delta\phi = 0 \Rightarrow$ V_c should be constant in steady-state

↳ corresponds to the output frequency of the PLL/VCO

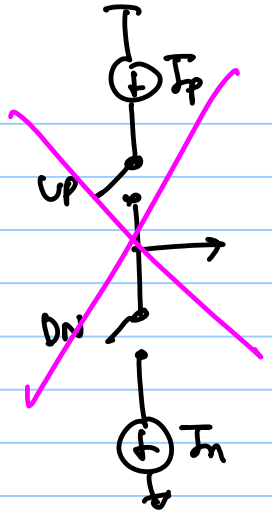
$$V_{c_{final}} = \frac{C_x V_x + C_y V_y + C V_{c_{initial}}}{C_x + C_y + C}$$

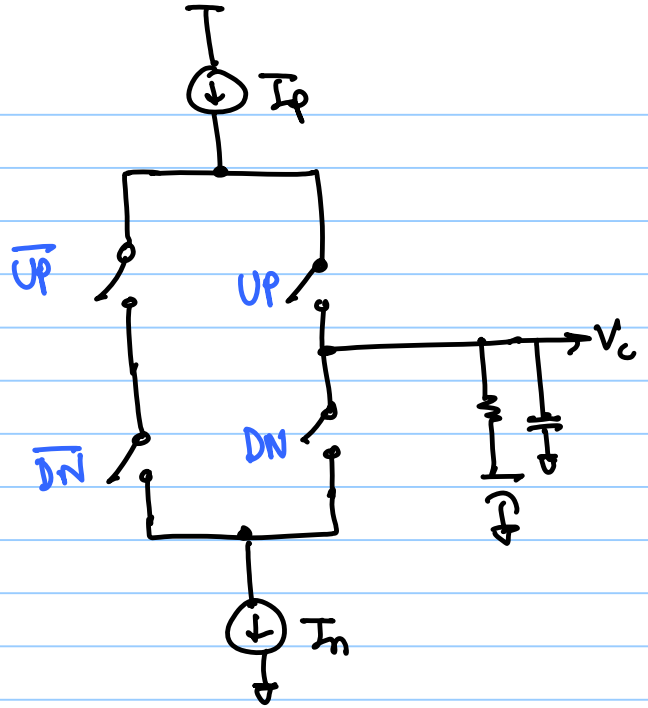
↳ V_c jumps ⇒ periodic disturbance

↳ jitter

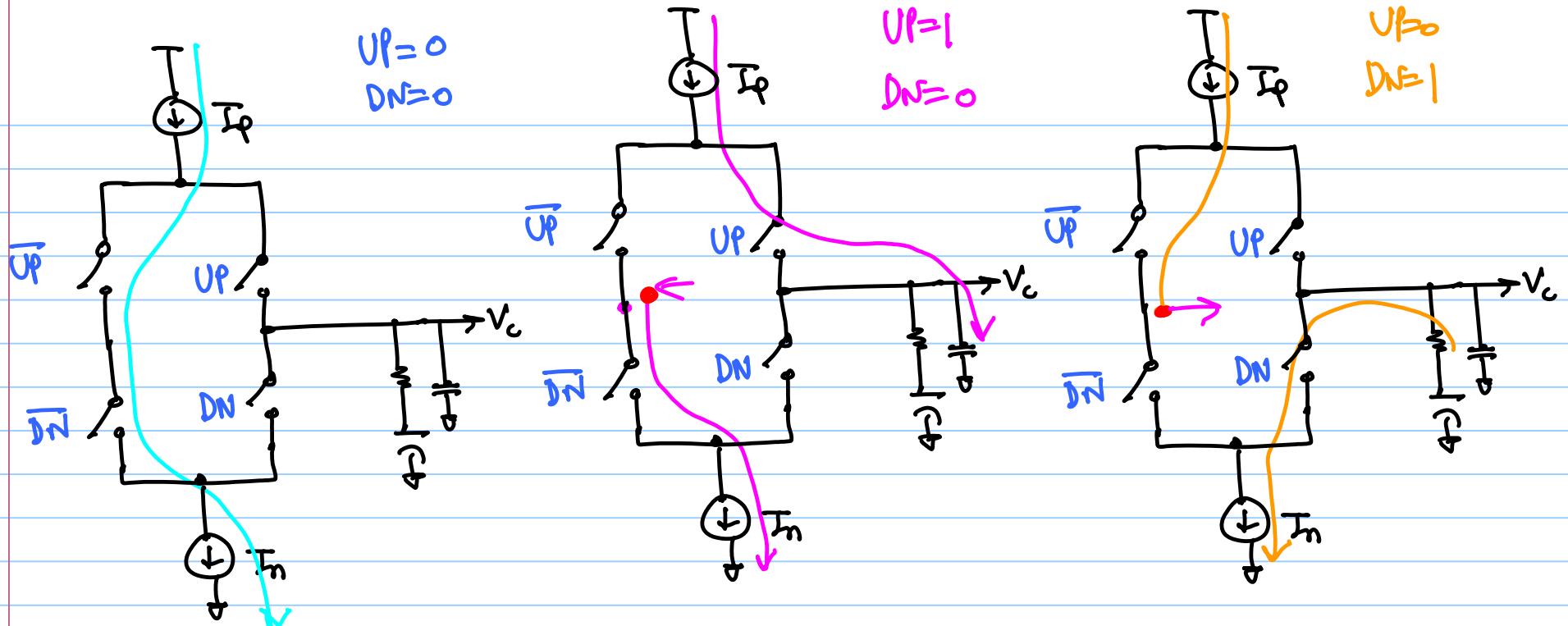
* This disturbance is frequency dependent

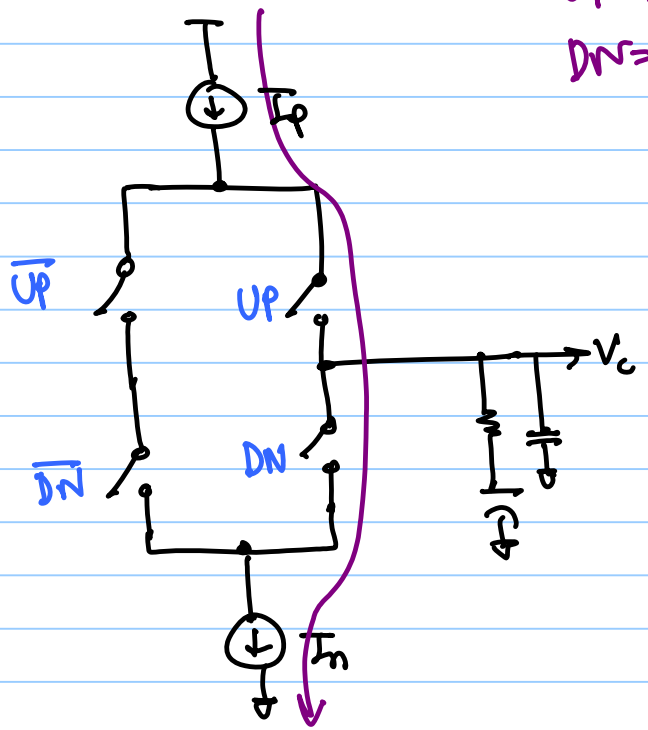
"Big problem!"

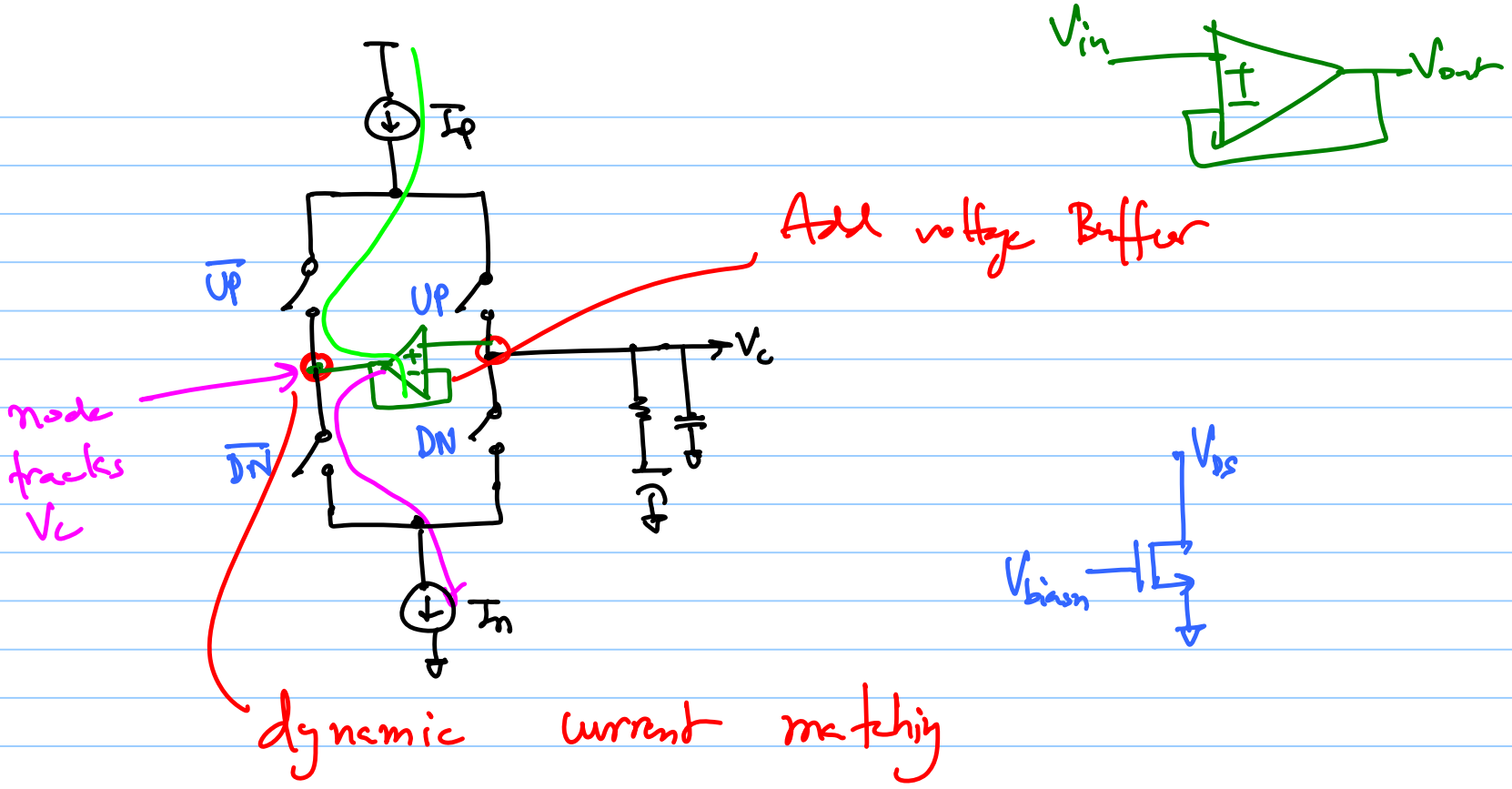




Differential Current Steering Topology


UP=0
DN=0
I_p
$\overline{UP}$
UP
V_c
$\overline{DN}$
DN
I_n
UP=1
DN=0
I_p
$\overline{UP}$
UP
V_c
$\overline{DN}$
DN
I_n
UP=0
DN=1
I_p
$\overline{UP}$
UP
V_c
$\overline{DN}$
DN
I_n


UP=1
DN=1
I_p
$\overline{UP}$
UP
V_c
DN
$\overline{DN}$
C
I_n


I_p
$\overline{UP}$
UP
V_c
node tracks V_c
$\overline{DN}$
DN
I_n
Add voltage Buffer
dynamic current matching
V_{in}
V_{out}
V_{DS}
V_{biasn}