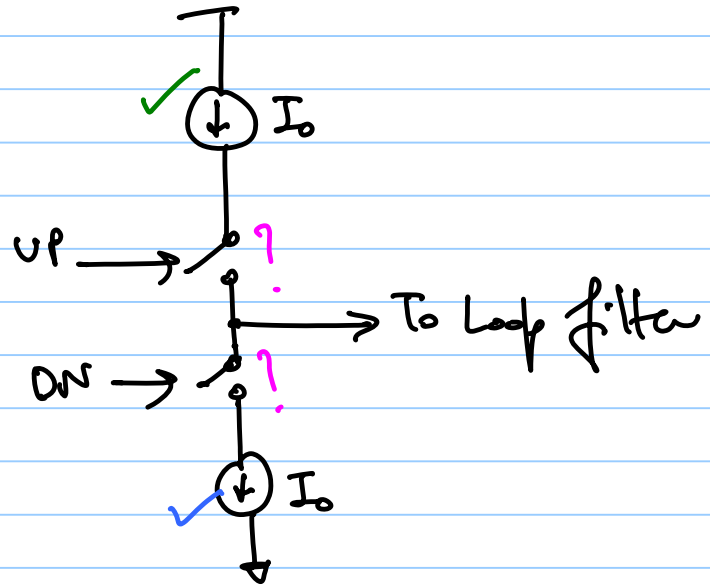
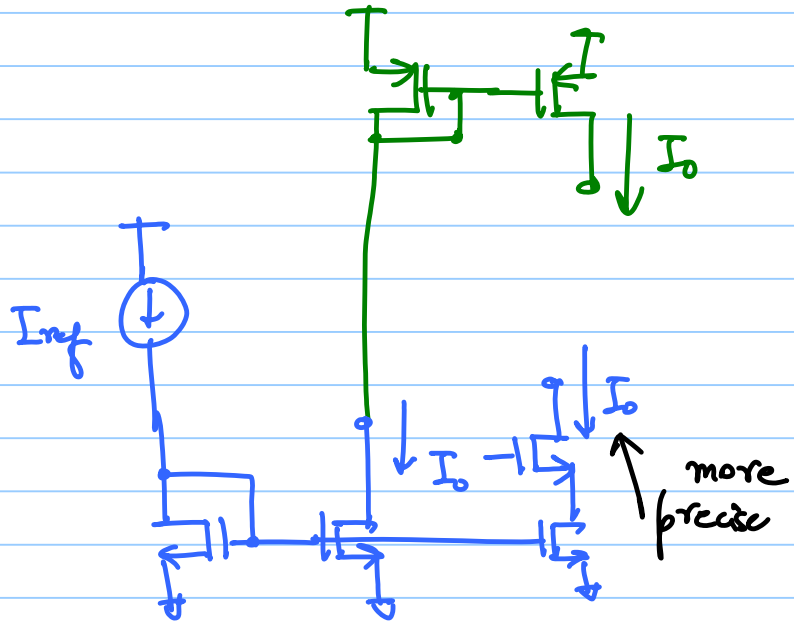
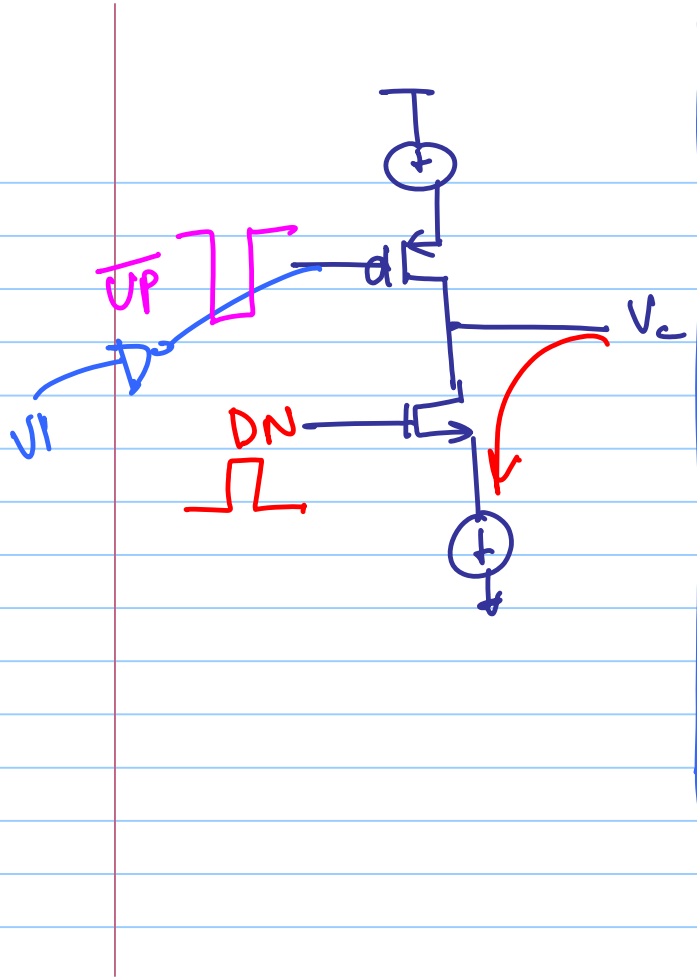
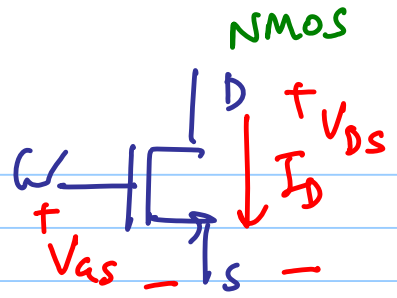
ECE 504- Lecture 11

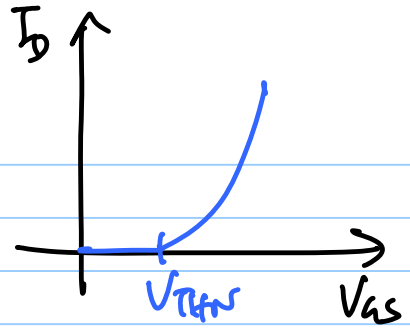
Note Title 9/28/2016

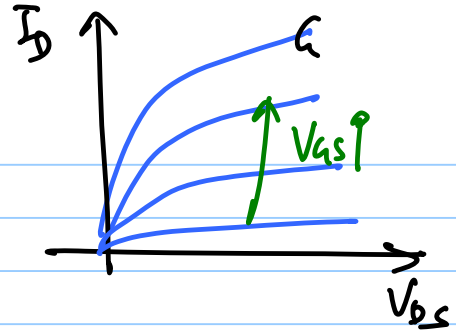


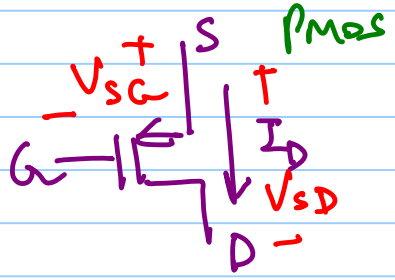


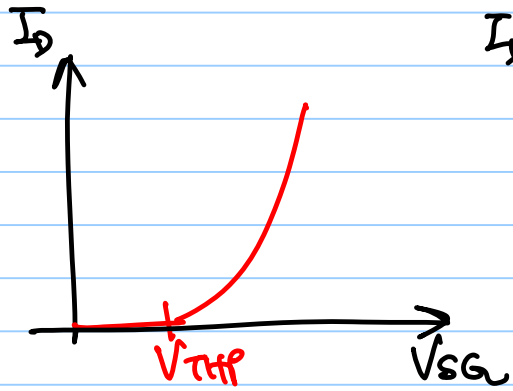

UP
DN
Vc
Vi

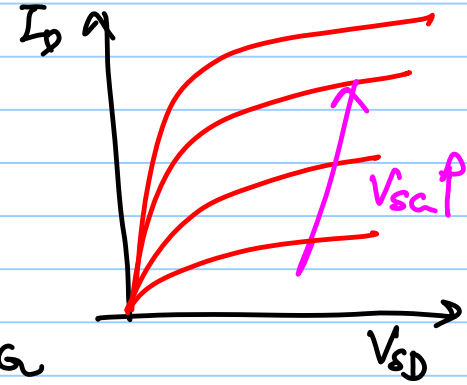

NMOS
D
+
VDS
ID
G
+
VGS
−
S
−

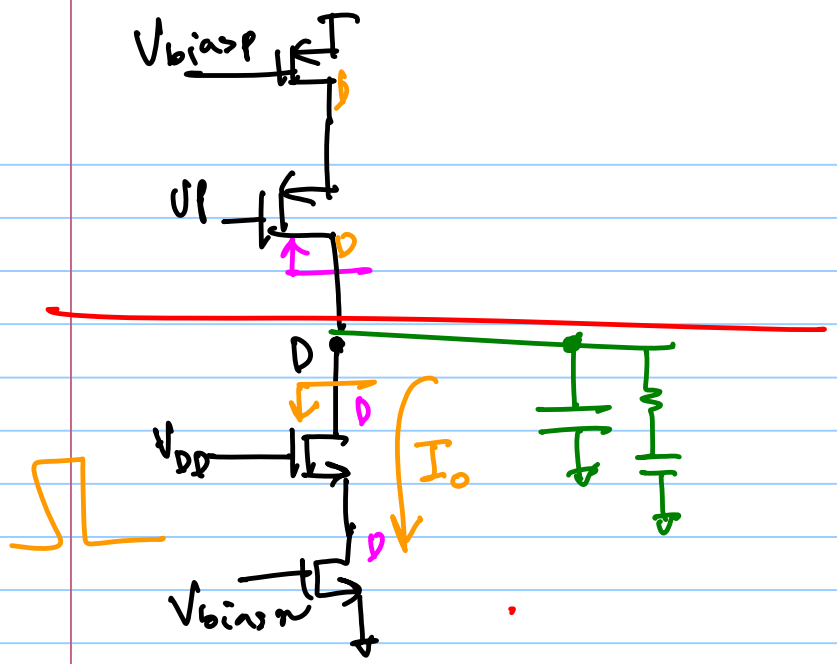

ID
VTHN
VGS

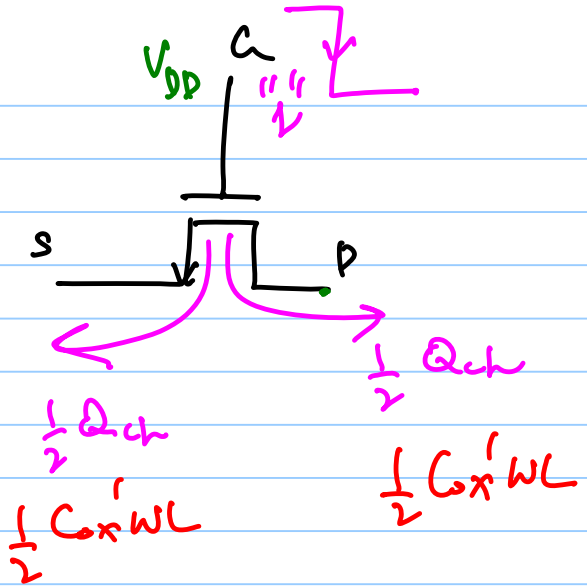

ID
VGS↑
VDS


PMOS
S
+
VSG
−
G
+
ID
VSD
D
−

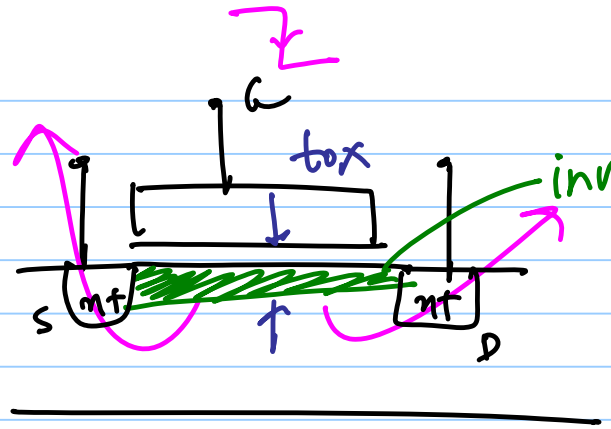

ID
VTHP
VSG


ID
VSG↑
VSD


Vbiasp
Vl
D
D
D
VDD
Io
D
Vbiasn

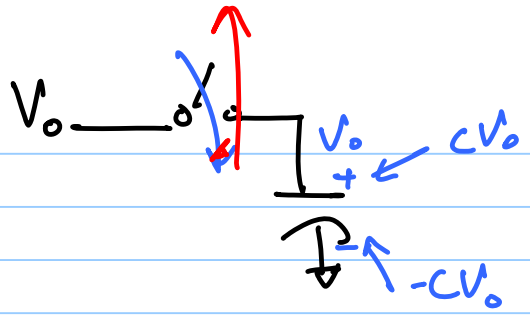


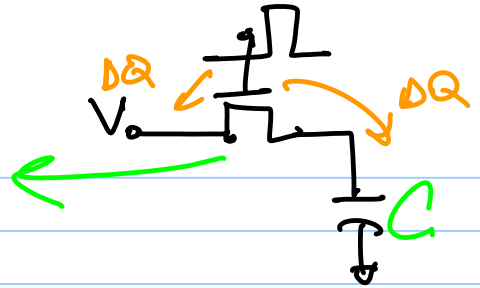
"Charge injection"

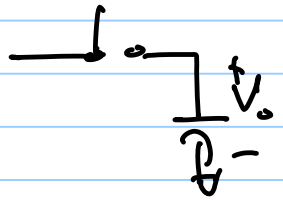


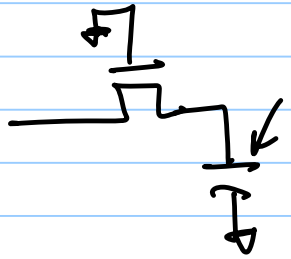
$Q_{ch} = C_{ox}'WL$

$\hookrightarrow \frac{\varepsilon_0 \varepsilon_{oxide}}{t_{ox}}$





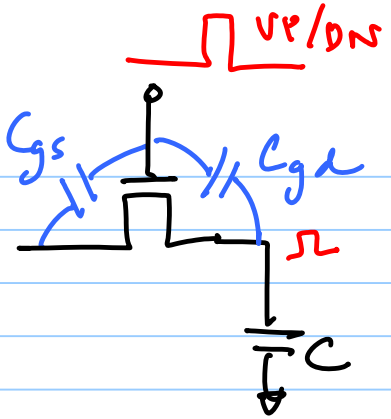




$$Q = cV_o - \frac{1}{2} C_{ox}' WL$$

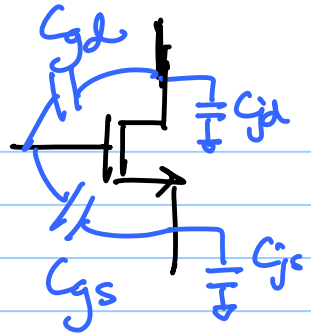
$$V_{final} = \frac{Q}{C} = V_o - \frac{\frac{1}{2} C_{ox}' WL}{C}$$

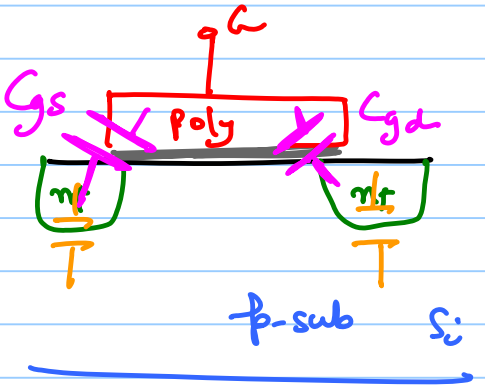
switched-capacitor circuits

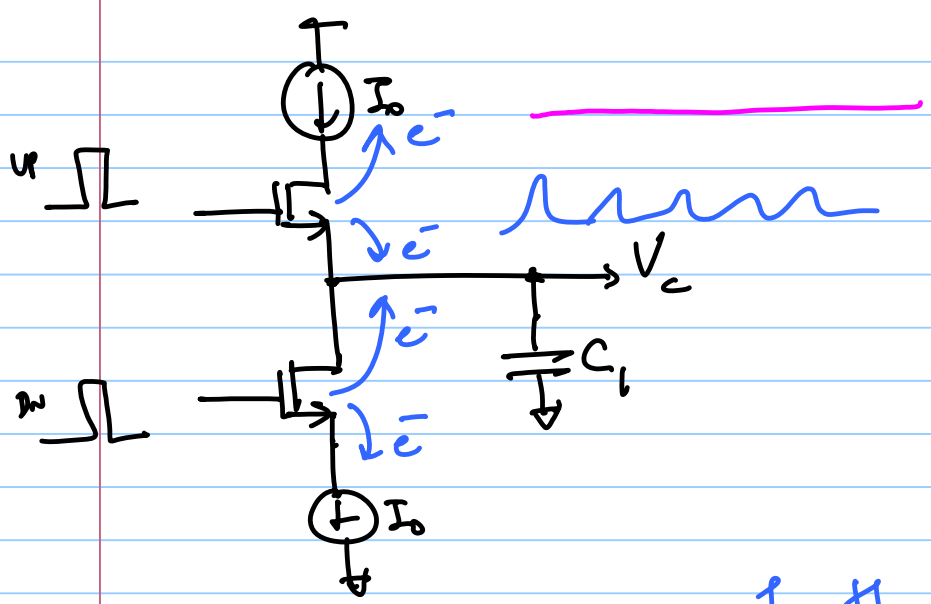


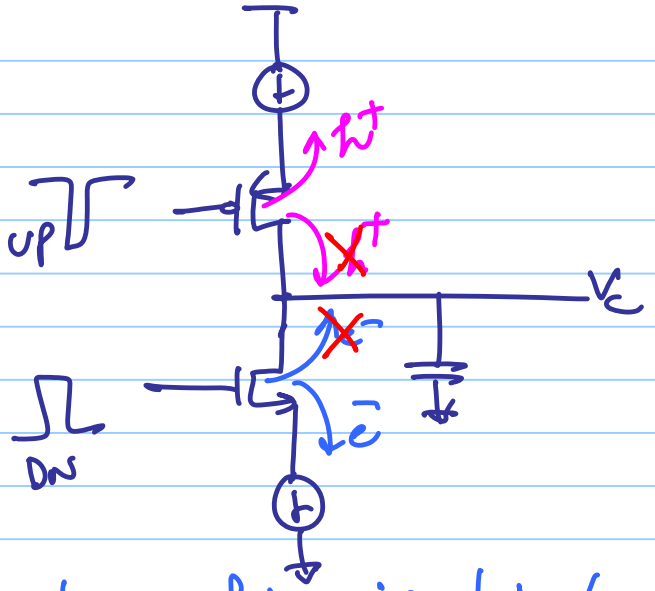
Clock feedthrough

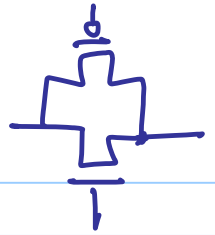
parasitic capacitances





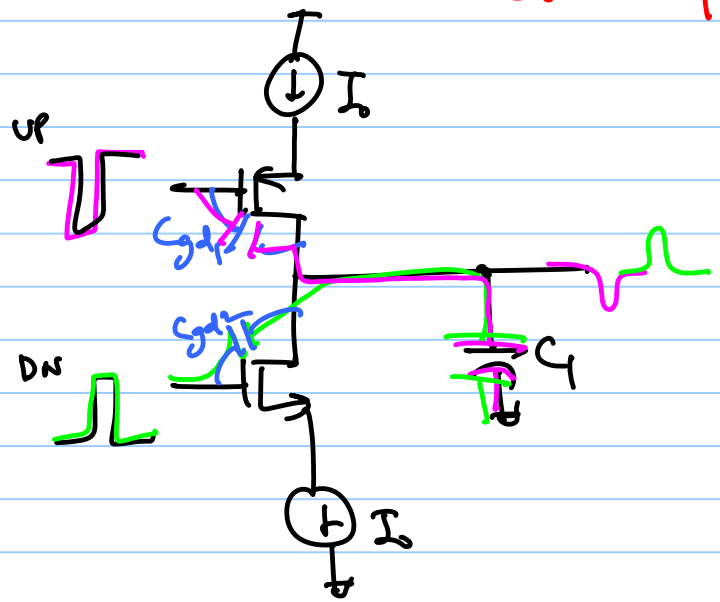


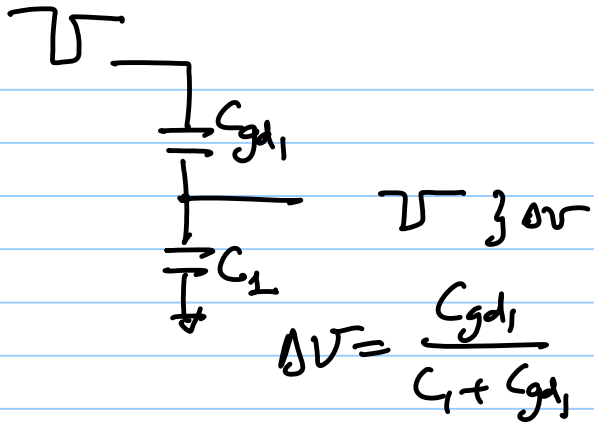




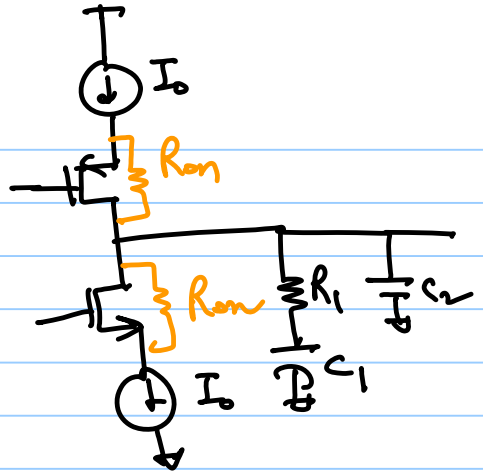
* if the # of holes injected ≠ # of e^-s injected
  ↳ V_c is disturbed

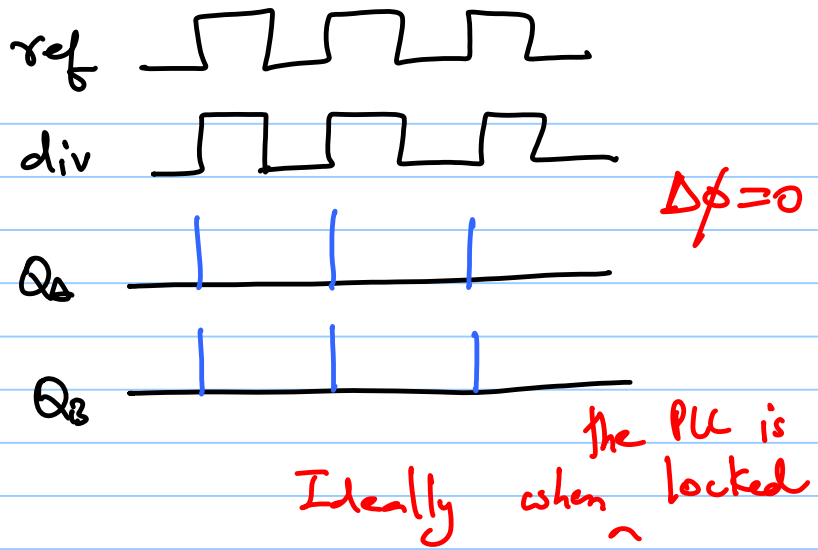
clock-feedthrow



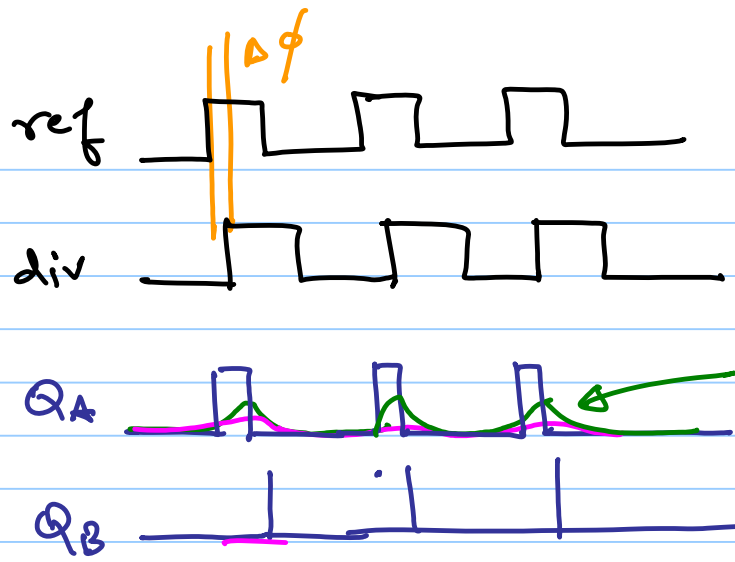


* clock feedthrow: UP & DN pulses couple through C_{gd_1} & C_{gd_2} respectively and reach V_c





Ideally when the PLL is locked



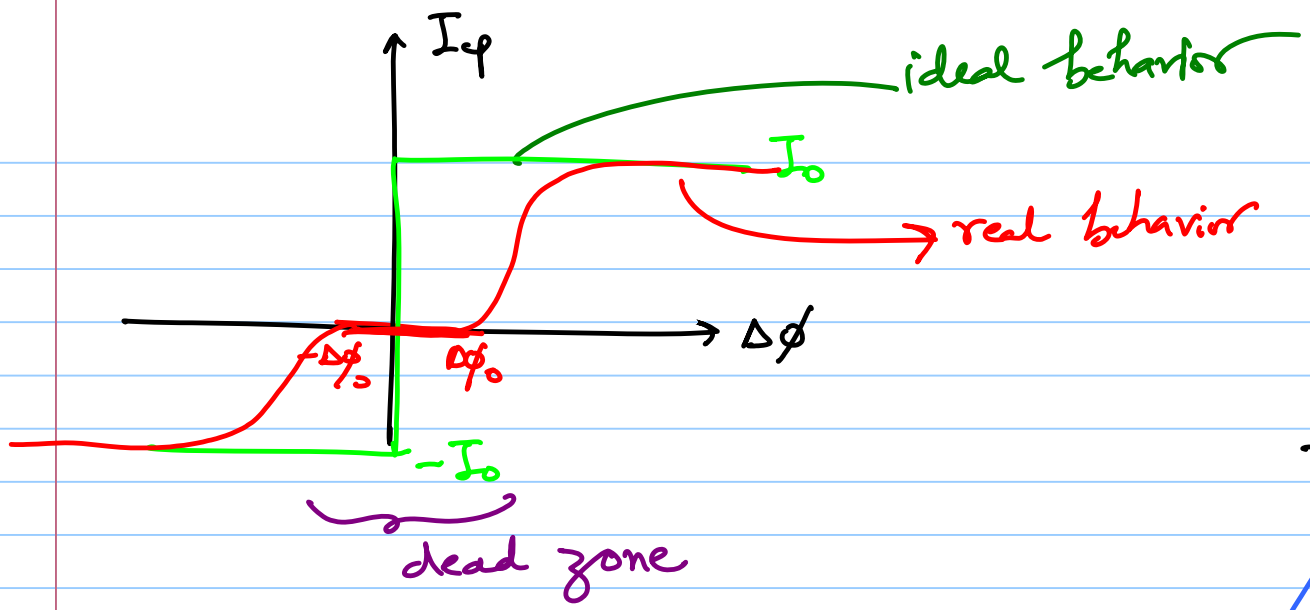
$\Delta\phi > 0$, small value

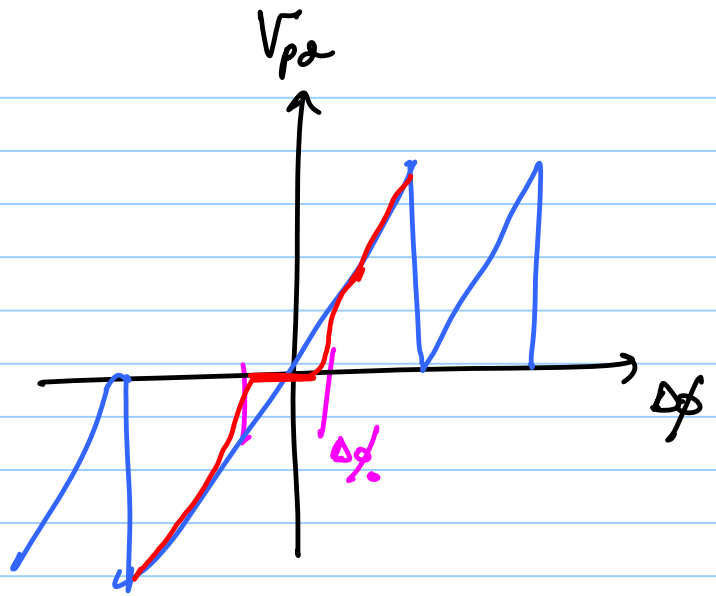
limited Rc time constants

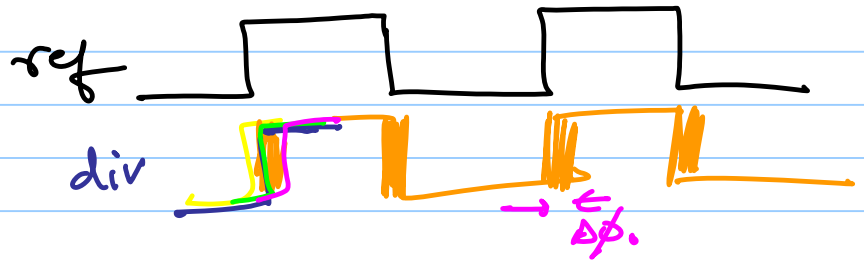
due to charging & discharging of the caps ← caps of the switch

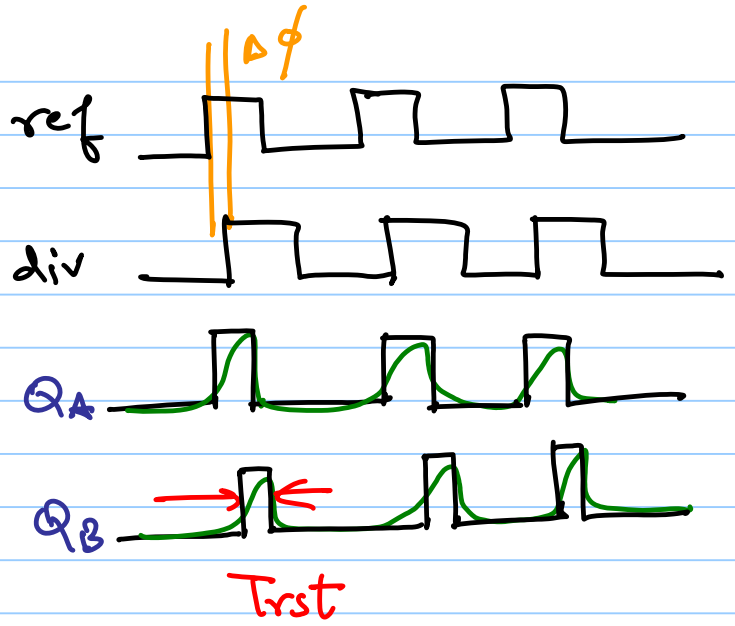
for small $\Delta\phi$ ⇒ the charge pump switches fail to turn on

⇒ $I_{cp} = 0$ for some $\Delta\phi < \Delta\phi_0$


I_{cp}
ideal behavior
I_0
real behavior
$\Delta\phi$
$-\Delta\phi_0$
$\Delta\phi_0$
$-I_0$
dead zone


V_{pd}
$\Delta\phi$
$\Delta\phi_0$


ref
div
$\Delta\phi_0$



Enforce a finite reset pulse width (Trst)

* PFD/CP suffers from a dead zone around zero & equal to $\pm \Delta\phi_0$

↳ dead zone allows the VCO to accumulate as much phase error as $\Delta\phi_0$, as there is no corrective feedback. → Jitter

* But if we use coincident pulses on Q_A & Q_B, we can eliminate the dead zone