ECE518 Memory/Clock Synchronization IC Design

Integer-N Frequency Synthesizers

Dr. Vishal Saxena

Electrical and Computer Engineering Department
Boise State University, Boise, ID

Outline

Basic Synthesizer

- ✓ Settling Behavior
- ✓ Spur Reduction Techniques

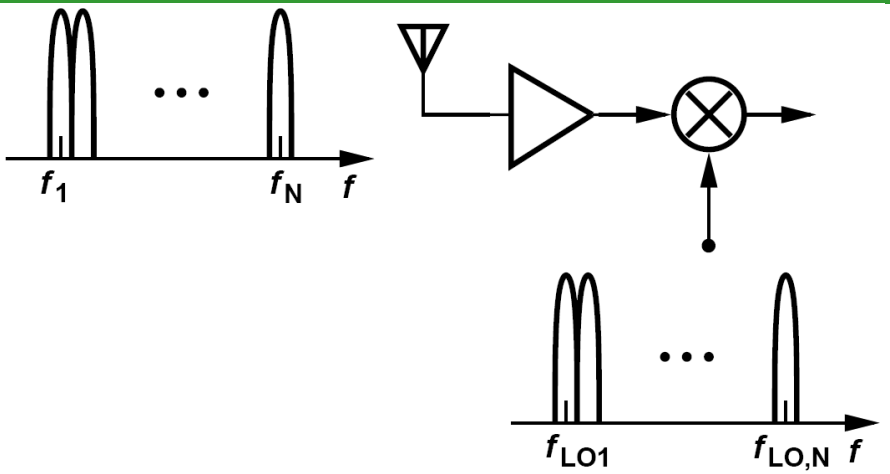
PLL-Based Modulation

- ✓ In-Loop Modulation
- ✓ Offset-PLL TX

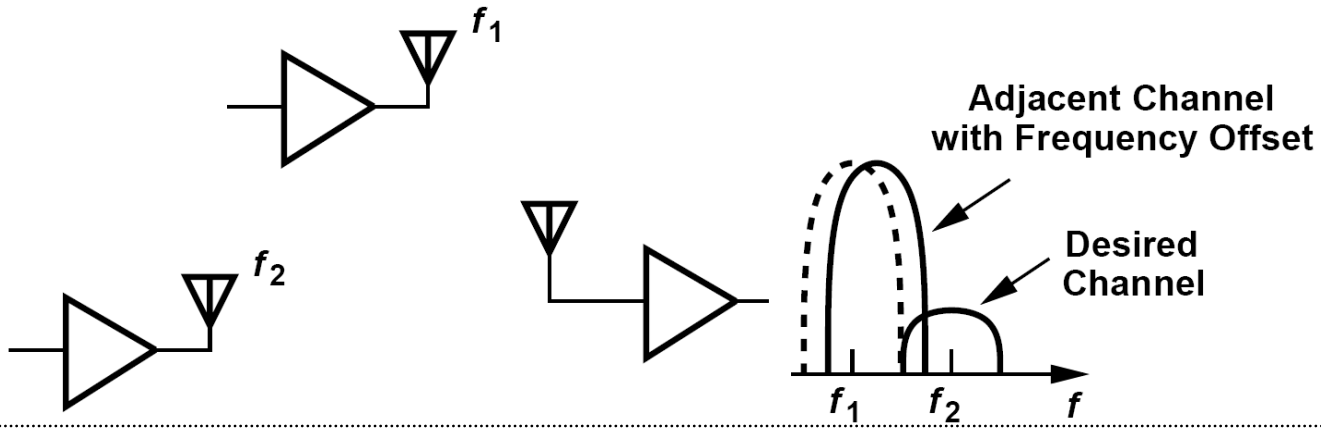
Divider Design

- ✓ Pulse-Swallow Divider
- ✓ Dual-Modulus Dividers
- ✓ CML and TSPC Techniques
- ✓ Miller and Injection-Locked Dividers

General Considerations: Why Do We Need Synthesizers?



- The synthesizer performs the precise setting of LO frequency



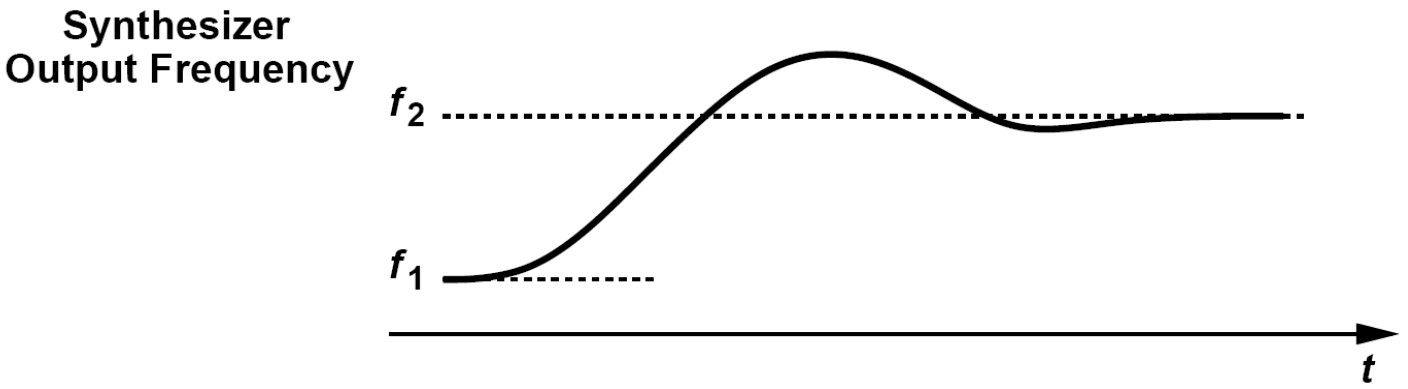
- **A slight shift leads to significant spillage of a high-power interferer in to a desired channel**

Wireless Standards

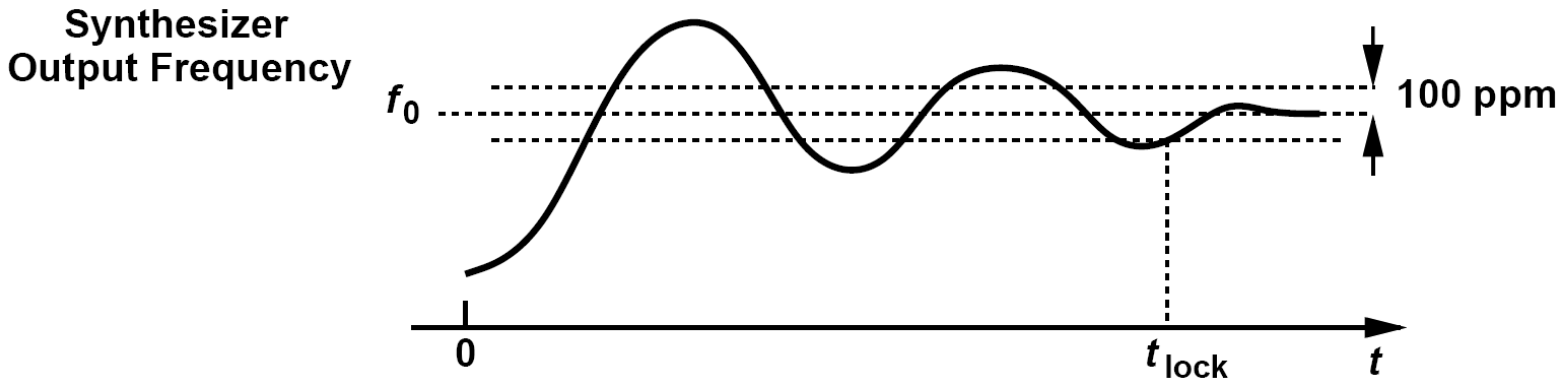
Parameter	DECT	GSM	802.11
Modulation	GFSK	GFSK	GFSK
Data Rate	1.152Mbps	270.8Kbps	1-2Mbps
Frequency	1800MHz	900MHz	2.4-2.5GHz
Channels	10	124	75
Spacing	**1.782MHz**	**200KHz**	**1MHz**

- **Difficult LO design → narrower channel spacing and stringent phase noise/spur requirements**
- **LO for GSM receiver is the hardest**

Lock Time

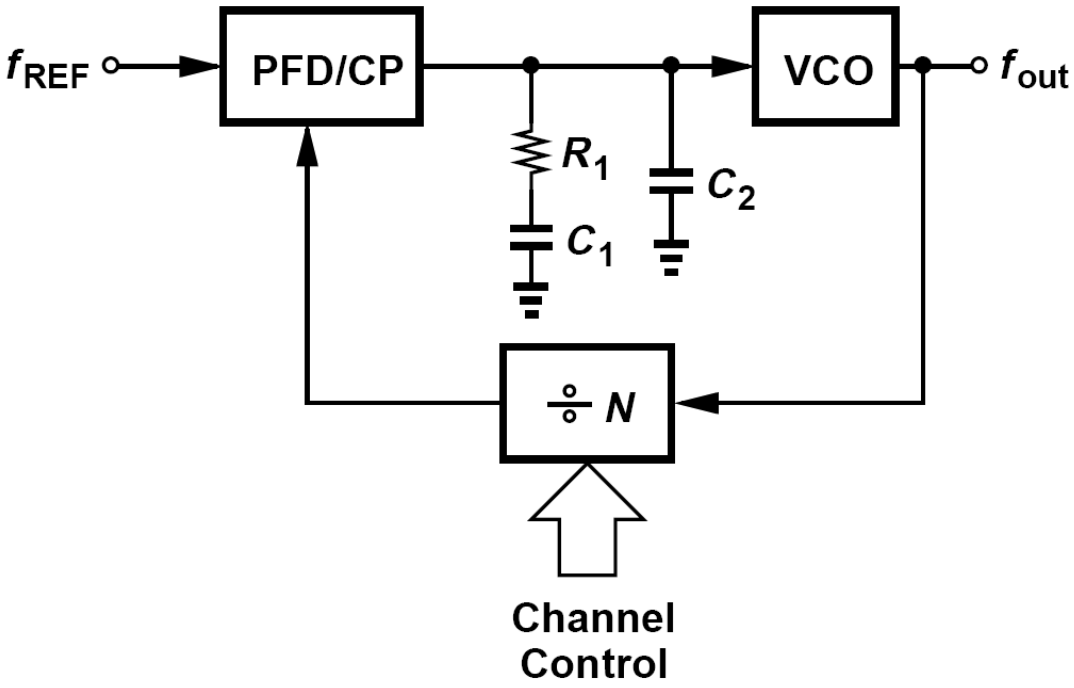


- **Lock time directly subtracts from the time available for communication**



- **The lock time is typically specified as the time required for the output frequency to reach within a certain margin around its final value**

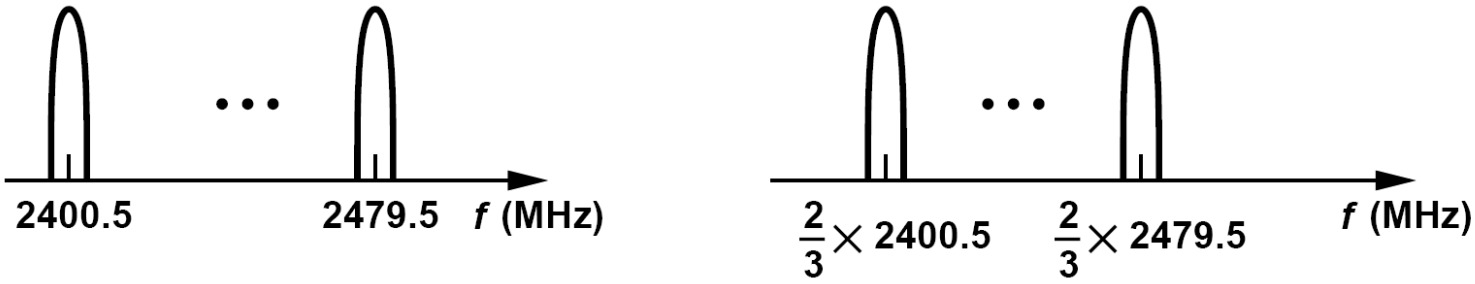
Basic Integer-N Synthesizer



- **Integer-*N* synthesizer produce an output frequency that is an integer multiple of the reference frequency.**
- **The choice of f_{REF}: it must be equal to the desired channel spacing and it must be the greatest common divisor of f_1 and f_2.**

Example of Reference Frequency and Divide Ratio Selection

Compute the required reference frequency and range of divide ratios for an integer-*N* synthesizer designed for a Bluetooth receiver. Consider two cases: (a) direct conversion, (b) sliding-IF downconversion with $f_{LO} = (2/3)f_{RF}$



(a) (b)

(a)Shown in (a), the LO range extends from the center of the first channel, 2400.5 MHz, to that of the last, 2479.5 MHz. Thus, even though the channel spacing is 1 MHz, f_{REF} must be chosen equal to 500 kHz. Consequently, $N_1 = 4801$ and $N_2 = 4959$.

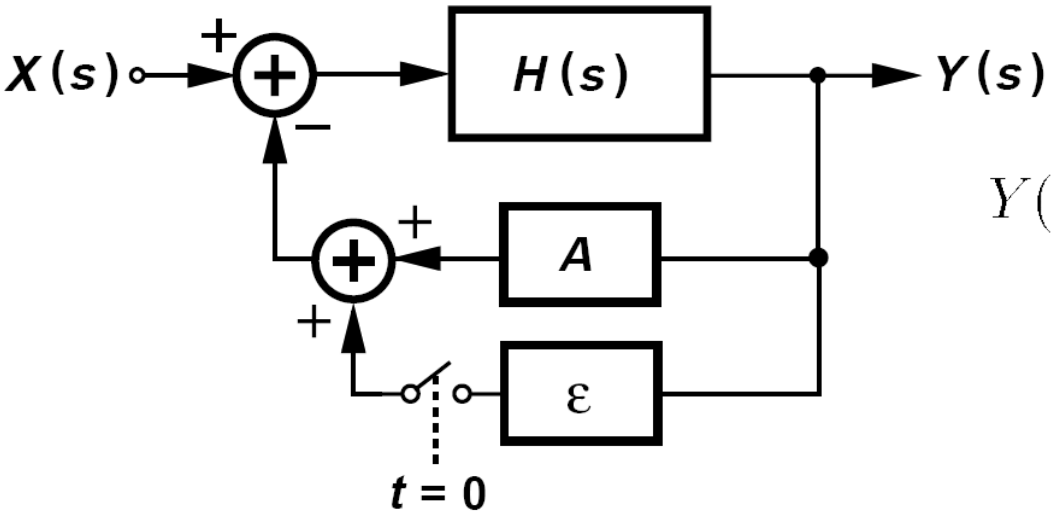
(b) As illustrated in (b), in this case the channel spacing and the center frequencies are multiplied by 2/3. Thus, $f_{REF} = 1/3$ MHz, $N_1 = 4801$, and $N_2 = 4959$.

Choosing N_1 and N_2

- $f_{in} = GCD (f_{ref}, f_{out})$
- f_{ref} = 19.68MHz and f_{out} = 2.402GHz $\rightarrow f_{in}$ = 40 kHz
- f_{ref} = 19.68MHz and f_{in} = 40kHz $\rightarrow N_1$ = 492
- f_{in} = 40kHz and f_{out} = 2.042GHz $\rightarrow N_2$ = 60050

- Need programmable: 2.042GHz $\leq f_{out} \leq$ 2.480GHz
- f_{out} = 2.480GHz + m MHz with $2 \leq m \leq 78$
- $\rightarrow N2 = 60050 + 25 \cdot m$

Settling Behavior: Channel Switching



$$Y(s) = \frac{H(s)}{1+(A+\epsilon)H(s)}X(s)$$

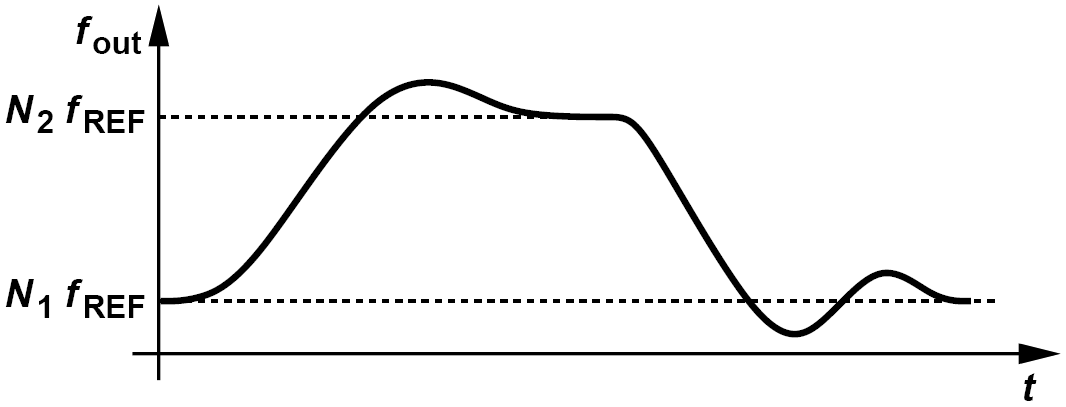
$$\approx \frac{H(s)}{1+AH(s)} \cdot \frac{1}{1+\epsilon/A}X(s)$$

$$\approx \frac{H(s)}{1+AH(s)}\left(1-\frac{\epsilon}{A}\right)X(s)$$

we can view multiplication by (1 –ε/A) as a step function from f_0 to $f_0(1 - \varepsilon/A)$, i.e., a frequency jump of $-(\varepsilon/A)f_0$.

- **When the divide ratio changes, the loop responds as if an input frequency step were applied**

Worst Case Settling and Example of Error



- **The worse case occurs when the synthesizer output frequency must go from the first channel, $N_1 f_{REF}$, to the last, $N_2 f_{REF}$, or vice versa**

In synthesizer settling, the quantity of interest is the frequency error, $\Delta\omega_{out}$, with respect to the final value. Determine the transfer function from the input frequency to this error.

The error is equal to $\omega_{in}[N - H(s)]$, where $H(s)$ is the transfer function of a type-II PLL (Chapter 9). Thus,

$$\frac{\Delta\omega_{out}}{\omega_{in}} = N\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Calculation of Settling Time

Assuming $N_2 - N_1 << N_1$

If the divide ratio jumps from N_1 to N_2, this change is equivalent to an input frequency step of $\Delta\omega_{in} = (N_2 - N_1)\omega_{REF} = N_1$.

For the normalized error to fall below a certain amount, α, we have

$$\left|1 - \frac{N_1}{N_2}\right| g(t)u(t) \leq \alpha$$

Where

$$g(t) = 1 - \left[\cos(\sqrt{1-\zeta^2}\omega_n t) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin(\sqrt{1-\zeta^2}\omega_n t)\right] e^{-\zeta\omega_n t} \quad \zeta < 1$$

$$= 1 - (1 - \omega_n t)e^{-\zeta\omega_n t} \quad \zeta = 1$$

$$= 1 - \left[\cosh(\sqrt{\zeta^2-1}\omega_n t) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh(\sqrt{\zeta^2-1}\omega_n t)\right] e^{-\zeta\omega_n t} \quad \zeta > 1.$$

For example, if ζ=$\sqrt{2}/2$

$$\left|1 - \frac{N_1}{N_2}\right| \left(\cos\frac{\omega_n t_s}{\sqrt{2}} - \sin\frac{\omega_n t_s}{\sqrt{2}}\right) e^{-\omega_n t_s/\sqrt{2}} = \alpha$$

$$\left|1 - \frac{N_1}{N_2}\right| \sqrt{2} e^{-\omega_n t_s/\sqrt{2}} = \alpha \quad \Rightarrow \quad t_s = \frac{\sqrt{2}}{\omega_n} \ln\left|\sqrt{2}\left(1 - \frac{N_1}{N_2}\right)\frac{1}{\alpha}\right|$$

Example of Settling Time Calculation

A 900-MHz GSM synthesizer operates with f_{REF} = 200 kHz and provides 128 channels. If ζ=$\sqrt{2}/2$, determine the settling time required for a frequency error of 10 ppm.

The divide ratio is approximately equal to 4500 and varies by 128, i.e., $N_1 \approx 4500$ and $N_2 - N_1 = 128$. Thus,

$$t_s \approx \sqrt{2}\frac{8.3}{\omega_n} \quad \text{or} \quad t_s = \frac{8.3}{\zeta\omega_n}$$

While this relation has been derived for $\zeta = \sqrt{2}/2$, it provides a reasonable approximation for other values of ζ up to about unity. How is the value of $\zeta\omega_n$ chosen? From Chapter 9, we note that the loop time constant is roughly equal to one-tenth of the input period. It follows that $(\zeta\omega_n)^{-1} \approx 10T_{REF}$ and hence

$$t_s \approx 83T_{REF}$$

In practice, the settling time is longer and a rule of thumb for the settling of PLLs is 100 times the reference period.

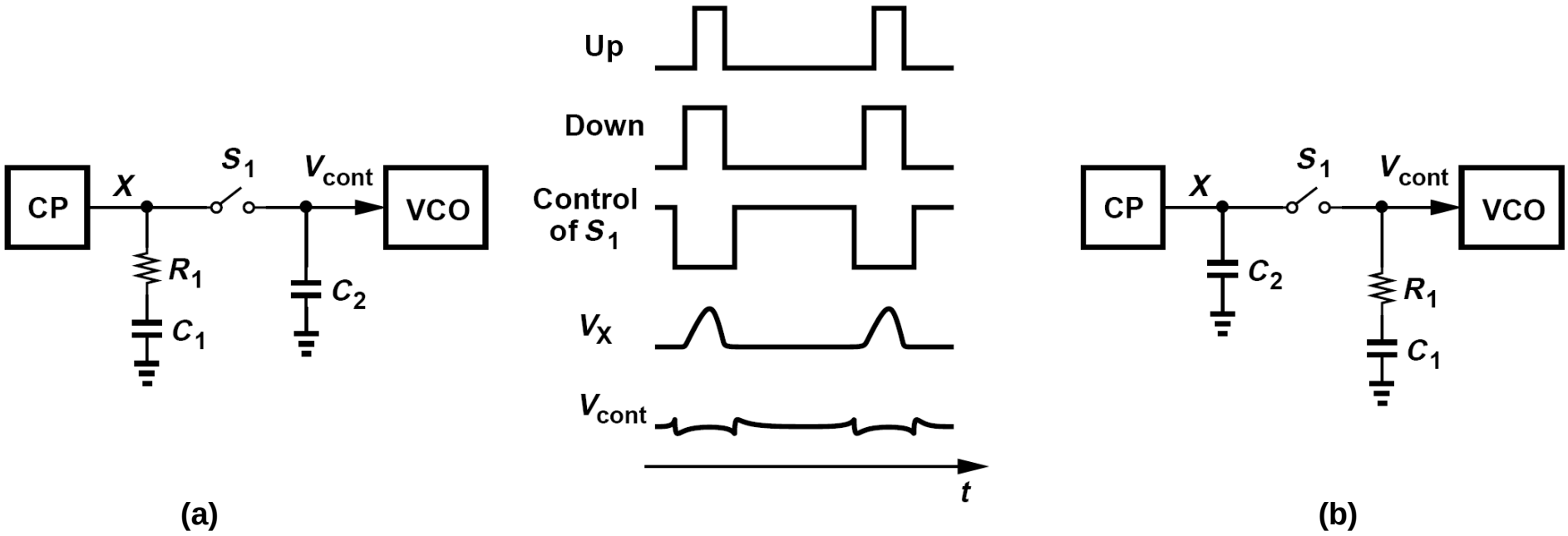
Spur Reduction Techniques: Will Scaling Down Transistor Widths Work?

A student reasons that if the transistor widths and drain currents in a charge pump are scaled down, so is the ripple. Is that true?

Solution:

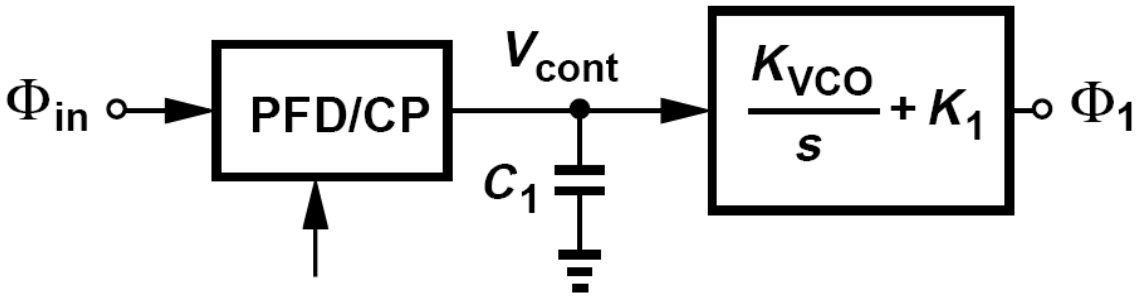
This is true because the ripple is proportional to the absolute value of the unwanted charge pump injections rather than their relative value. This reasoning, however, can lead to the wrong conclusion that scaling the CP down reduces the output sideband level. Since a reduction in I_P must be compensated by a proportional increase in K_{VCO} so as to maintain _ constant, the sideband level is almost unchanged.

Spur Reduction Techniques: Masking the Ripple by Insertion of a Switch



- V_{cont} is disturbed for a short duration (at the phase comparison instant) and remains relatively constant for the rest of the input period.
- The arrangement of (a) leads to an unstable PLL
- Topology of (b) can yield a stable PLL

Stabilization of PLL by Adding K_1 to the Transfer Function of VCO (I)



Open-loop transfer function of a type-II second-order PLL

$$H_{open}(s) = \frac{I_P}{2\pi}\left(R_1 + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{s}$$

Can we realize:

$$H_{open}(s) = \frac{I_P}{2\pi}\frac{1}{C_1 s}\left(\frac{K_{VCO}}{s} + K_1\right)$$

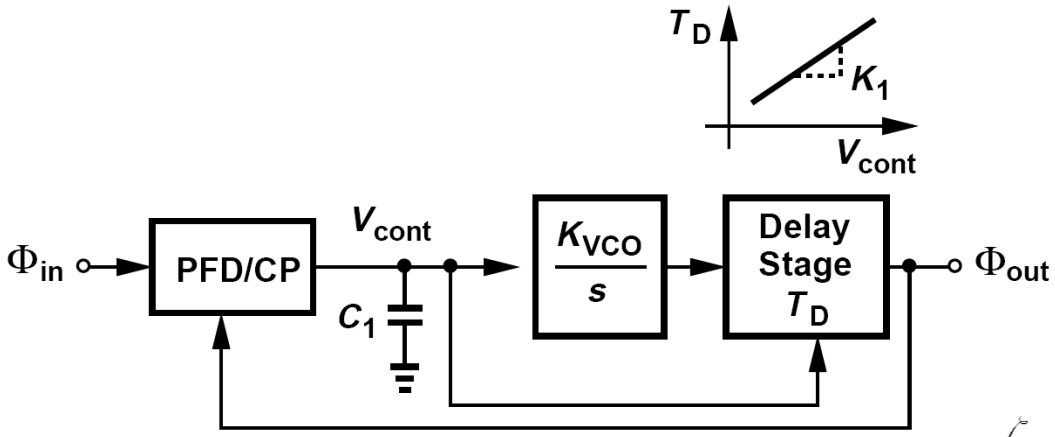
to obtain a zero?

$$\frac{\phi_1}{V_{cont}}(s) = \frac{K_{VCO}}{s} + K_1$$

Indeed, K_1 represents a variable-delay stage having a "gain" of K_1:

$$K_1 = \frac{\Delta T_d}{\Delta V_{cont}}$$

Stabilization of PLL by Adding K_1 to the Transfer Function of VCO (Ⅱ)



$$H_{closed}(s) = \frac{\frac{I_P}{2\pi C_1 s}(\frac{K_{VCO}}{s} + K_1)}{1 + \frac{I_P}{2\pi C_1 s}(\frac{K_{VCO}}{s} + K_1)}$$

$$= \frac{\frac{I_P K_1}{2\pi C_1}s + \frac{I_P K_{VCO}}{2\pi C_1}}{s^2 + \frac{I_P K_1}{2\pi C_1}s + \frac{I_P K_{VCO}}{2\pi C_1}}.$$

$$\zeta = \frac{K_1}{2}\sqrt{\frac{I_P}{2\pi C_1 K_{VCO}}}$$

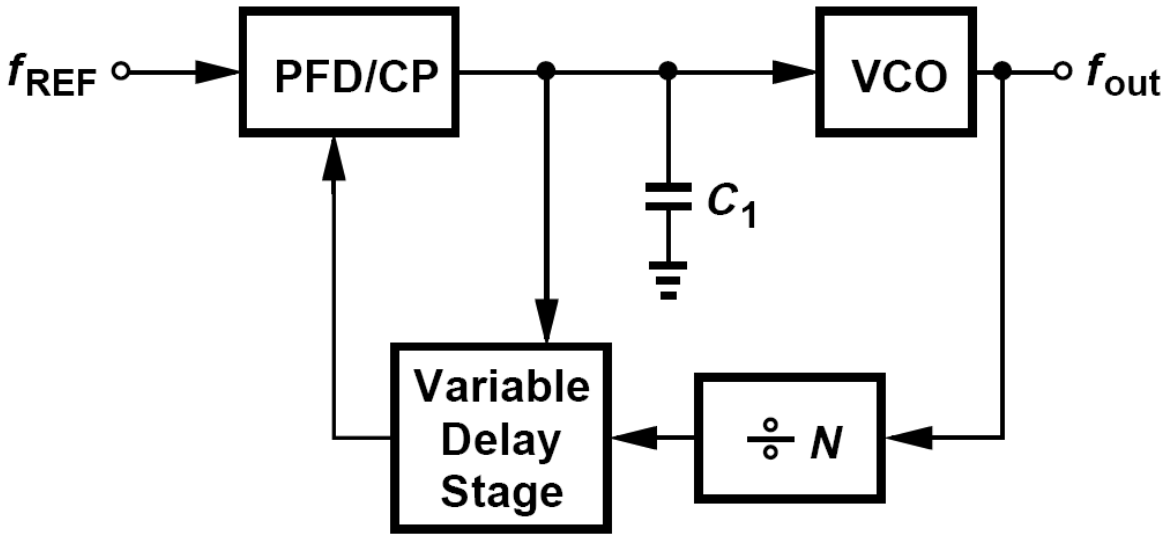
$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}$$

With Divider

$$\zeta = \frac{K_1}{2}\sqrt{\frac{I_P}{2\pi C_1 K_{VCO} N}}$$

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1 N}}.$$

Stabilization of PLL by Adding K_1 to the Transfer Function of VCO: Modified Architecture



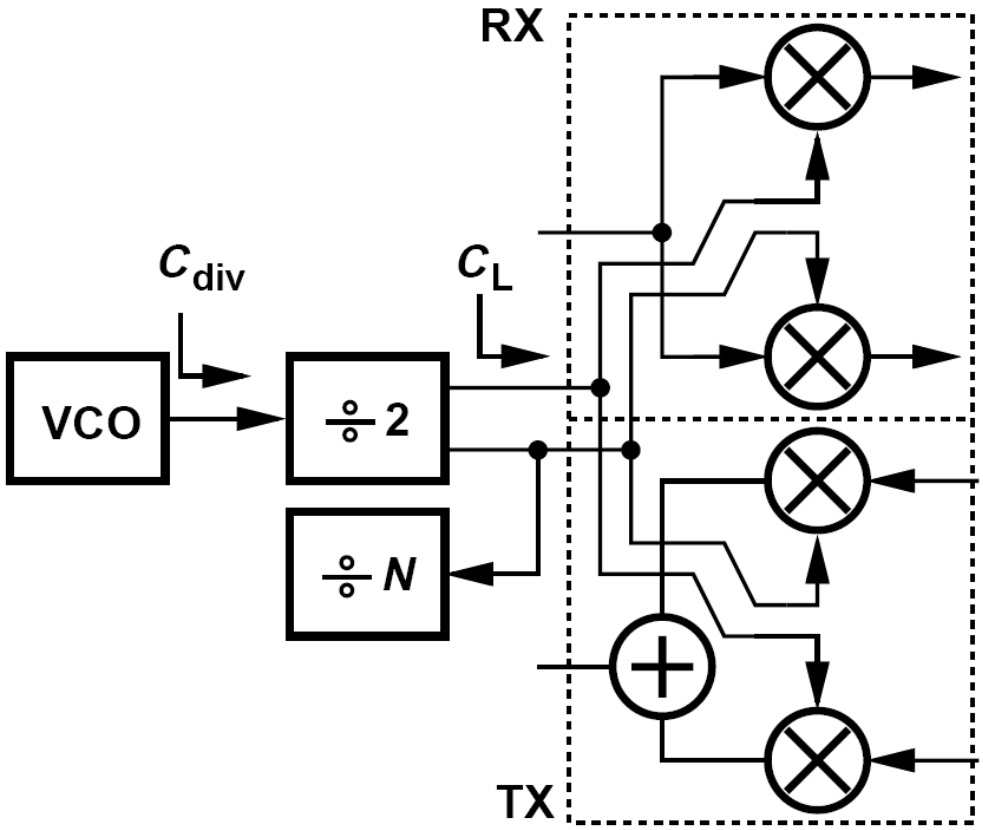
$$\zeta = \frac{K_1}{2}\sqrt{\frac{I_P N}{2\pi C_1 K_{VCO}}}$$

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1 N}}.$$

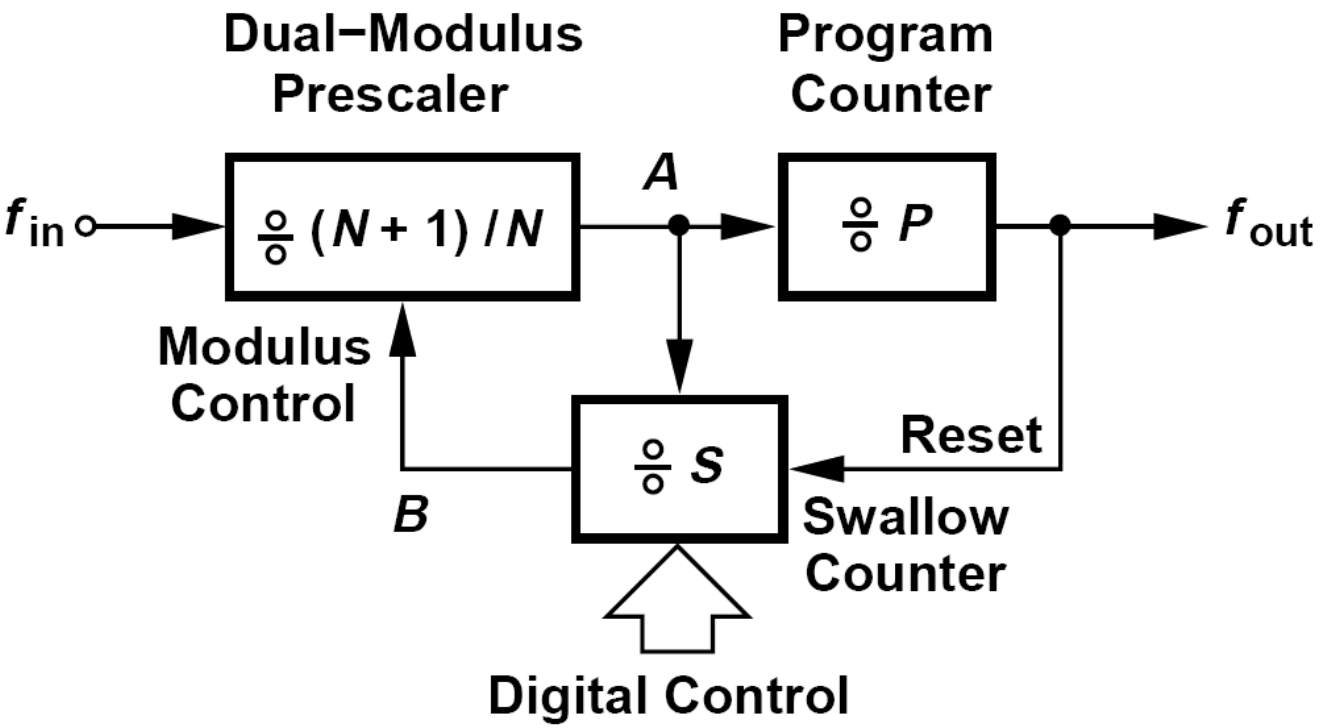
- **A retiming flipflop can be inserted between the delay line and the PFD to remove the phase noise of the former**

Divider Design: Requirements

- **The divider modulus, *N*, must change in unity steps**
- **The first stage of the divider must operates as fast as the VCO**
- **The divider input capacitance and required input swing must be commensurate with the VCO drive capability**
- **The divider must consume low power, preferably less than the VCO**

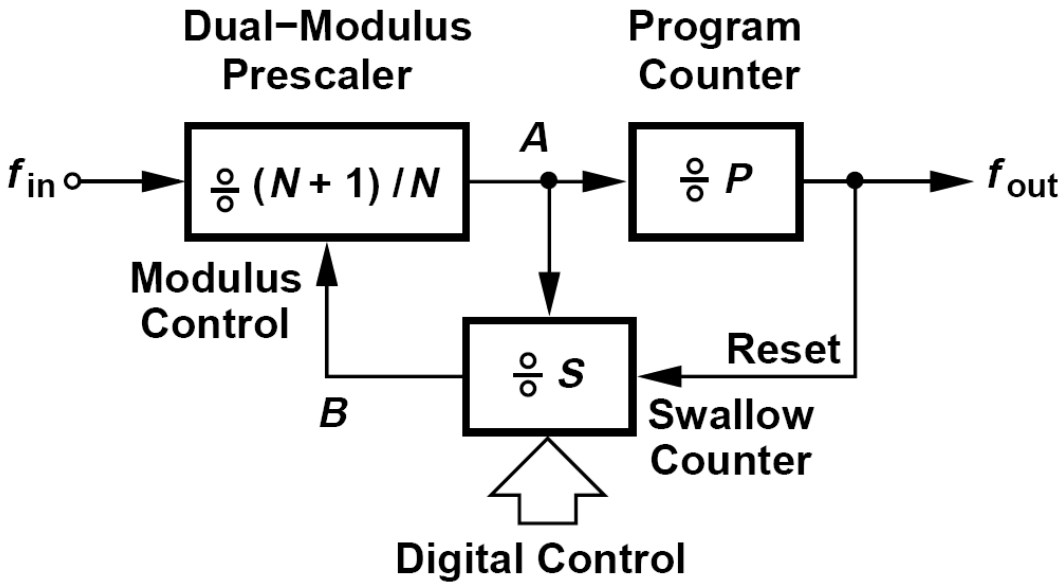


Pulse Swallow Divider



- **Sensing the high-frequency input, the prescaler proves the most challenging of the three building blocks.**
- **As a rule of thumb, dual-modulus prescalers are about a factor of two slower than ÷2 circuits**

Pulse Swallow Divider

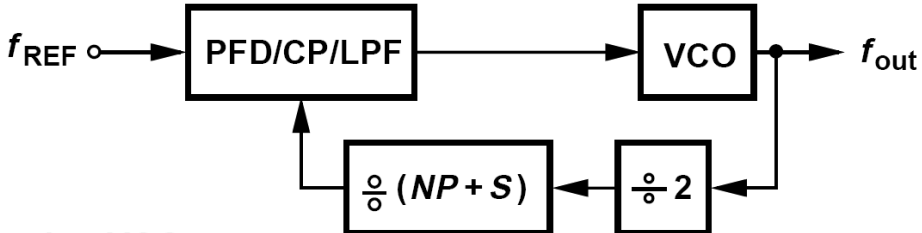


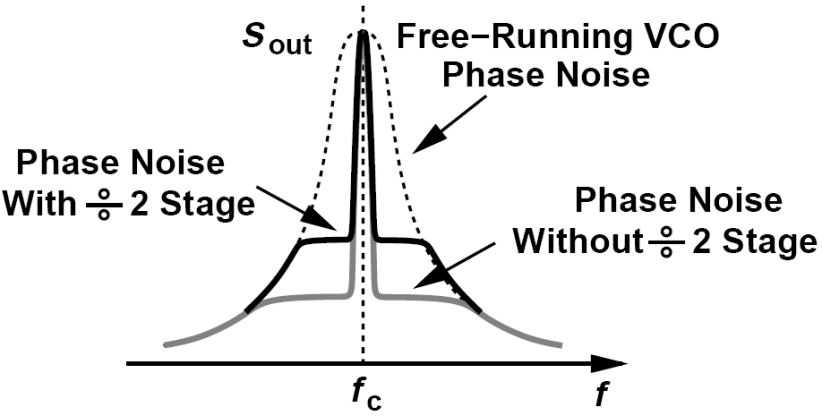
- S pulses counted with a (N+1) modulus, and remaining (P-S) pulses counted with a N modulus
- Adding the total number of pulses at the prescalar input in the two modes
  - $(N+1)S + N(P-S) = NP + S$
- Thus, for every NP+S pulse at the main input, the PC generates one pulse at the output.

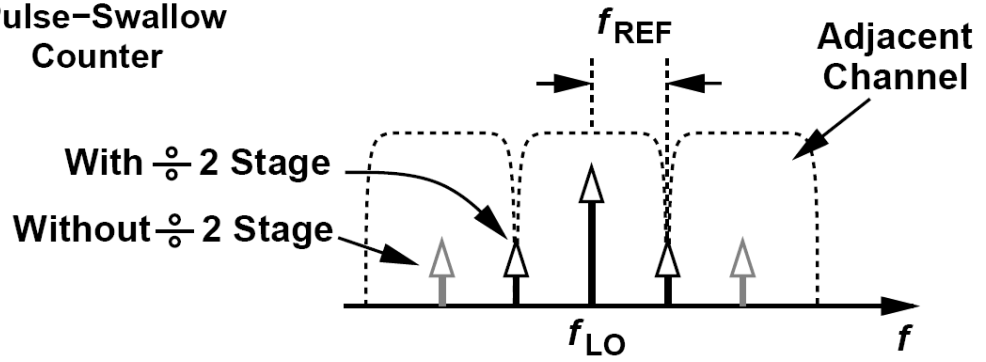
Example of Preceding the Pulse Swallow Divider by a ÷2

In order to relax the speed required of the dual-modulus prescaler, the pulse swallow divider can be preceded by a ÷2. Explain the pros and cons of this approach.

Solution:

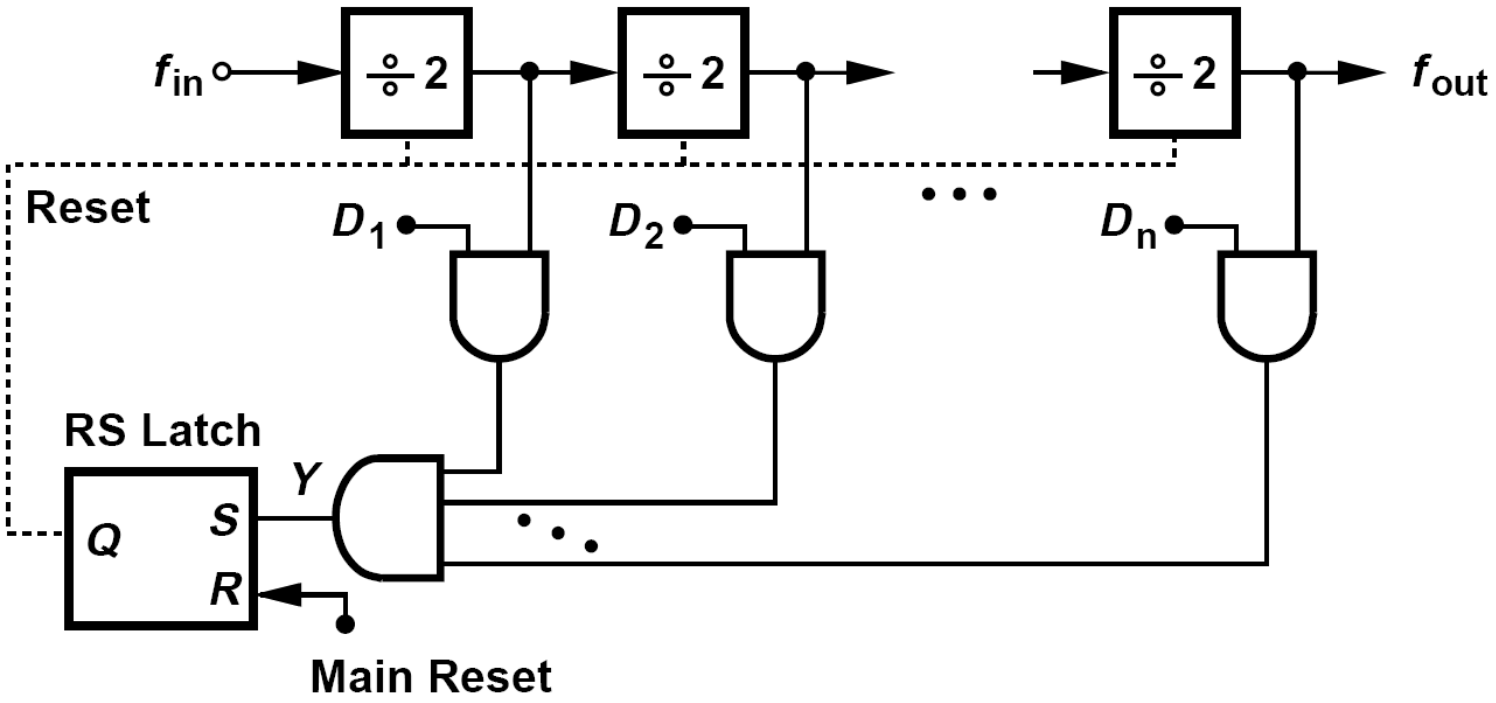






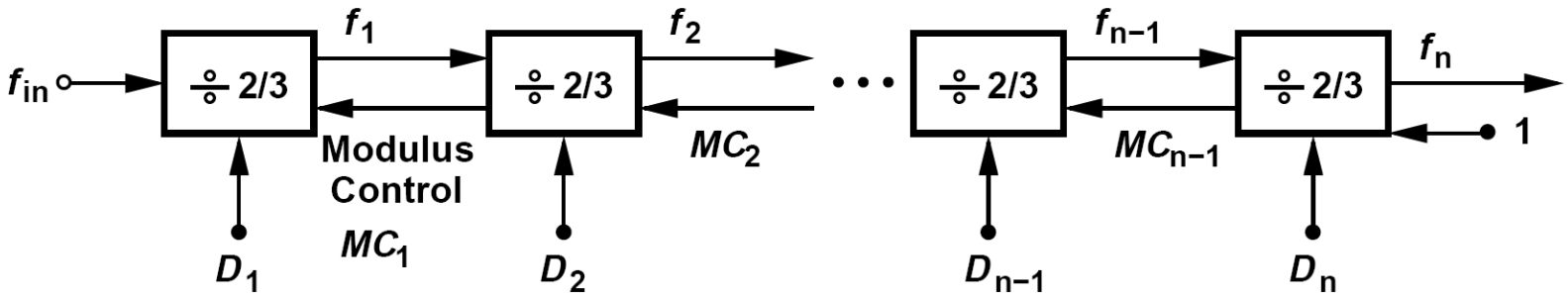
Here, $f_{out} = 2(NP + S)f_{REF}$. Thus, a channel spacing of f_{ch} dictates $f_{REF} = f_{ch}$=2. The lock speed and the loop bandwidth are therefore scaled down by a factor of two, making the VCO phase noise more pronounced. One advantage of this approach is that the reference sideband lies at the edge of the adjacent channel rather than in the middle of it. Mixed with little spurious energy, the sidebands can be quite larger than those in the standard architecture.

Swallow Counter Realization



- **The swallow counter is typically designed as an asynchronous circuit for the sake of simplicity and power saving**

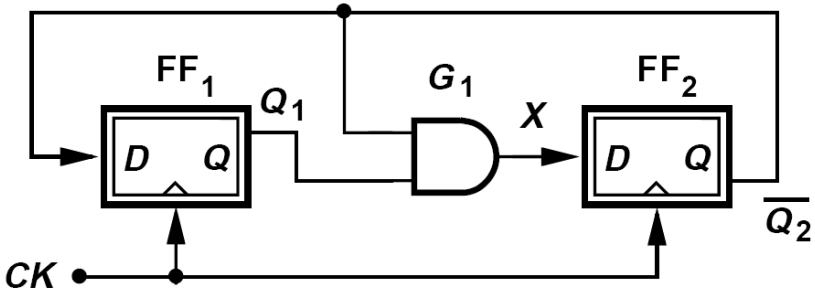
Modular Divider Realizing Multiple Divider Ratios



- **This method incorporates ÷2/3 stages in a modular form so as to reduce the design complexity. Each ÷2/3 block receives a modulus control from the next stage. The digital inputs set the overall divide ratio according to:**

$$N = 2^n + D_n 2^{n-1} + D_{n-1} 2^{n-2} + \cdots + 2D_2 + D_1$$

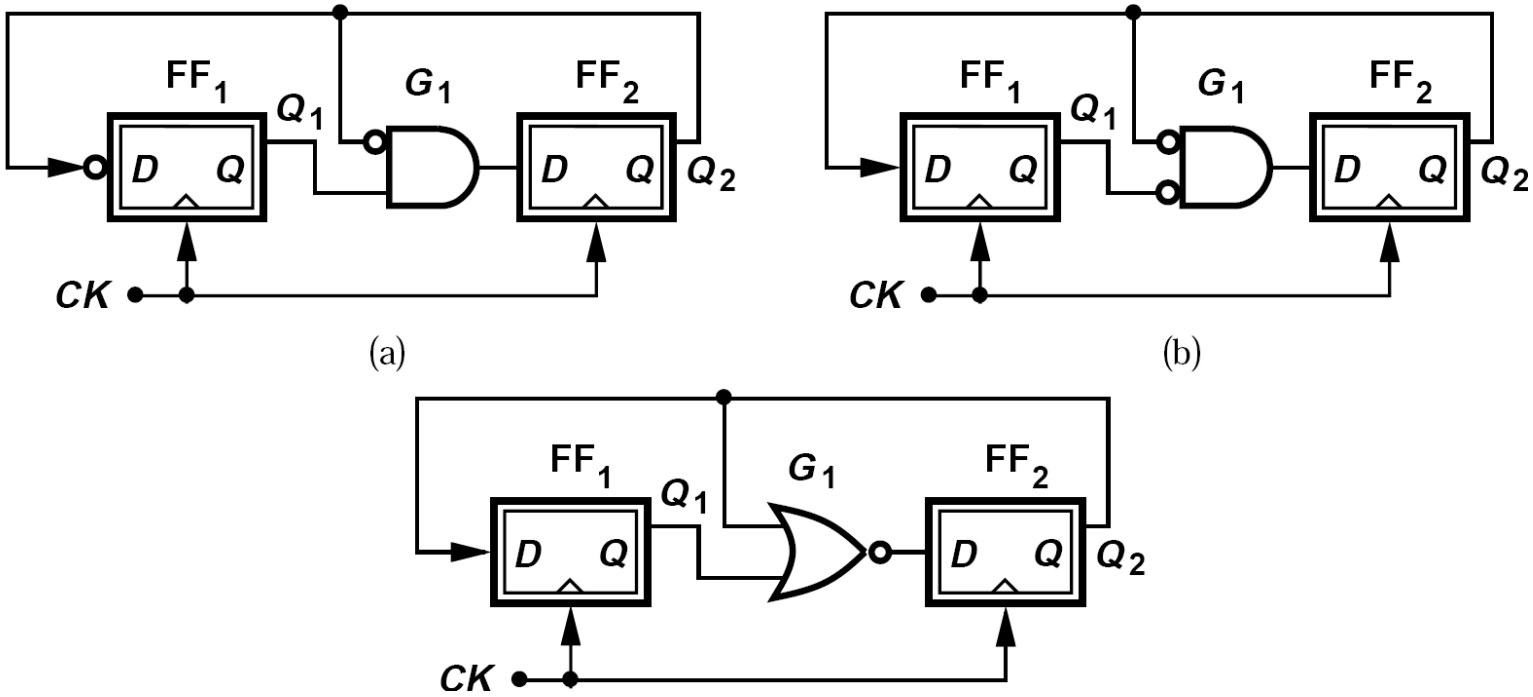
Divide- by-3 Circuit:



Suppose the circuit begins with $Q_1\overline{Q}_2$ = 00. next three cycles, $Q_1\overline{Q}_2$ goes to 10, 11, and 01. Note that the state Q_1Q_2 = 00 does not occur again because it would require the previous values of $\overline{Q}_2$ and X to be ZERO and ONE, respectively,

Example of a ÷3 Circuit Using a NOR Gate rather than a AND Gate

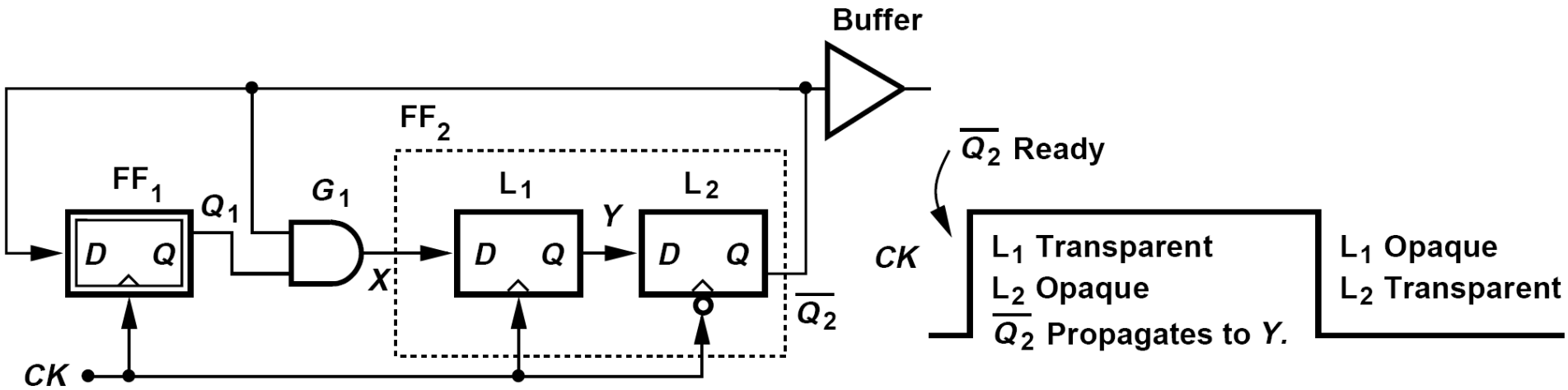
Design a ÷3 circuit using a NOR gate rather than an AND gate.



We begin with the previous topology, sense the *Q* output of FF_2, and add "bubbles" to compensate for the logical inversion. The inversion at the input of FF_1 can now be moved to its output and hence realized as a bubble at the corresponding input of the AND gate. Finally, the AND gate with two bubbles at its input can be replaced with a NOR gate. The reader can prove that this circuit cycles through the following three states: Q_1Q_2 = 00; 01; 10.

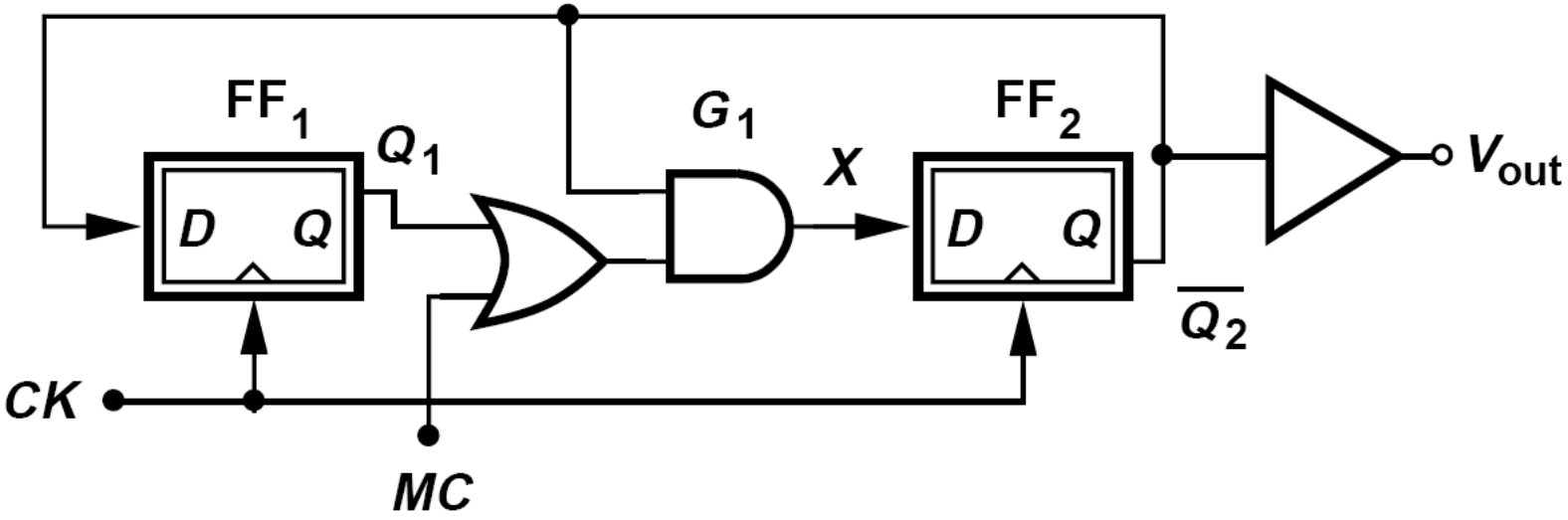
Speed Limitation of the ÷3 Stage

Analyze the speed limitations of the ÷3 stage shown in Fig. 10.28



We draw the circuit as above, explicitly showing the two latches within FF_2. Suppose *CK* is initially low, L_1 is opaque (in the latch mode), and L_2 is transparent (in the sense mode). In other words, $\overline{Q_2}$ has just changed. When *CK* goes high and L_1 begins to sense, the value of Q_2 must propagate through G_1 and L_1 before *CK* can fall again. Thus, the delay of G_1 enters the critical path. Moreover, L_2 must drive the input capacitance of FF_1, G_1, and an output buffer. These effects degrade the speed considerably, requiring that *CK* remain high long enough for $\overline{Q_2}$ to propagate to *Y* .

Divide-by-2/3 Circuit

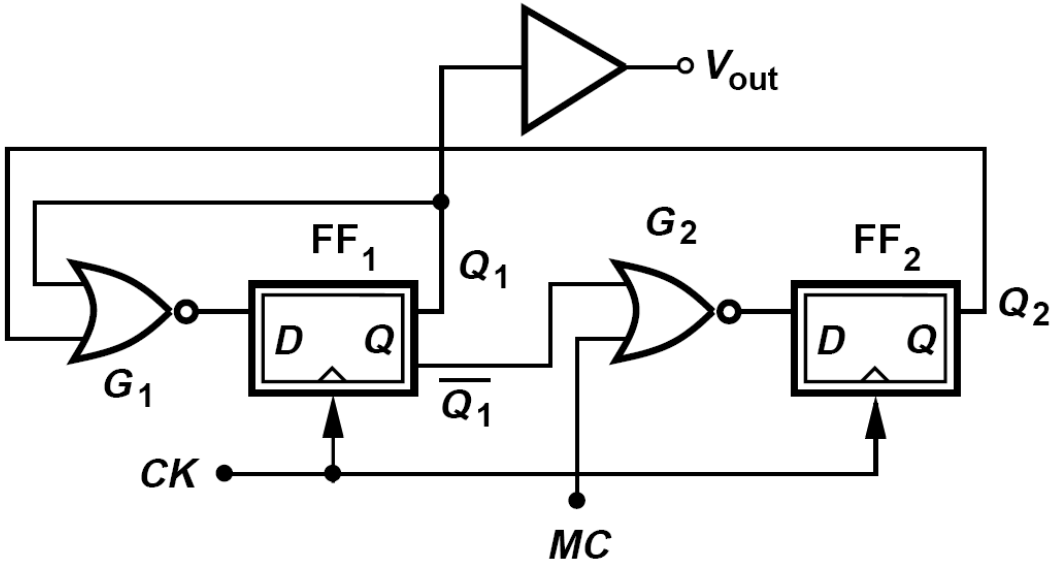


- **The ÷2/3 circuit employs an OR gate to permit ÷3 operation if the modulus control, MC, is low or ÷2 operation if it is high**

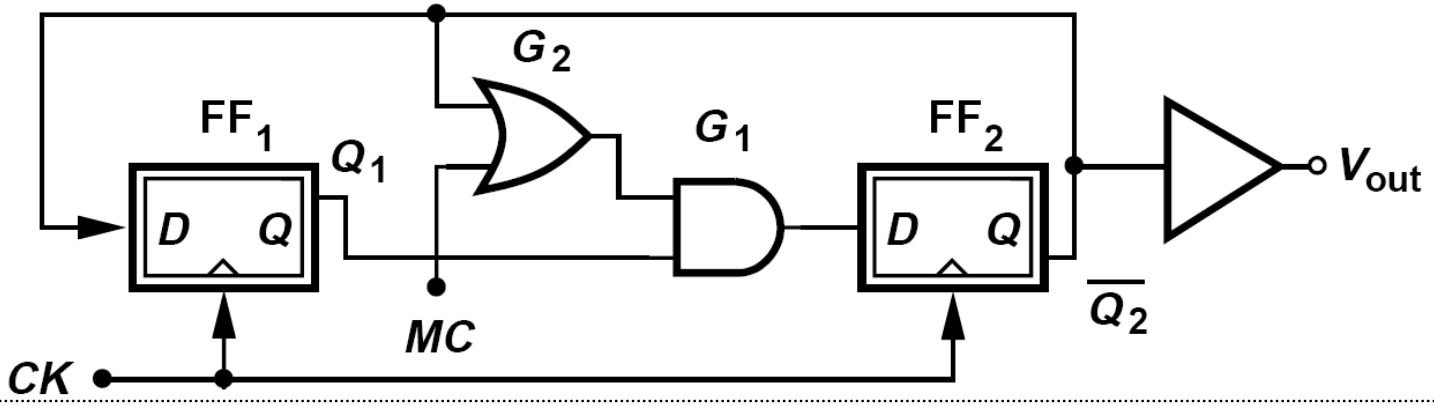
A student seeking a low-power prescaler design surmises that FF_1 in the ÷ 3 circuit can be turned off when MC goes high. Explain whether this is a good idea.

While saving power, turning off FF_1 may prohibit instantaneous modulus change because when FF_1 turns on, its initial state is undefined, possibly requiring an additional clock cycle to reach the desired value. For example, the overall circuit may begin with $Q_1\overline{Q}_2 = 00$.

Divide-by-2/3 Circuit with Higher Speed and Divide-by-3/4 Circuit

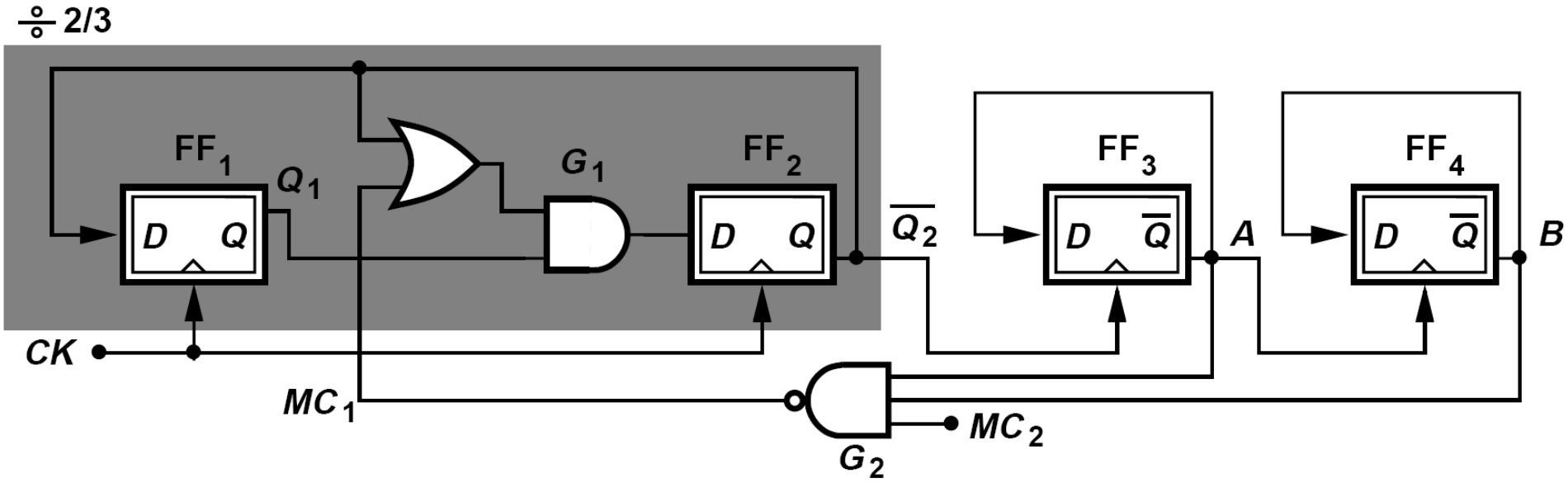


- **The output can be provided by only *FF*$_1$. This circuit has a 40% speed advantage over ÷2/3 circuit we introduced previously.**



- **When *MC*=ONE, the circuit divides by 4; If *MC*=0, it divides by 3**

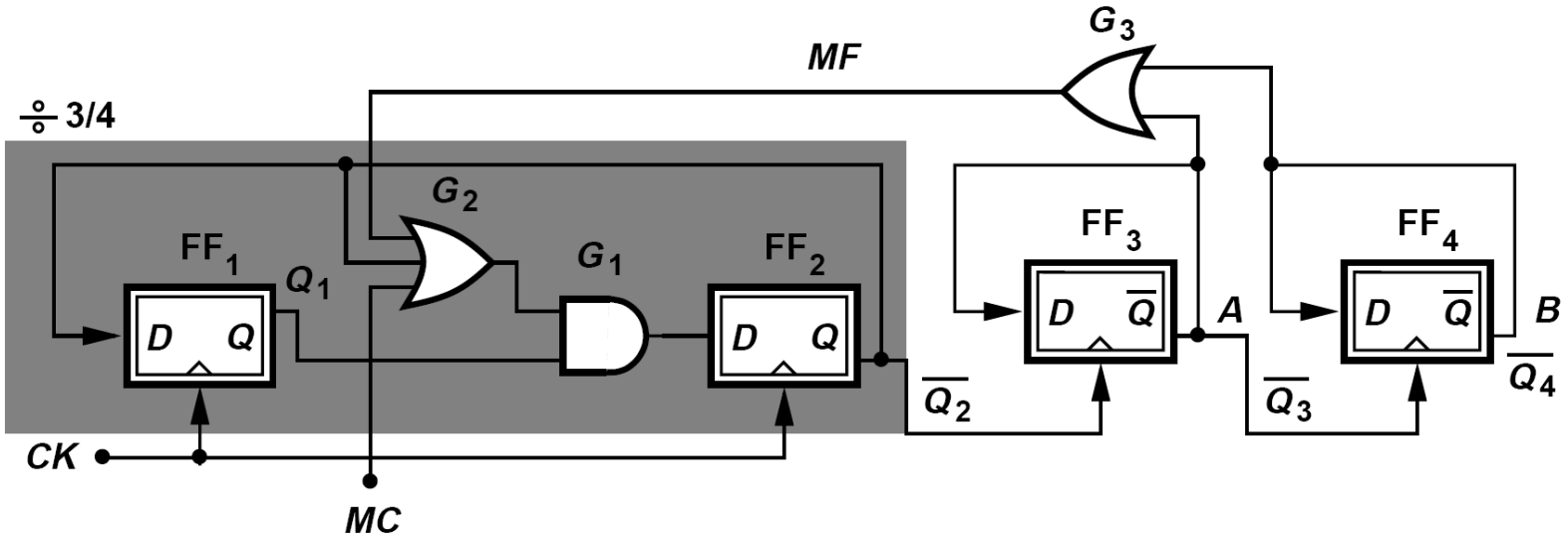
Divide-by-8/9 Circuit



- For higher moduli, a synchronous core having small moduli is combined with asynchronous divider stages.
- If MC_2 is low, MC_1 is high, the overall circuit operates as a ÷8 circuit; if MC_2 is high, the circuit divides by 9.

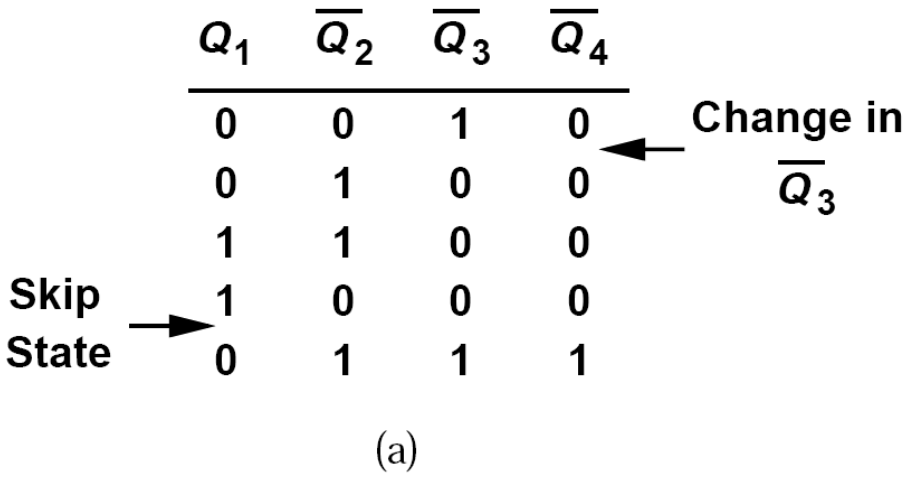
Example: Design of a Divide-by-15/16 Circuit

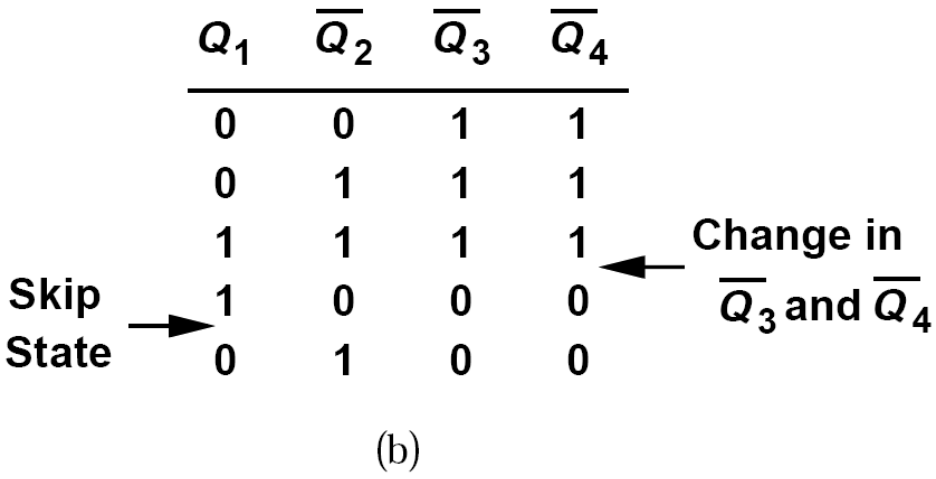
Design a ÷15/16 circuit using the synchronous ÷3/4 stage.



Since the ÷3/4 stage (D34) divides by 4 when *MC* is high, we surmise that only two more ÷2 circuits must follow to provide ÷16. To create ÷15, we must force D34 to divide by 3 for one clock cycle. Shown in the figure above, the circuit senses the outputs of the asynchronous ÷2 stages by an OR gate and lowers *MF* when *AB* = 00. Thus, if *MC* is high, the circuit divides by 16. If *MC* is low and the ÷2 stages begin from 11, *MF* remains high and D34 divides by 4 until *AB* = 00. At this point, *MF* falls and D34 divides by 3 for one clock cycle before *A* goes high.

Potential Race Conditions

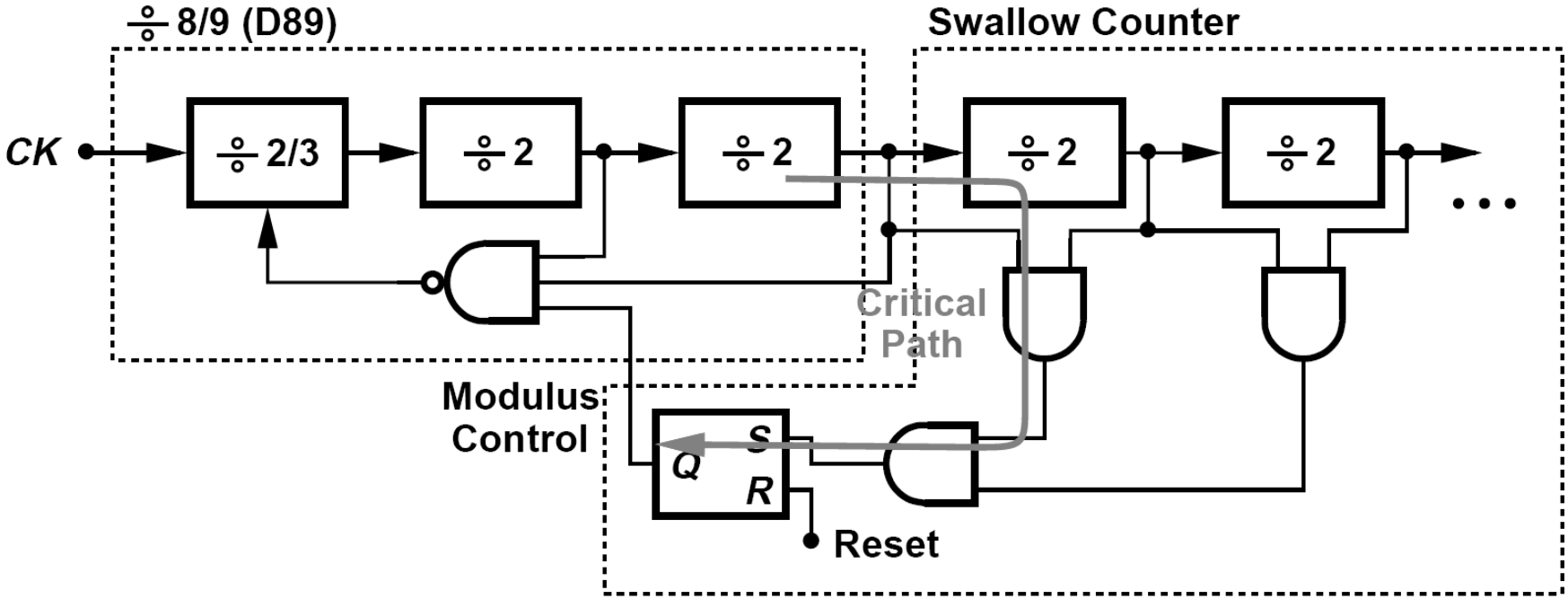




- First suppose FF_3 and FF_4 change their output state on the rising edge of their clock inputs. If MC is low, the circuit continues to divide by 16. As in (a), state 00 is skipped. The propagation delay through FF_3 and G_3 need not be less than a cycle of CK_{in}
- In the case FF_3 and FF_4 change their output state on the falling edge of their clock inputs, the ÷3/4 circuit must skip the state 00. This is in general difficult to achieve, complicating the design and demanding higher power dissipation. Thus the first choice is preferable.

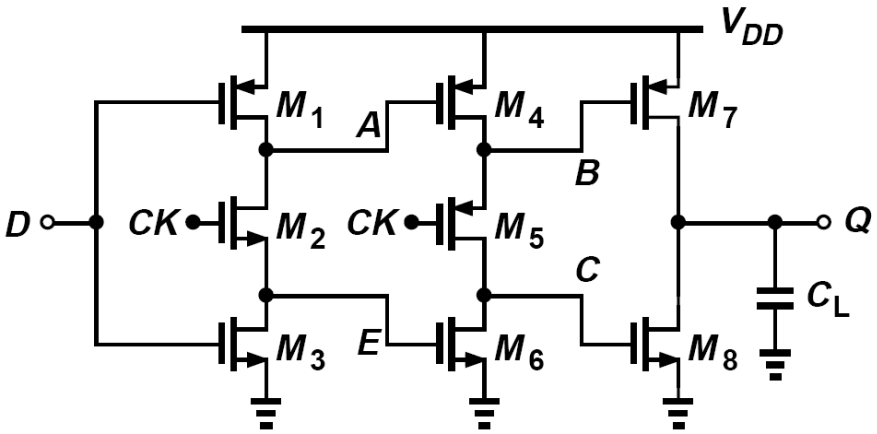
Example of Choice of Prescaler Modulus

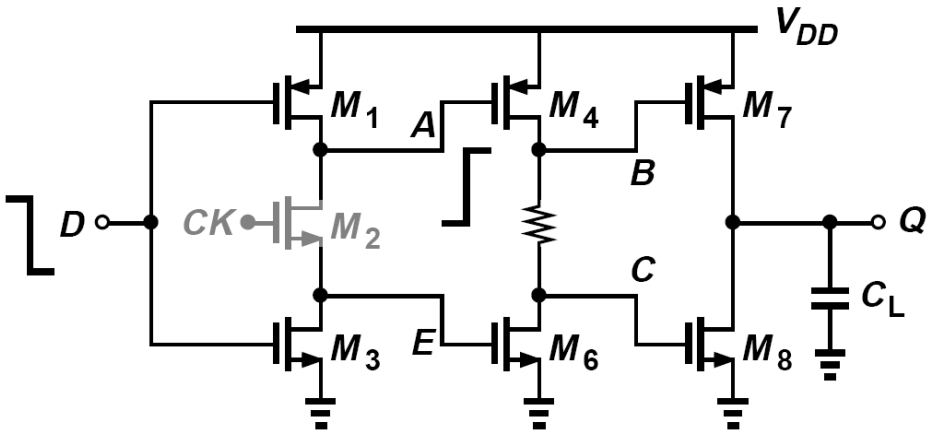
Consider the detailed view of a pulse swallow divider shown below. Identify the critical feedback path through the swallow counter.



When the ÷9 operation of the prescaler begins, the circuit has at most seven input cycles to change its modulus to 8. Thus, the last pulse generated by the prescaler in the previous ÷8 mode (just before the ÷9 mode begins) must propagate through the first ÷2 stage in the swallow counter, the subsequent logic, and the RS latch in fewer than seven input cycles.

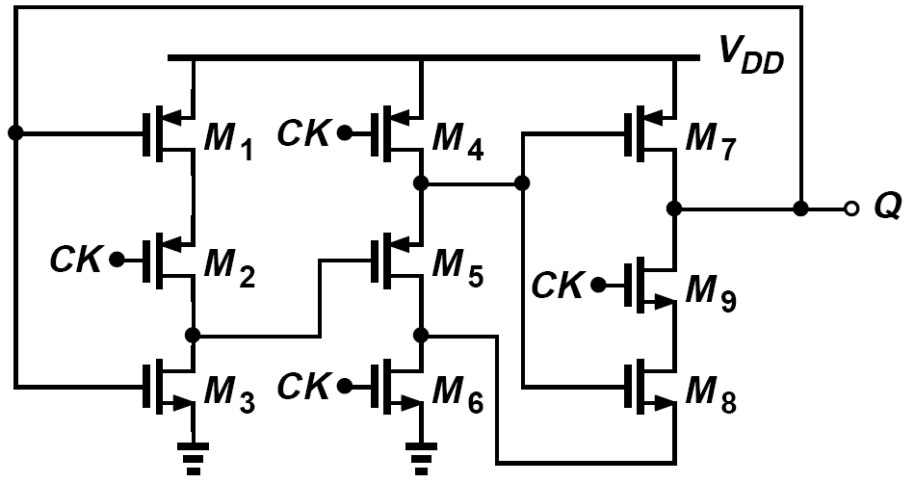
Divider Logic Styles: True Single-Phase Clocking



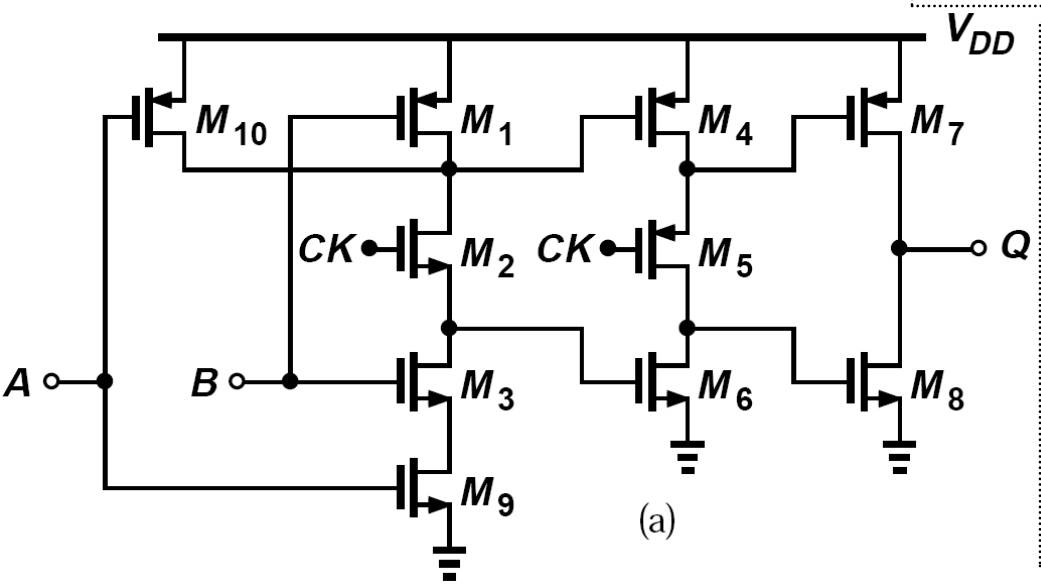


- **When *CK* is high, the first stage operates as an inverter, impressing $\overline{D}$ at *A* and *E*. When *CK* goes low, the first stage is disabled and the second stage becomes transparent, writing $\overline{A}$ at *B* and *C* and hence making *Q* equal to *A*. The logical high at *E* and the logical low at *B* are degraded but the levels at *A* and *C* ensure proper operation of the circuit.**

TSPC Divide-by-2 Circuit / Incorporating a NAND Gate

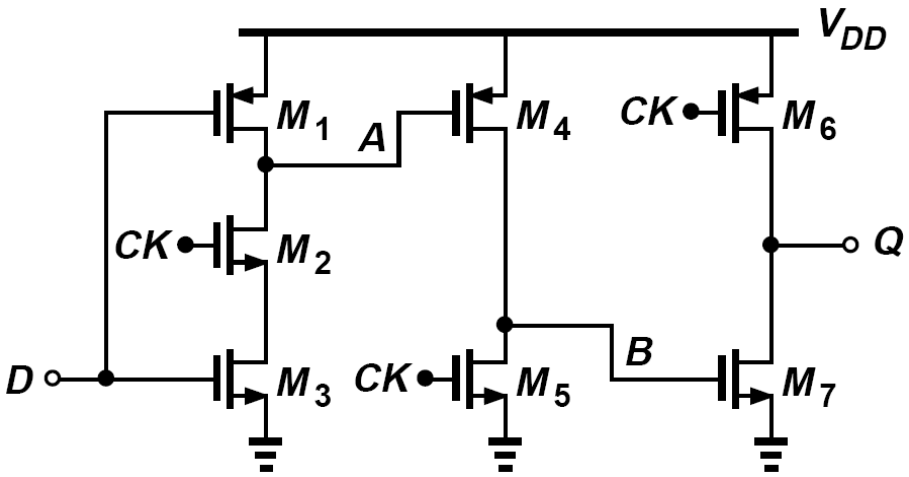


- This topology achieves relatively high speeds with low power dissipation, but, unlike CML dividers, it requires rail-to-rail clock swings for proper operation.
- The circuit consumes no static power and as a dynamic logic topology, the divider fails at very low clock frequencies due to the leakage of the transistors.



- A NAND gate can be merged with the master latch.
- In the design of TSPC circuit, one observes that wider clocked devices raises the maximum speed, but at the cost of loading the preceding stage.

TSPC Using Ratioed Logic



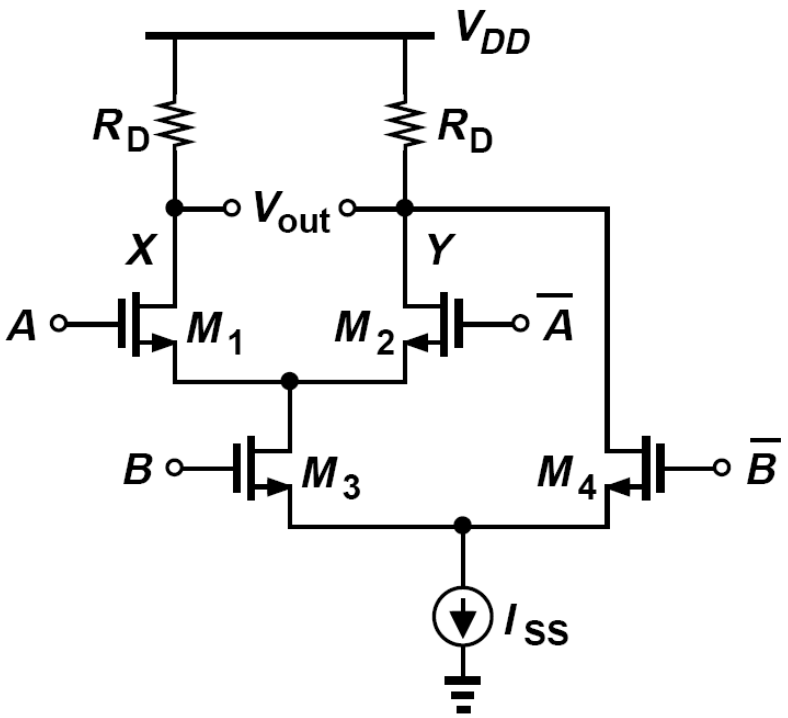
- **The slave latch is designed as "ratioed" logic, achieving higher speeds.**

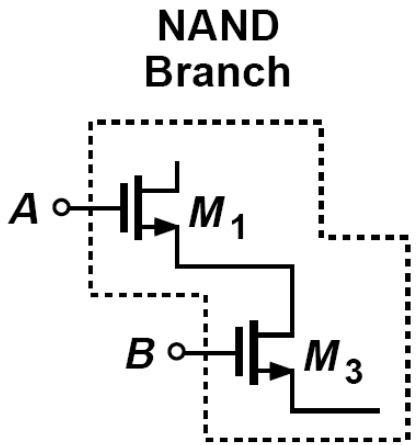
The first stage in figure above is not completely disabled when *CK* is low. Explain what happens if *D* changes in this mode.

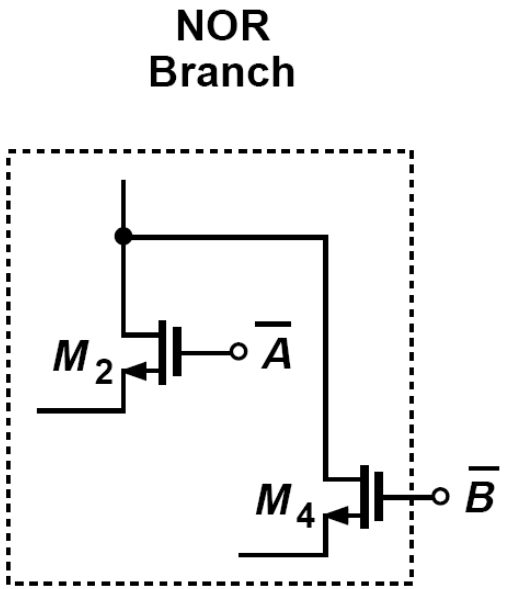
Solution:

If *D* goes from low to high, *A* does not change. If *D* falls, *A* rises, but since M_4 turns off, it cannot change the state at *B*. Thus, *D* does not alter the state stored by the slave latch.

Divider Logic Styles-Current Steering Circuit

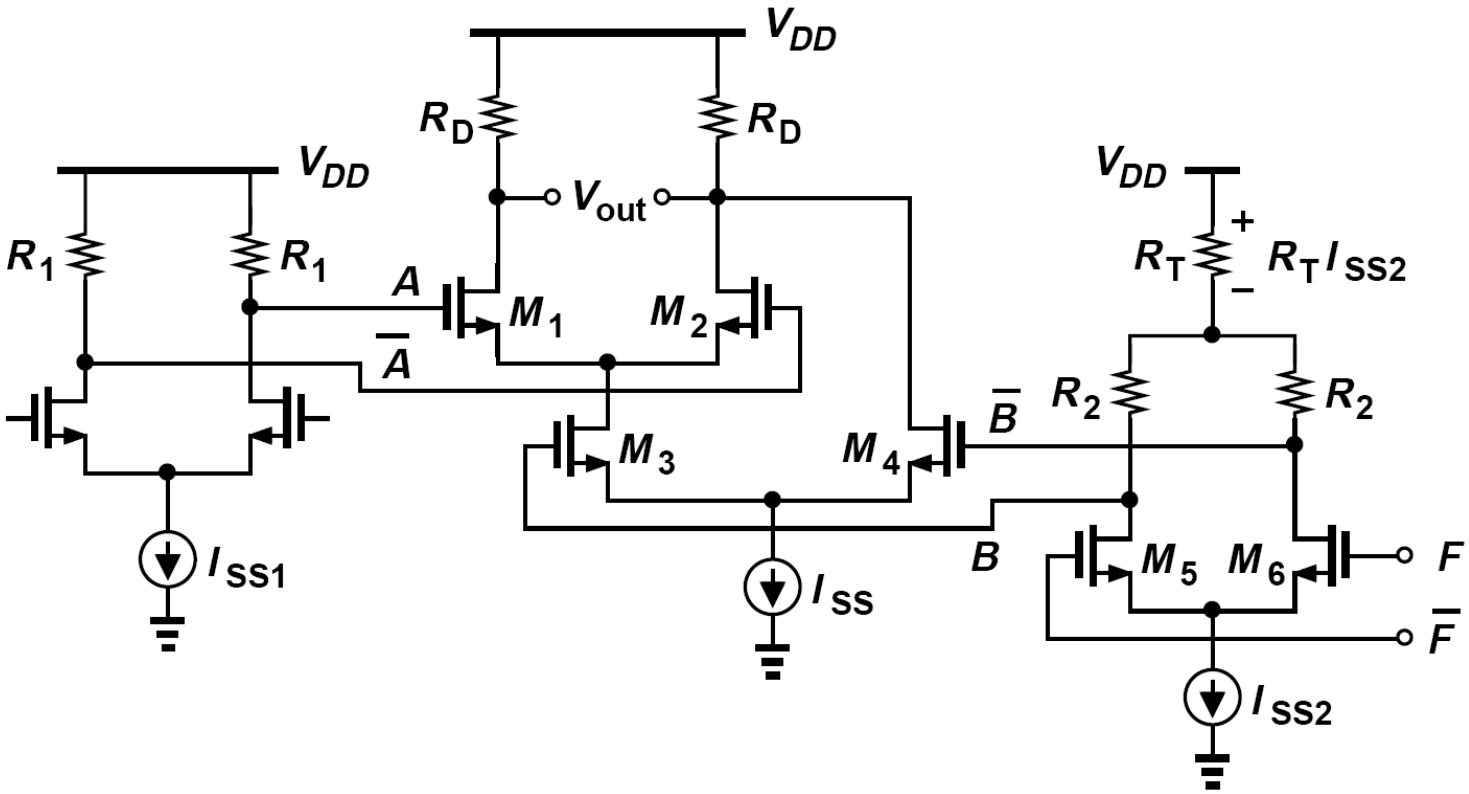






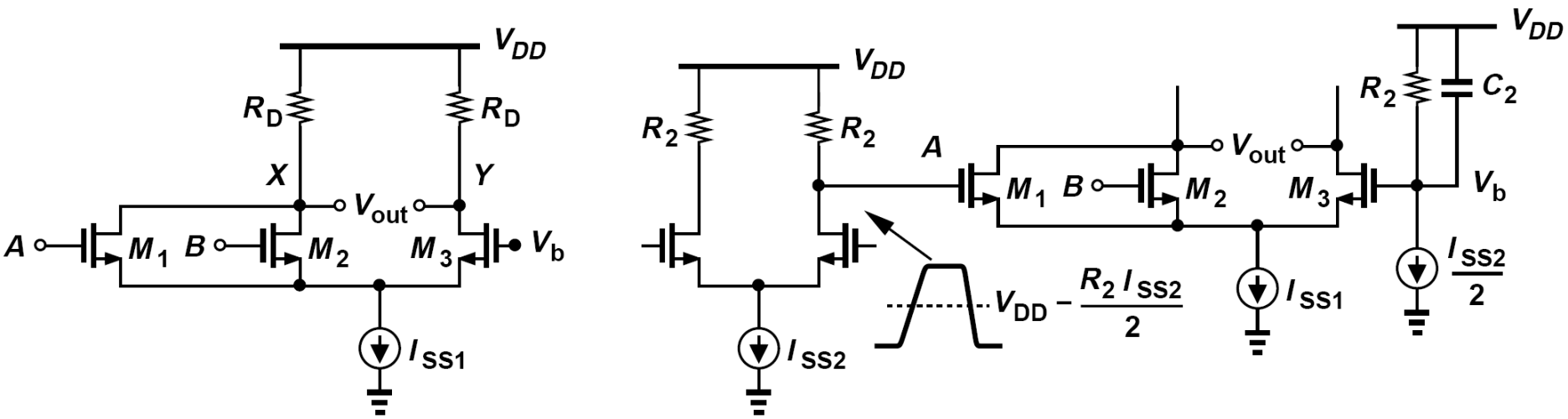
- **CML operates with moderate input and output swings, and provides differential outputs and hence a natural inversion.**
- **The circuit above is typically designed for a single-ended output swing of $R_D I_{SS}$ = 300mV, and the transistors are sized such that they experience complete switching with such input swings**

Problem of Common-Mode Compatibility at NAND Inputs



- **NAND gate is preceded by two representative CML stages.**
- **R_T shifts the CM level of B and $\overline{B}$ by $R_T I_{SS2}$. The addition of R_T appears simple, but now the high level of F and $\overline{F}$ is constrained if M_5 and M_6 must not enter the triode region**

Choice at Low Supply Voltages

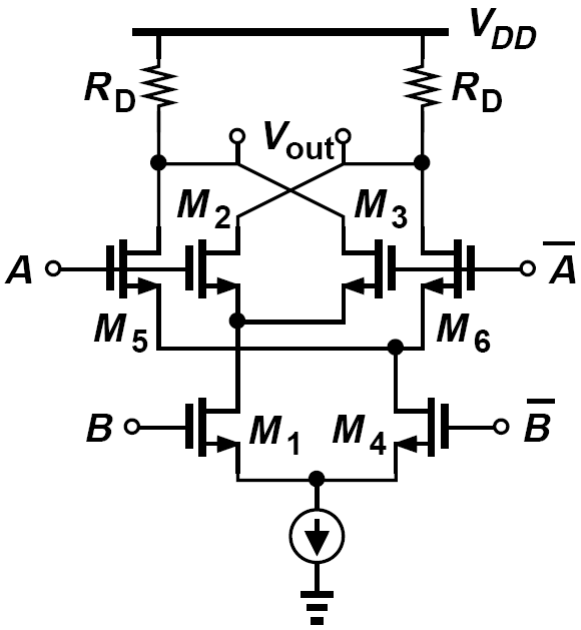


- **The CML NOR/OR gate, avoid stacking. This stage operates only with single-ended inputs.**

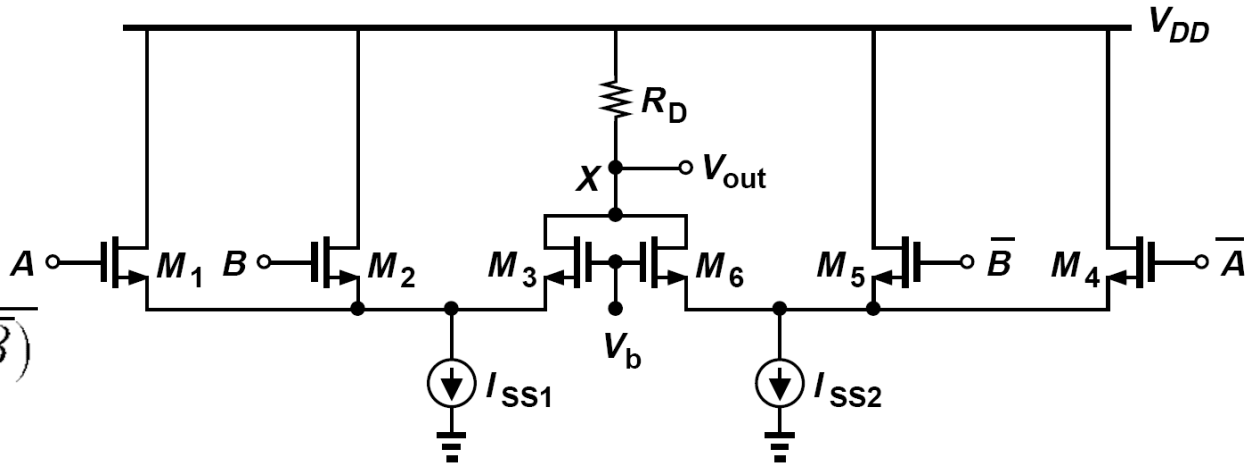
Should M_1-M_3 in figure above have equal widths?

One may postulate that, if both M_1 and M_2 are on, they operate as a single transistor and absorb all of I_{SS1}, i.e., W_1 and W_2 need not exceed $W_3/2$. However, the worst case occurs if only M_1 or M_2 is on. Thus, for either transistor to "overcome" M_3, we require that $W_1 = W_2 \geq W3$.

CML XOR Implementation



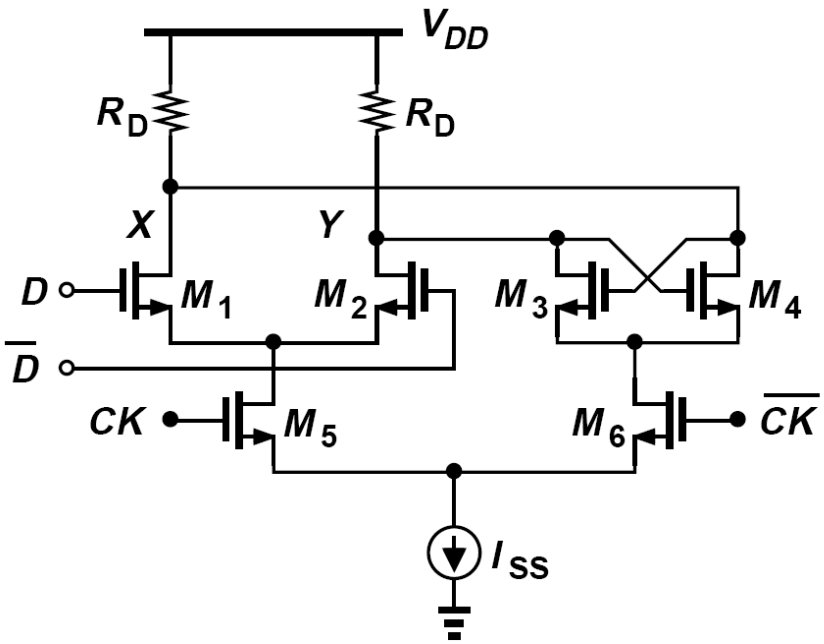
- **The topology is identical to the Gilbert cell mixer. As with the CML NAND gate, this circuit requires proper CM level shift and does not easily operate with low supply voltages.**

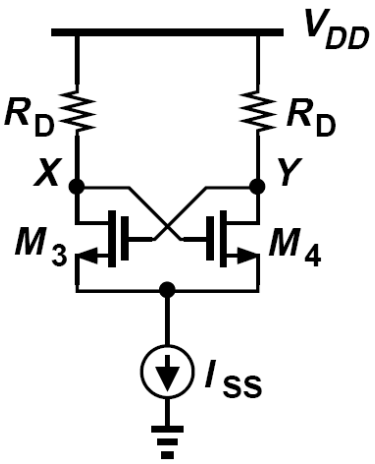


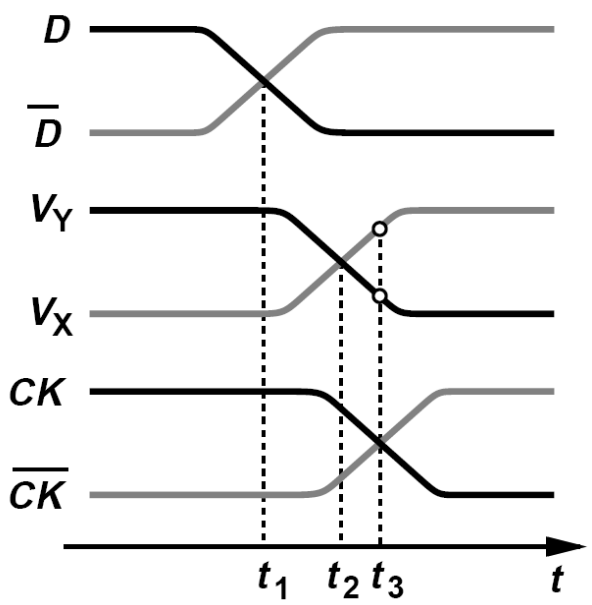
$$V_{out} = \overline{(\overline{A+B}+\overline{A}+\overline{B})}$$
$$= \overline{A}B + A\overline{B}.$$

- **While lending itself to low supply voltage, this topology senses each of the inputs in single-ended form, facing issues similar to those of the NOR gate.**

Speed Attributes of CML Latch





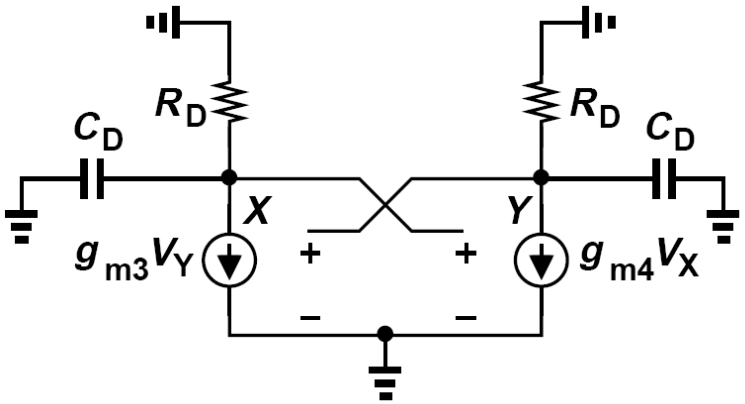


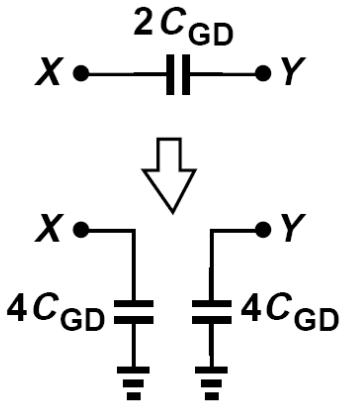
- **Speed advantage of CML circuits is especially pronounced in latches.**
- **The latch operates properly even with a limited bandwidth at *X* and *Y* if (a) in the sense mode V_X and V_Y begin from their full levels and cross, and (b) in the latch mode, the initial difference between V_X and V_Y can be amplified to a final value of $I_{SS}R_D$**

Example to Formulate Regenerative Amplification (I)

Formulate the regenerative amplification of the above circuit in regeneration mode if V_X - V_Y begins with an initial value of V_{XY0}.

Solution:



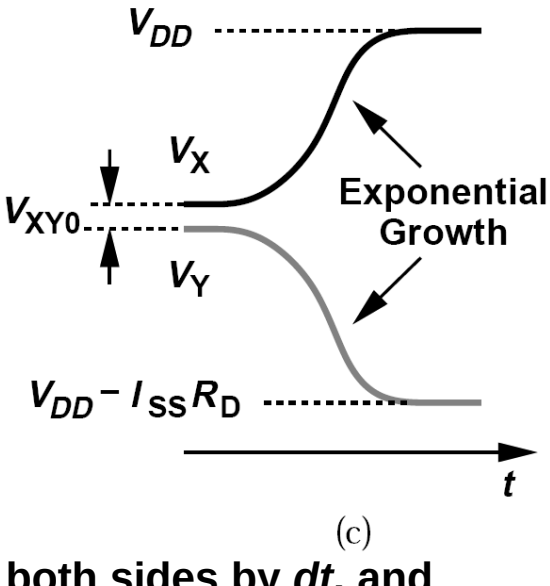


If V_{XY0} is small, M_3 and M_4 are near equilibrium and the small-signal equivalent circuit can be constructed as shown above. Here, C_D represents the total capacitance seen at X and Y to ground, including $C_{GD1} + C_{DB1} + C_{GS3} + C_{DB3} + 4C_{GD3}$ and the input capacitance of the next stage. The gate-drain capacitance is multiplied by a factor of 4 because it arises from both M_3 and M_4 and it is driven by differential voltages. Writing a KCL at node X gives

$$\frac{V_X}{R_D} + C_D\frac{dV_X}{dt} + g_{m3,4}V_Y = 0$$

Example to Formulate Regenerative Amplification (Ⅱ)

Similarly, $$\frac{V_Y}{R_D} + C_D\frac{dV_Y}{dt} + g_{m3,4}V_X = 0$$



Subtracting and grouping the terms, we have

$$-R_DC_D\frac{d(V_X - V_Y)}{dt} = (1 - g_{m3,4}R_D)(V_X - V_Y)$$

We denote V_X - V_Y by V_{XY} , divide both sides by $-R_DC_DV_{XY}$, multiply both sides by dt, and integrate with the initial condition V_{XY} (t = 0) = V_{XY0}. Thus,

$$V_{XY} = V_{XY0}\exp\frac{(g_{m3,4}R_D - 1)t}{R_DC_D}$$

Interestingly, V_{XY} grows exponentially with time, exhibiting a "regeneration time constant" of

$$\tau_{reg} = \frac{R_DC_D}{g_{m3,4}R_D - 1}$$

Of course, as V_{XY} increases, one transistor begins to turn off and its g_m falls toward zero. Note that, if $g_{m3,4}R_D >> 1$, then $\tau_{reg} \approx C_D/g_{m3,4}$.

Example to Derive Relation Between Circuit Parameters and Clock Period

Suppose the *D* latch of the CML latch must run with a minimum clock period of T_{ck}, spending half of the period in each mode. Derive a relation between the circuit parameters and T_{ck}. Assume the swings in the latch mode must reach at least 90% of their final value.

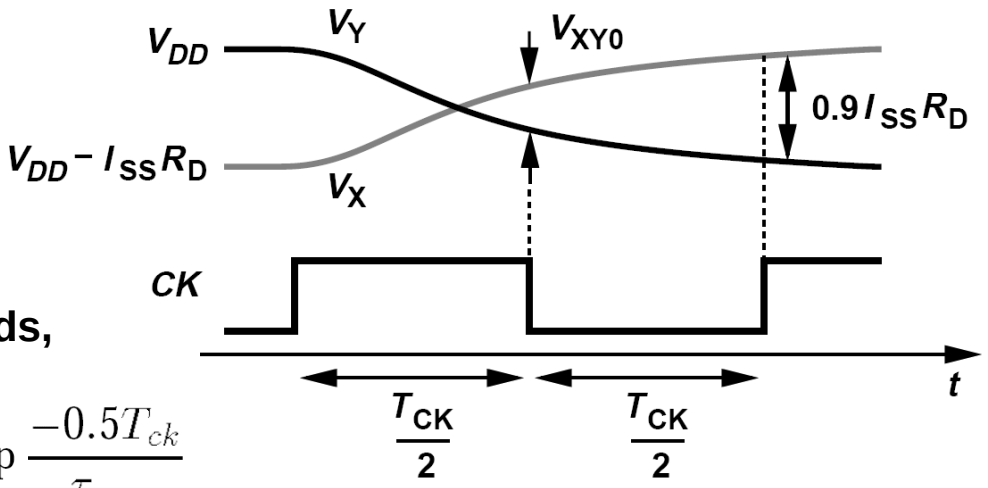
Initial voltage difference

$$V_{XY0} = 0.9 I_{SS} R_D \exp \frac{0.5T_{ck}}{\tau_{reg}}$$

The minimum initial voltage must be established by the input differential pair in the sense mode [just before t = t3]. In the worst case, when the sense mode begins, V_X and V_Y are at the opposite extremes and must cross and reach V_{XY0} in $0.5T_{ck}$ seconds. For example, V_Y begins at V_{DD} and falls according to

$$V_Y(t) = V_{DD} - I_{SS} R_D \left(1 - \exp \frac{-t}{R_D C_D}\right)$$

$$V_X(t) = V_{DD} - I_{SS} R_D \exp \frac{-t}{R_D C_D}$$

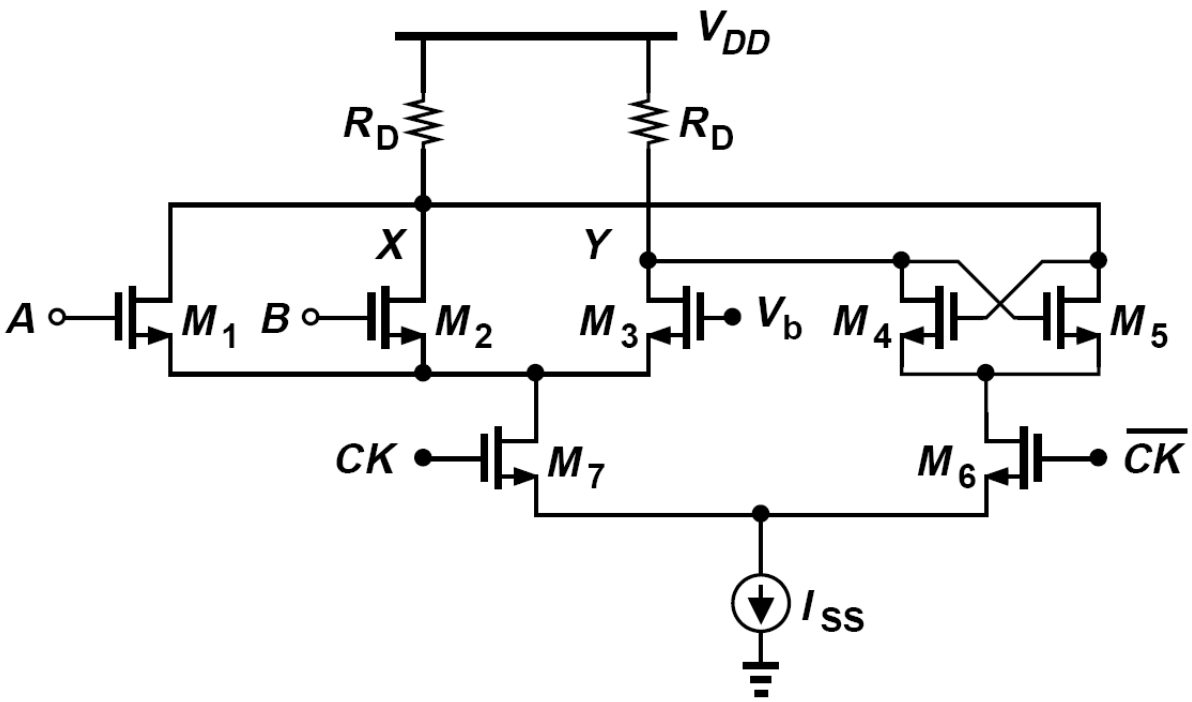


Since V_X - V_Y must reach V_{XY0} in $0.5T_{ck}$ seconds, we have

$$-2 I_{SS} R_D \exp \frac{-0.5T_{ck}}{R_D C_D} + I_{SS} R_D = 0.9 I_{SS} R_D \exp \frac{-0.5T_{ck}}{\tau_{reg}}$$

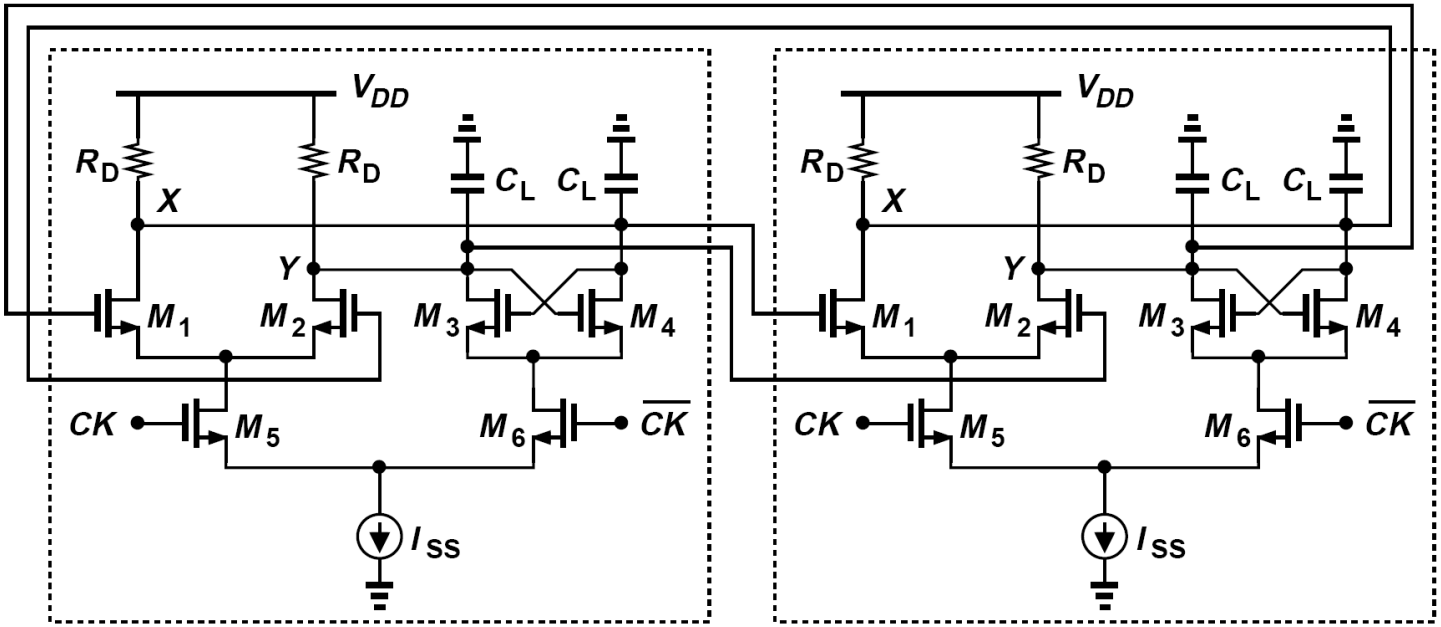
$$0.9 \exp \frac{-0.5T_{ck}}{\tau_{reg}} + 2 \exp \frac{-0.5T_{ck}}{R_D C_D} = 1$$

Merging Logic with Latch



- **It is possible to merge logic with a latch, thus reducing both the delay and the power dissipation. For example, the NOR and the master latch of FF_1 depicted in previous high-speed divide-by-2/3 circuit can be realized as shown above. The circuit performs a NOR/OR operation on *A* and *B* in the sense mode, and stores the result in the latch mode.**

Design Procedure



(1)Select I_{SS} based on the power budget (2)Select $R_D I_{SS} \approx 300$mV

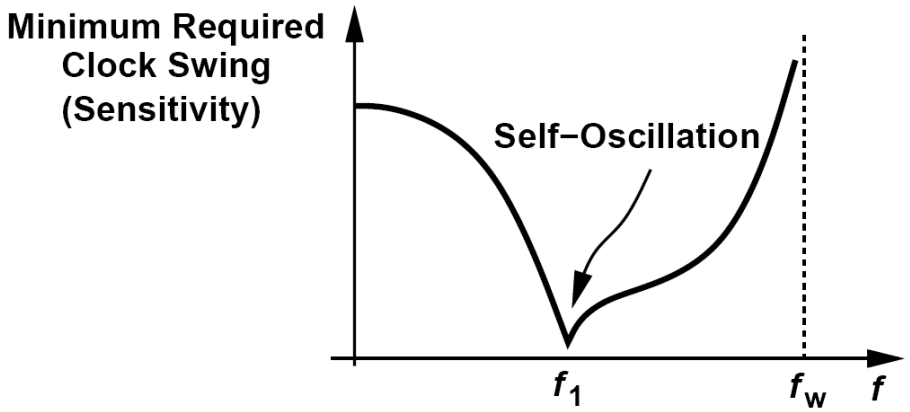
(3)Select $(W/L)_{1,2}$ such that the diff. pair experiences nearly complete switching for a diff. input of 300mV

(4)Select $(W/L)_{3,4}$ so that small-signal gain around regenerative loop exceeds unity

(5)Select $(W/L)_{5,6}$ such that the clocked pair steers most of the tail current with the specified clock swing

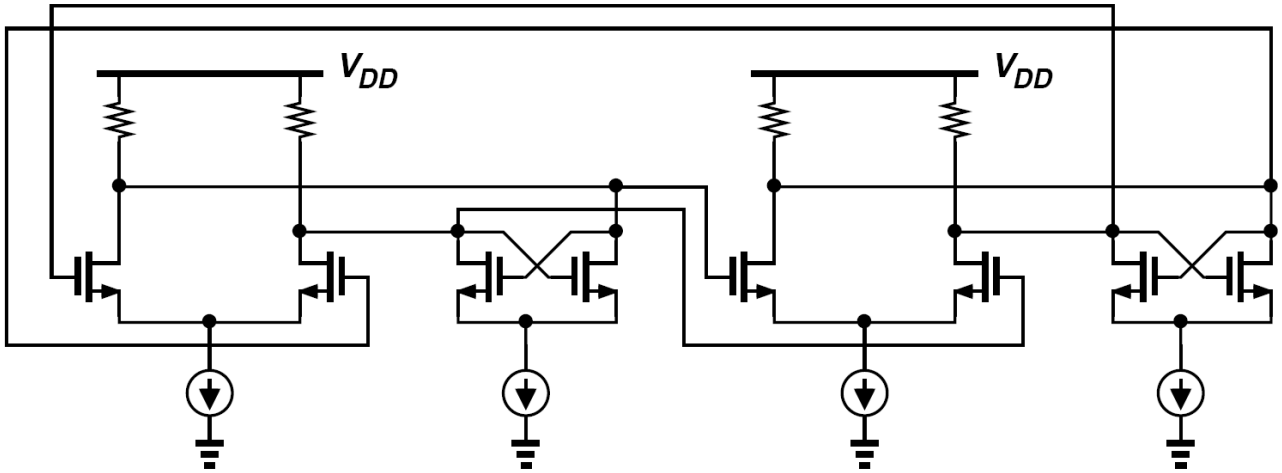
Example of the Sensitivity of the ÷2 Circuit (I)

The performance of high-speed dividers is typically characterized by plotting the minimum required clock voltage swing ("sensitivity") as a function of the clock frequency. Sketch the sensitivity for the ÷ 2 circuit of the figure above.



For a clock with abrupt edges, we expect the required clock swing to remain relatively constant up to the point where the internal time constants begin to manifest themselves. Beyond this point, the required swing must increase. The overall behavior, however, appears as shown in figure above. Interestingly, the required clock swing falls to zero at some frequency, f_1. Since for zero input swings, I_{SS} is simply split equally between M_5 and M_6 in figure above, the circuit reduces to that depicted in the figure below. We recognize that the result resembles a two-stage ring oscillator. In other words, in the absence of an input clock, the circuit simply oscillates at a frequency of $f_1/2$.

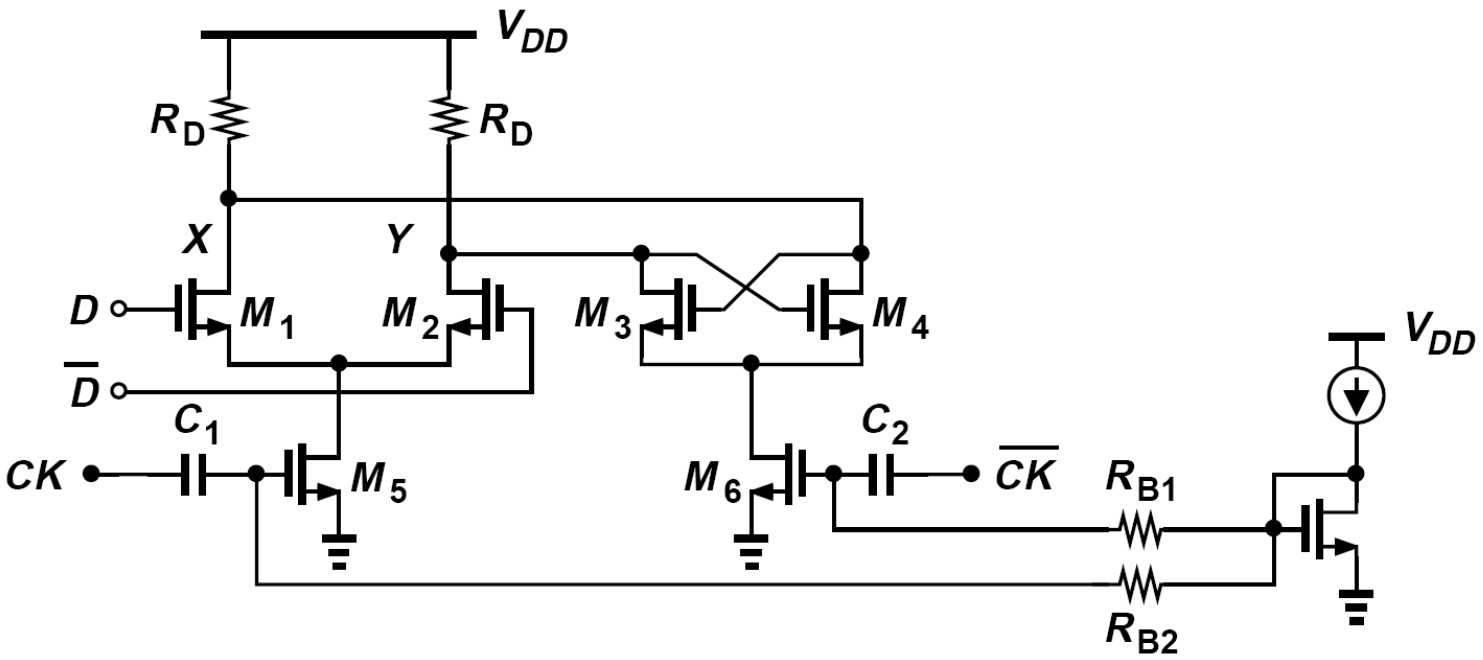
Example of the Sensitivity of the ÷2 Circuit (Ⅱ)



This observation provides another perspective on the operation of the divider: the circuit behaves as an oscillator that is injection-locked to the input clock. This viewpoint also explains why the clock swing cannot be arbitrarily small at low frequencies. Even with square clock waveforms, a small swing fails to steer all of the tail current, thereby keeping M_2-M_3 and M_3-M_4 simultaneously on. The circuit may therefore oscillate at $f_1/2$ (or injection-pulled by the clock).

The "self-oscillation" of the divider also proves helpful in the design process: if the choice of device dimensions does not allow self-oscillation, then the divider fails to operate properly. We thus first test the circuit with a zero clock swing to ensure that it oscillates.

Class-AB Latch

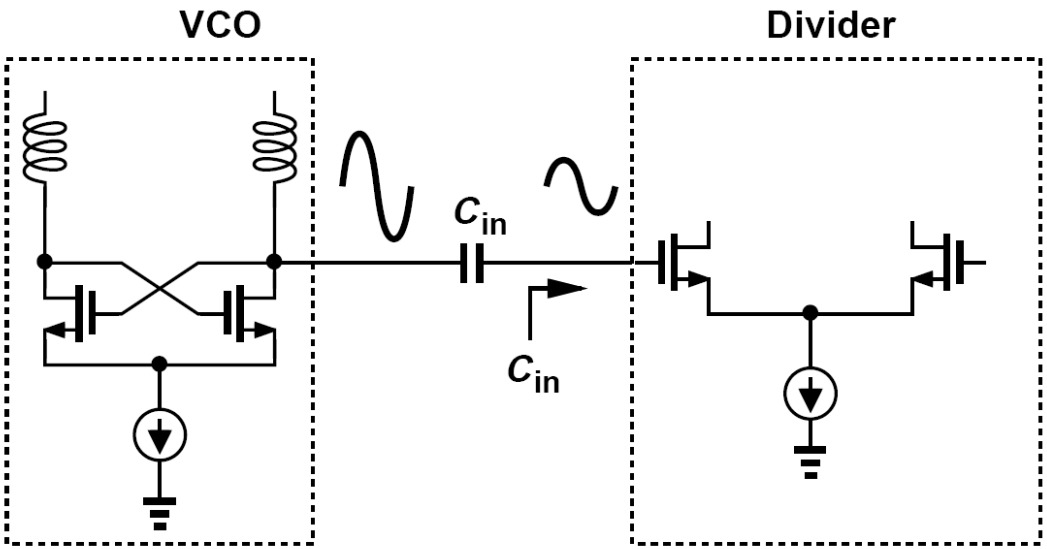


- **The bias of the clocked pair is defined by a current mirror and the clock is coupled capacitively.**
- **Large clock swings allow transistors M_5 and M_6 to operate in the class AB mode, i.e., their peak current well exceed their bias current. This attribute improves the speed of the divider.**

Example of Choosing Coupling Capacitance

A student designs a VCO with relatively large swings to minimize relative phase noise and a CML ÷ 2 circuit that requires only moderate clock swings. How should the coupling capacitors be chosen?

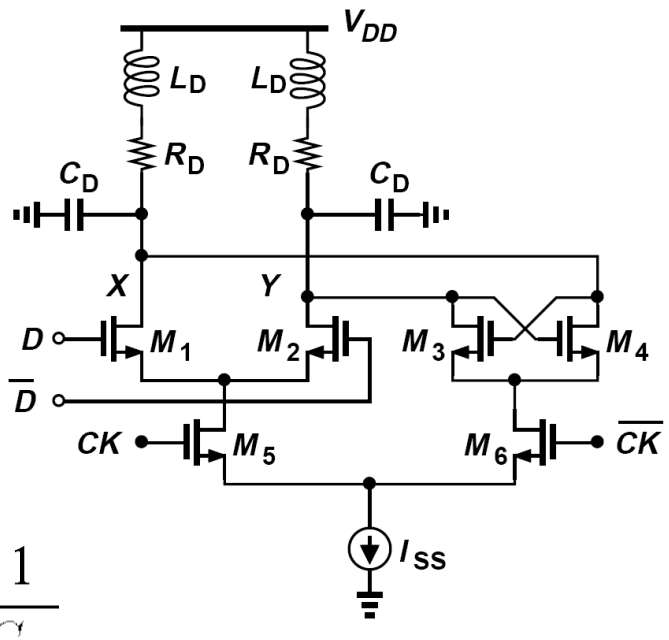
Solution:



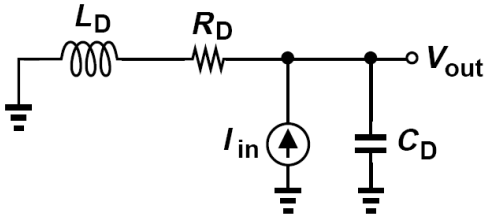
Suppose the VCO output swing is twice that required by the divider. We simply choose each coupling capacitor to be equal to the input capacitance of the divider. This minimizes the size of the coupling capacitors, the load capacitance seen by the VCO (half of the divider input capacitance), and the effect of divider input capacitance variation on the VCO.

CML Using Inductive Peaking

$$\frac{V_{out}}{I_{in}} = \frac{L_D s + R_D}{L_D C_D s^2 + R_D C_D s + 1}$$



(a)



(b)

Rewrite this as

$$\frac{V_{out}}{I_{in}} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \cdot \frac{1}{C_D}$$

where $\zeta = \frac{R_D}{2}\sqrt{\frac{C_D}{L_D}}$ $\qquad \omega_n = \frac{1}{\sqrt{L_D C_D}}$

To determine the -3 dB bandwidth:

$$\frac{\omega_{-3dB}^2 + 4\zeta^2\omega_n^2}{(\omega_{-3dB}^2 - \omega_n^2)^2 + 4\zeta^2\omega_n^2\omega_{-3dB}^2} = \frac{2\zeta^2}{\omega_n^2}$$

It follows that

$$\omega_{-3dB}^2 = \left[-2\zeta^2 + 1 + \frac{1}{4\zeta^2} + \sqrt{\left(-2\zeta^2 + 1 + \frac{1}{4\zeta^2}\right)^2 + 1}\right]\omega_n^2$$

Example of Inductive Peaking

What is the minimum tolerable value of ζ if the frequency response must exhibit no peaking?

Solution:

Peaking occurs if the magnitude of the transfer function reaches a local maximum at some frequency. Taking the derivative of the magnitude squared of the transfer function with respect to *ω* and setting the result to zero, we have

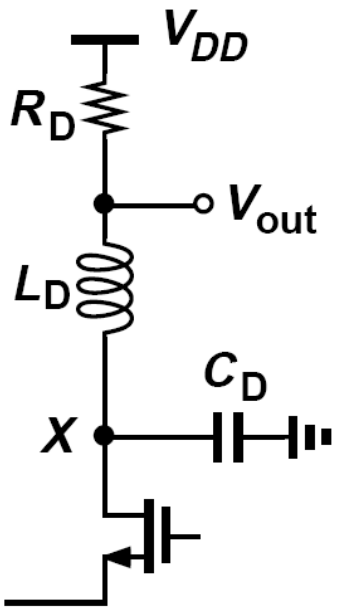
$$\omega^4 + 8\zeta^2\omega_n^2\omega^2 + [4\zeta^2(4\zeta^2 - 2) - 1]\omega_n^4 = 0$$

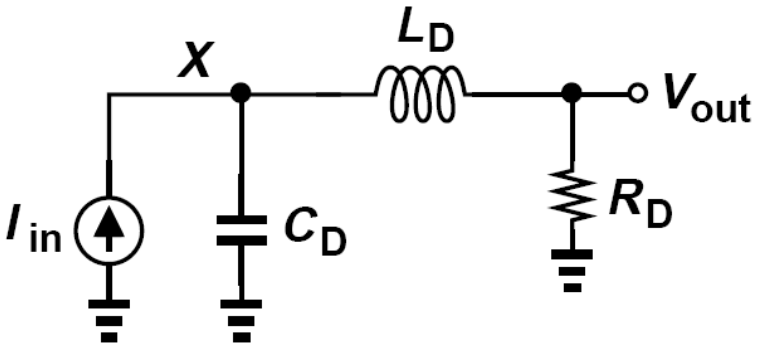
A solution exists if $-4\zeta^2 + \sqrt{8\zeta^2 + 1} \geq 0$

And hence if $\zeta \geq \sqrt{\frac{1+\sqrt{2}}{4}} \approx 0.78$

This bound on ζ translates to $\omega_{-3dB} \leq \frac{1.73}{R_D C_D}$

Series Peaking





$$\frac{V_{out}}{I_{in}}(s) = \frac{R_D}{L_D C_D s^2 + R_D C_D s + 1}$$

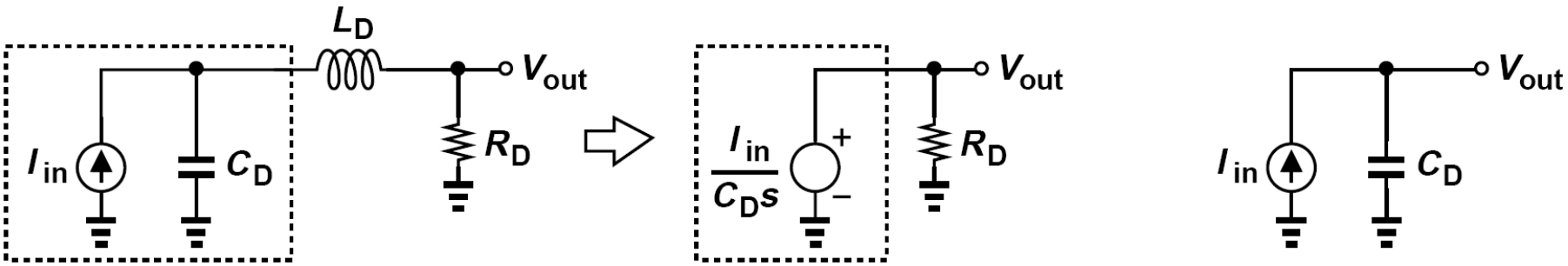
The -3 dB bandwidth is computed as

$$\omega^2_{-3dB} = [-(2\zeta^2 - 1) + \sqrt{(2\zeta^2 - 1)^2 + 1}]\omega_n^2,$$

- **Series peaking increases the bandwidth by about 40%**

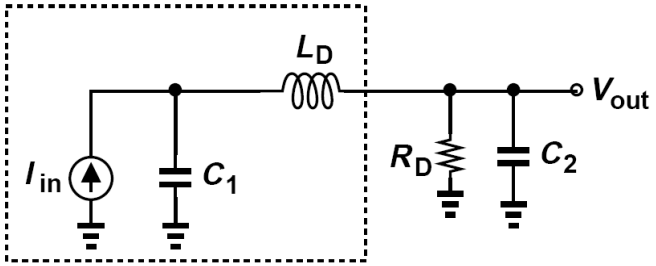
Example of Series Peaking

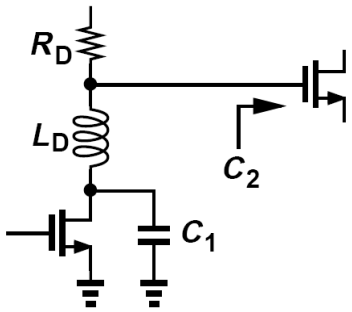
Having understood shunt peaking intuitively, a student reasons that series peaking degrades the bandwidth because, at high frequencies, inductor L_D in figure above impedes the flow of current, forcing a larger fraction of I_{in} to flow through C_D. Since a smaller current flows though L_D and R_D, V_{out} falls at higher frequencies. Explain the flaw in this argument.

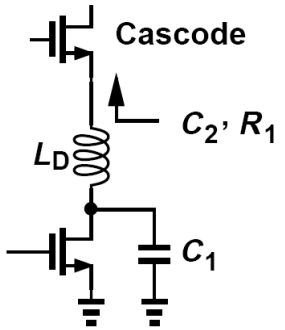


Let us study the behavior of the circuit at $\omega_n = 1/\sqrt{L_D C_D}$. As shown above, the Thevenin equivalent of I_{in}, C_D, and L_D is constructed by noting that (a) the open-circuit output voltage is equal to $I_{in}/(C_D s)$, and (b) the output impedance (with I_{in} set to zero) is zero because C_D and L_D resonate at ω_n. It follows that $V_{out} = I_{in}/(C_D s)$ at $\omega = \omega_n$, i.e., as if the circuit consisted of only I_{in} and C_D. Since I_{in} appears to flow entirely through C_D, it yields a larger magnitude for V_{out} than if it must split between C_D and R_D.

Series Peaking Circuit Driving Load Capacitance

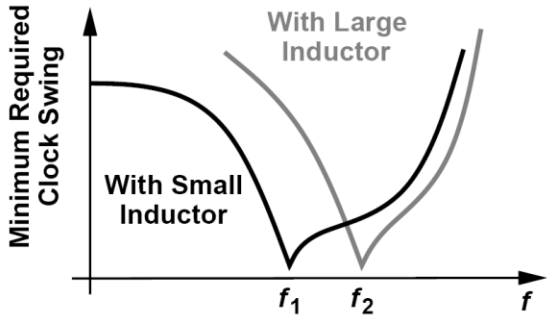


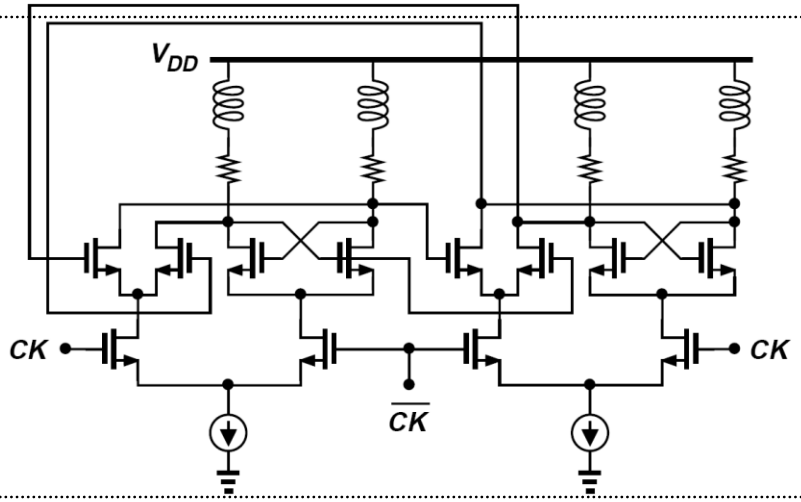




- **Compared to shunt peaking, series peaking typically requires a smaller inductor value**

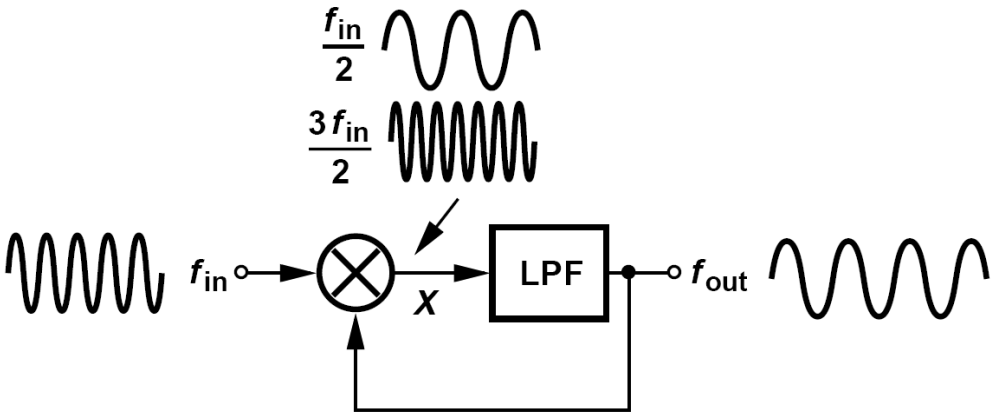
What Happens if Load Inductor Increase?

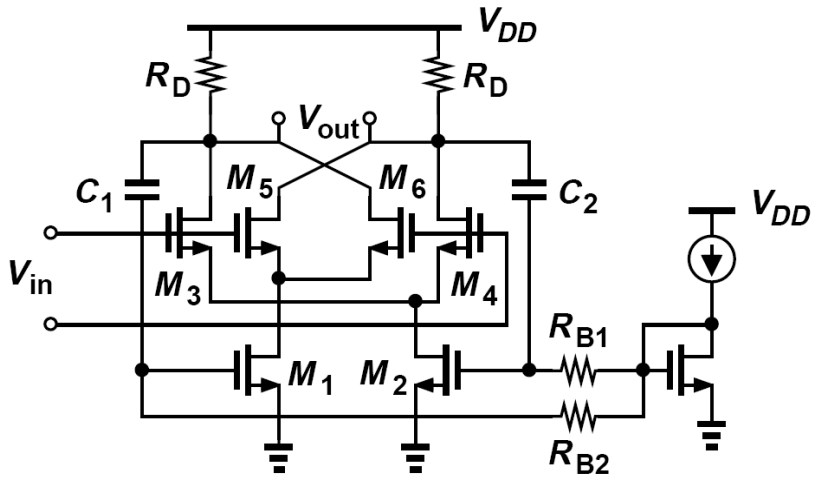




- **As the value of L_D becomes large enough, the circuit begins to fail at low frequencies. This is because the circuit approaches a quadrature LC oscillator that is injection-locked to the input clock**

Miller Divider



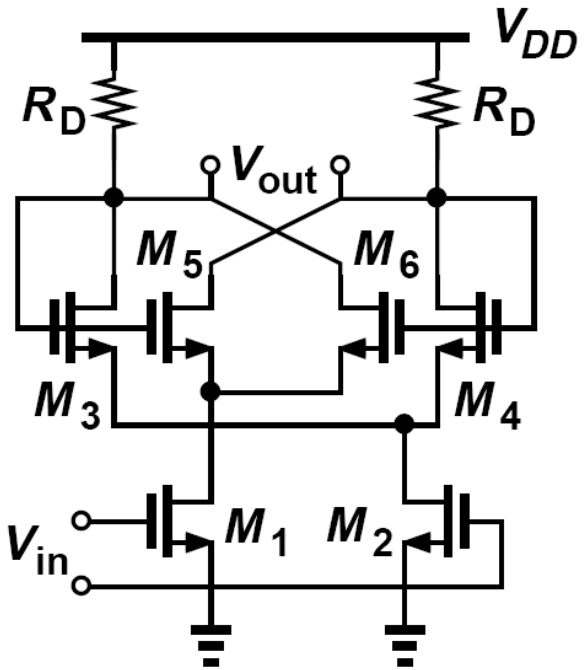


- **If the required speed exceeds that provided by CML circuits, one can consider the "Miller divider", also known as the "dynamic divider"**
- **The Miller divider can achieve high speeds for two reasons: (1) the low-pass behavior can simply be due to the intrinsic time constant at the output node of the mixer and (2) the circuit does not rely on latching and hence fails more gradually than flipflops as the input frequency increases**

Example of Miller Divider with Feedback

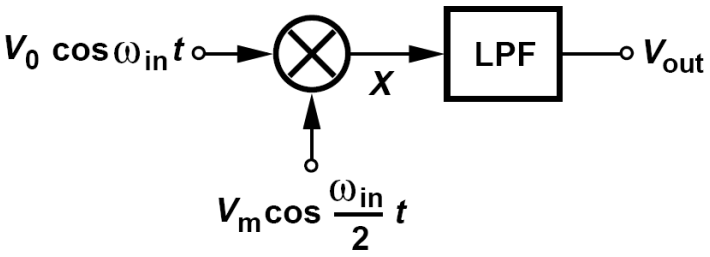
Is it possible to construct a Miller divider by returning the output to the LO port of the mixer?

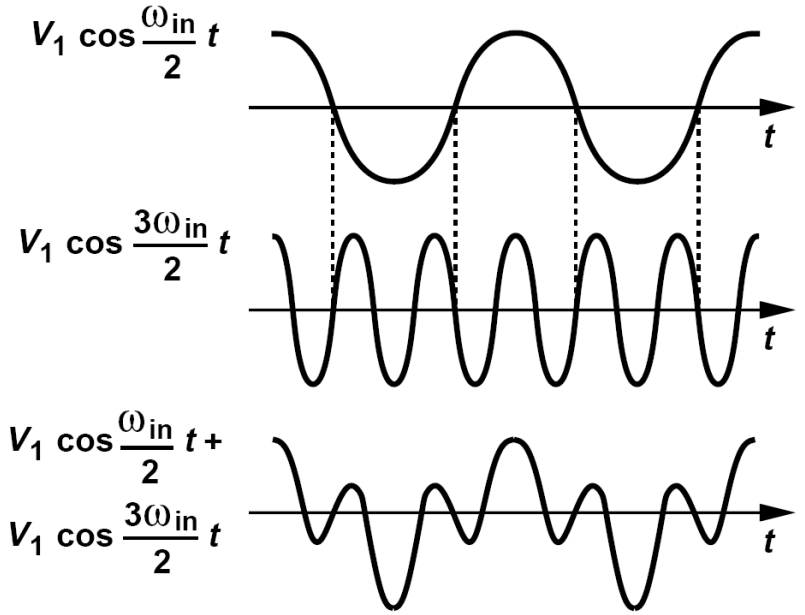
Solution:



Shown above, such a topology senses the input at the RF port of the mixer. (Strangely enough, M_3 and M_4 now appear as diode-connected devices.) We will see below that this circuit fails to divide.

Why the Component at $3f_{in}/2$ Must be Sufficiently Small?





$$V_X(t) = \alpha(V_0 \cos \omega_{in} t)\left(V_m \cos \frac{\omega_{in} t}{2}\right)$$
$$= \frac{\alpha V_0 V_m}{2}\left(\cos \frac{\omega_{in} t}{2} + \cos \frac{3\omega_{in} t}{2}\right)$$

- **This sum exhibits additional zero crossings, prohibiting frequency division if traveling through the LPF unchanged.**

Example of Miller Divider Using First-order Low-pass Filter

Does the arrangement shown below operate as a divider?

Since the voltage drop across R_1 is equal to $R_1C_1dV_{out}/dt$, we have $V_X = R_1C_1dV_{out}/dt + V_{out}$. Also, $V_X = \alpha V_{in}V_{out}$. If $V_{in} = V_0 \cos \omega_{in}t$, then

$$R_1C_1\frac{dV_{out}}{dt} + V_{out} = \alpha(V_0\cos\omega_{in}t)V_{out}$$

It follows that

$$R_1C_1\frac{dV_{out}}{V_{out}} = (\alpha V_0\cos\omega_{in}t - 1)dt$$

We integrate the left-hand side from V_{out0} (initial condition at the output) to V_{out} and the right-hand side from 0 to t:

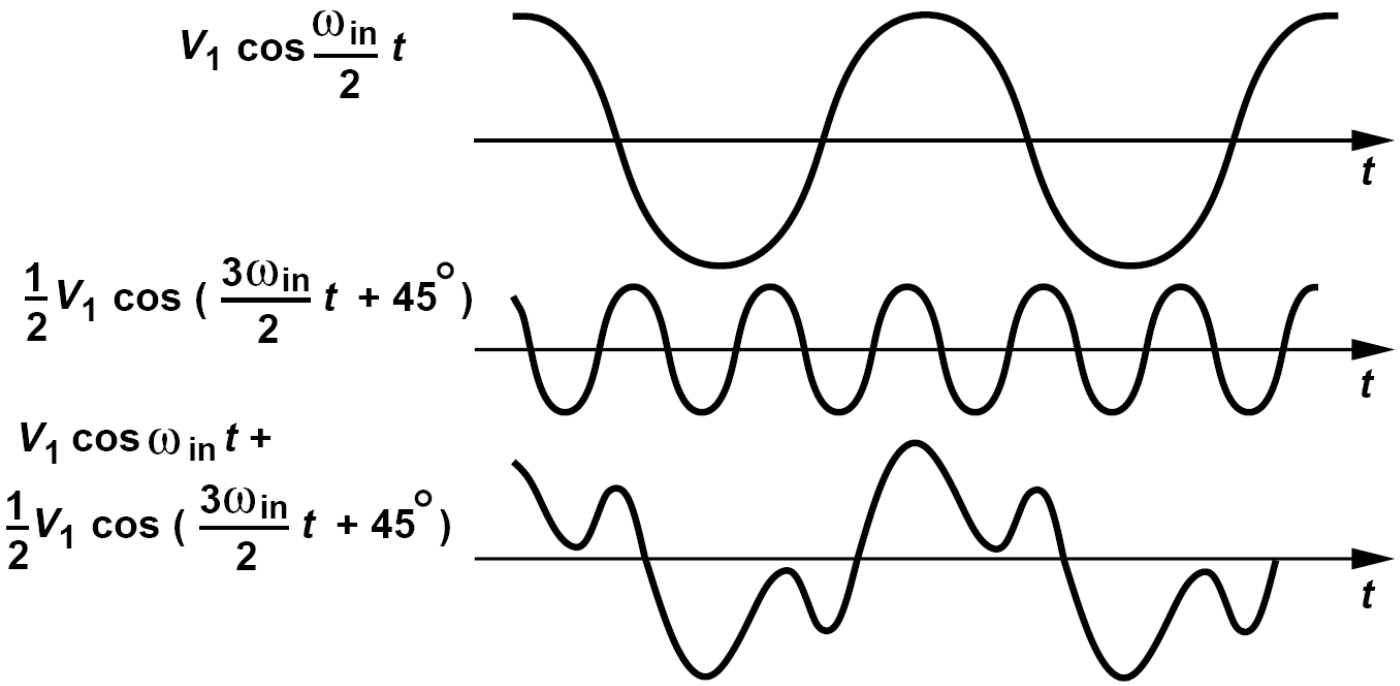
$$R_1C_1\ln\frac{V_{out}}{V_{out0}} = \frac{1}{\omega_{in}}\alpha V_0\sin\omega_{in}t - t$$

Thus

$$V_{out}(t) = V_{out0}\exp\left(\frac{-t}{R_1C_1} + \frac{\alpha V_0}{R_1C_1\omega_{in}}\sin\omega_{in}t\right)$$

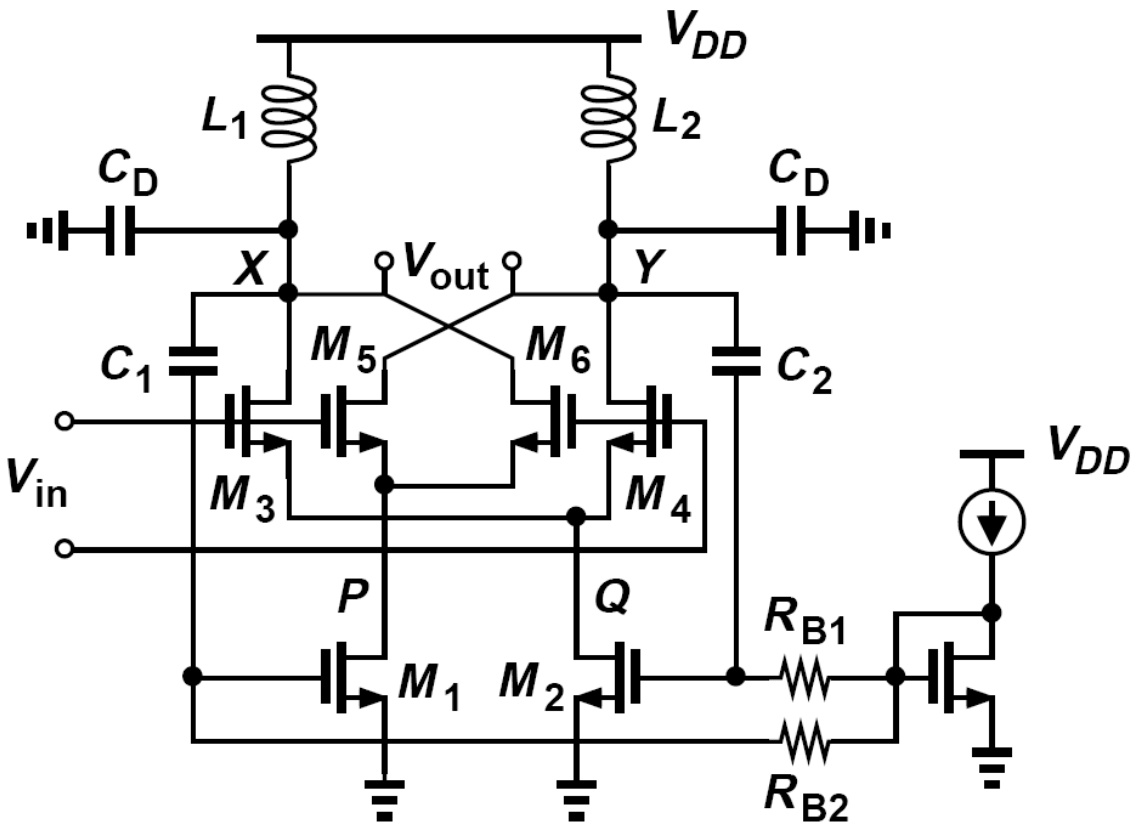
Interestingly, the exponential term drives the output to zero regardless of the values of α or ω_{in} . The circuit fails because a one-pole filter does not sufficiently attenuate the third harmonic with respect to the first harmonic. An important corollary of this analysis is that the topology of Miller divider with feedback to switching quad cannot divide: the single-pole loop does not adequately suppress the third harmonic at the output.

Introducing Phase Shift in Miller Divider



- **The Miller divider operates properly if the third harmonic is attenuated and shifted so as to avoid the additional zero crossings.**

Miller Divider with Inductive Load



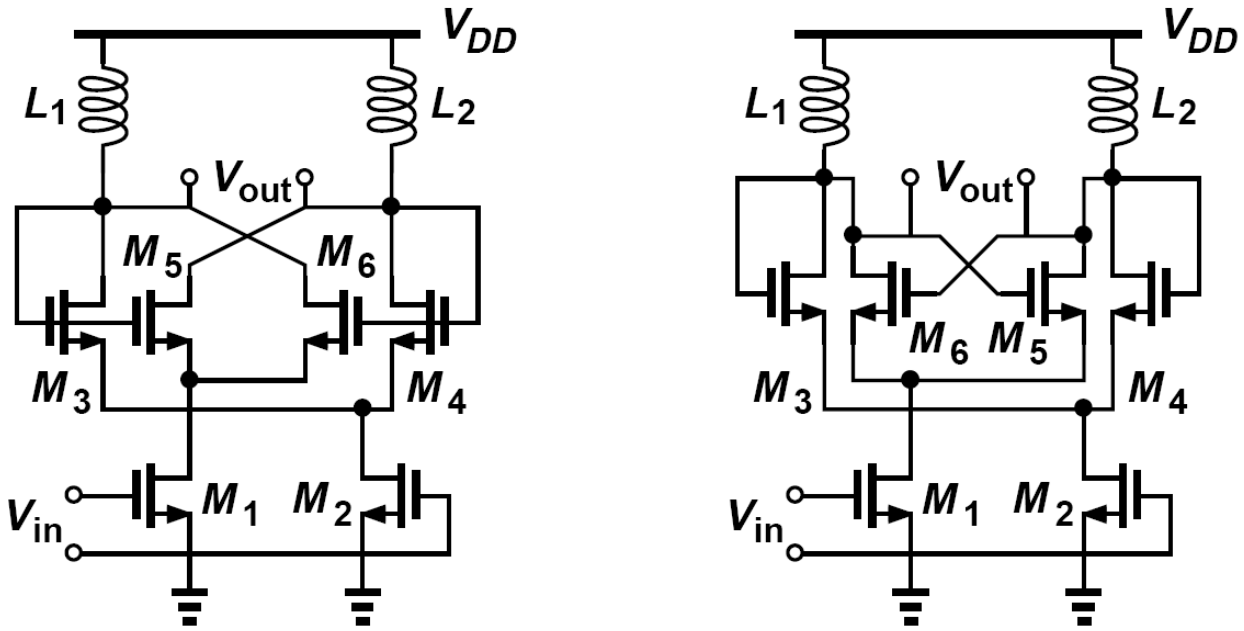
The input frequency range across which the circuit operates properly is given by

$$\Delta\omega = \frac{2\omega_0}{Q}\left(\frac{2}{\pi}g_{m1,2}R_p\right)^2$$

- **If the load resistors are replaced with inductors, the gain-headroom and gain-speed trade-offs are greatly relaxed, but the lower end of the frequency range rises. Also the inductor complicates the layout.**

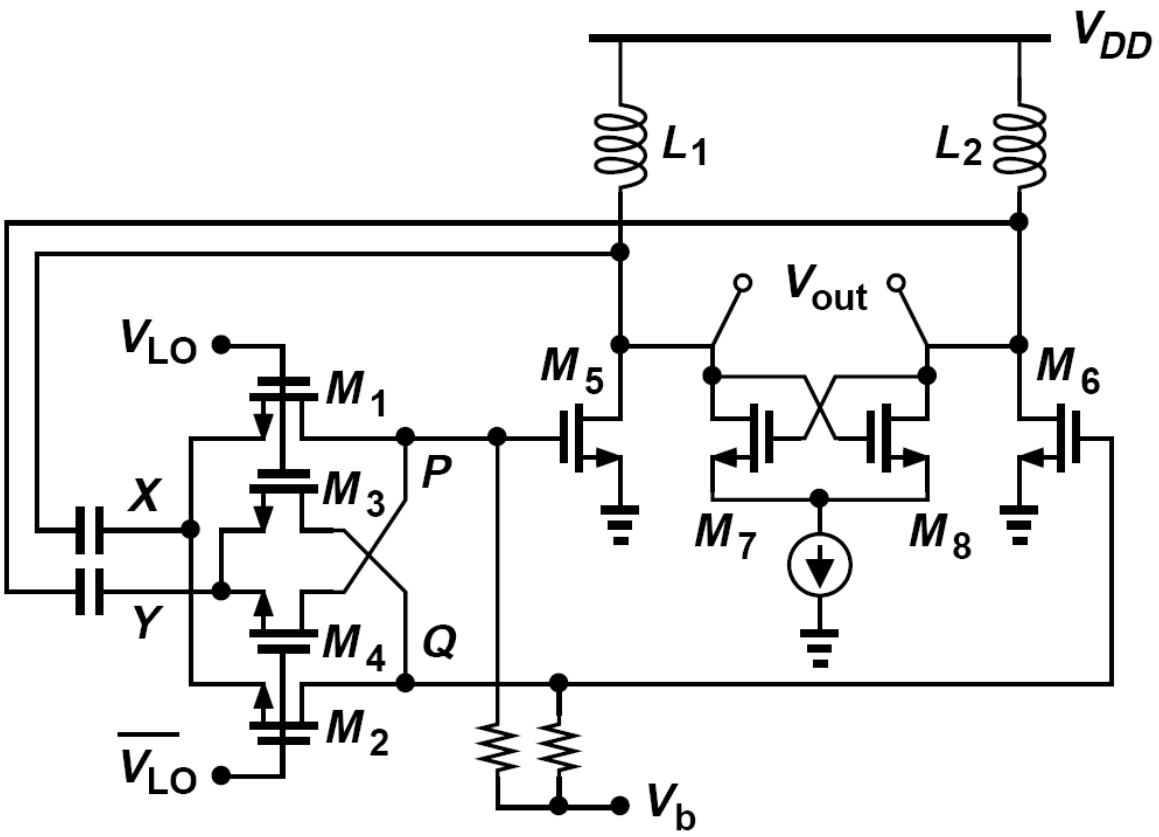
Example of Miller Divider with Inductive Loads

Does the previous Miller divider with feedback to switching quad operate as a divider if the load resistors are replaced with inductors?



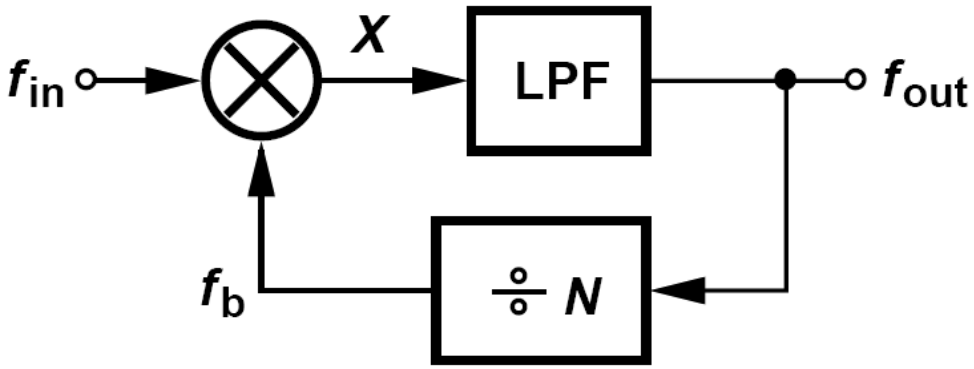
Depicted above left, such an arrangement in fact resembles an oscillator. Redrawing the circuit as shown right, we note M_5 and M_6 act as a cross-coupled pair and M_3 and M_4 as diode-connected devices. In other words, the oscillator consisting of M_5-M_6 and L_1-L_2 is heavily loaded by M_3-M_4, failing to oscillate (unless the Q of the tank is infinite or M_3 and M_4 are weaker than M_5 and M_6). This configuration does operate as a divider but across a narrower frequency range.

Miller Divider with Passive Mixers



- **Since the output CM level is near V_{DD}, the feedback path incorporates capacitive coupling, allowing the sources and drains of M_1-M_4 to remain about 0.4V above the ground. The cross-coupled pair M_7-M_8 can be added to increase the gain by virtue of its negative resistance.**

Miller Divider with Other Moduli

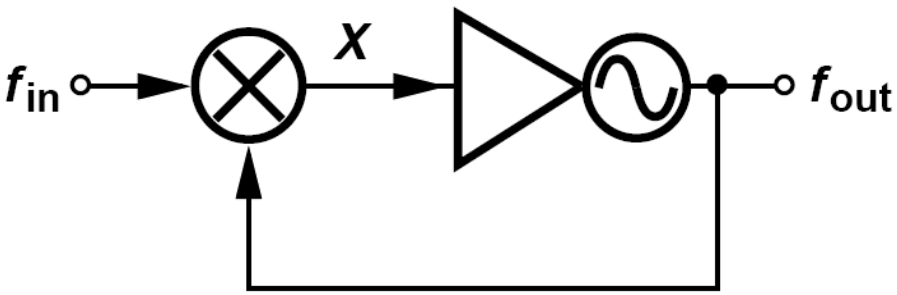


A $\div N$ circuit in the feedback path creates $f_b = f_{out}/N$, yielding $f_{in} \pm f_{out}/N$ at X. If the sum is suppressed by the LPF, then $f_{out} = f_{in} - f_{out}/N$ and hence

$$f_{out} = \frac{N}{N+1} f_{in} \qquad f_b = \frac{1}{N+1} f_{in}$$

- **The sum component at X comes closer to the difference component as N increases, dictating a sharper LPF roll-off.**
- **Another critical issue relates to the port-to-port feedthroughs of the mixer**

Injection-Locked Dividers



- Based on oscillators that are injection-locked to a harmonic of their oscillation frequency
- If f_{in} varies across a certain "lock range", the oscillator remains injection-locked to the f_{out}-f_{in} component at node *X*

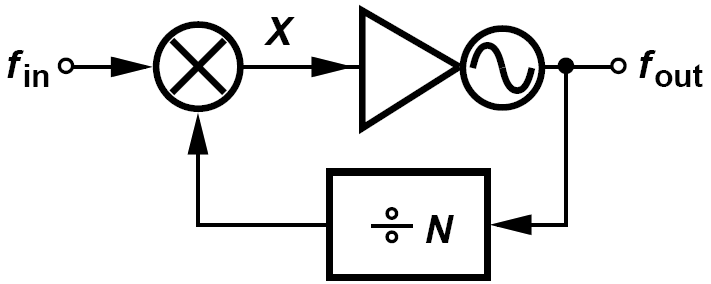
Determine the divide ratio of the topology shown below if the oscillator remains locked.

The mixer yields two components at node *X*, namely, $f_{in} - f_{out}/N$ and $f_{in} + f_{out}/N$. If the oscillator locks to the former, then $f_{in} - f_{out}/N = f_{out}$ and hence

$$f_{out} = \frac{N}{N+1} f_{in}$$

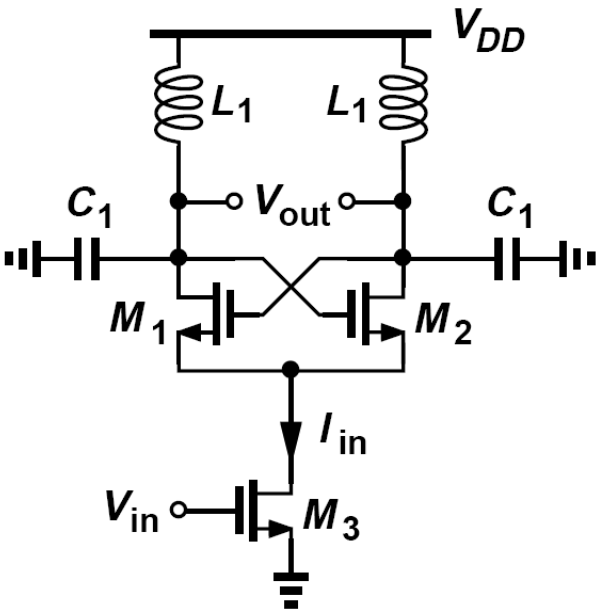
Similarly, if the oscillator locks to the latter then

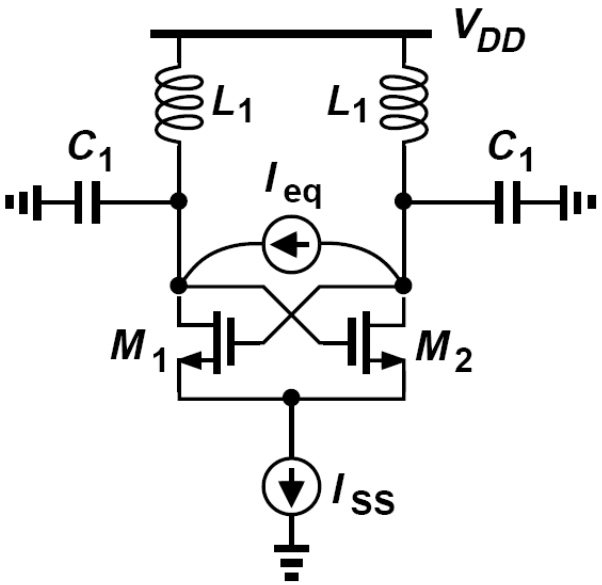
$$f_{out} = \frac{N}{N-1} f_{in}$$



The oscillator lock range must therefore be narrow enough to lock to only one of the two components.

Implementation of ILD





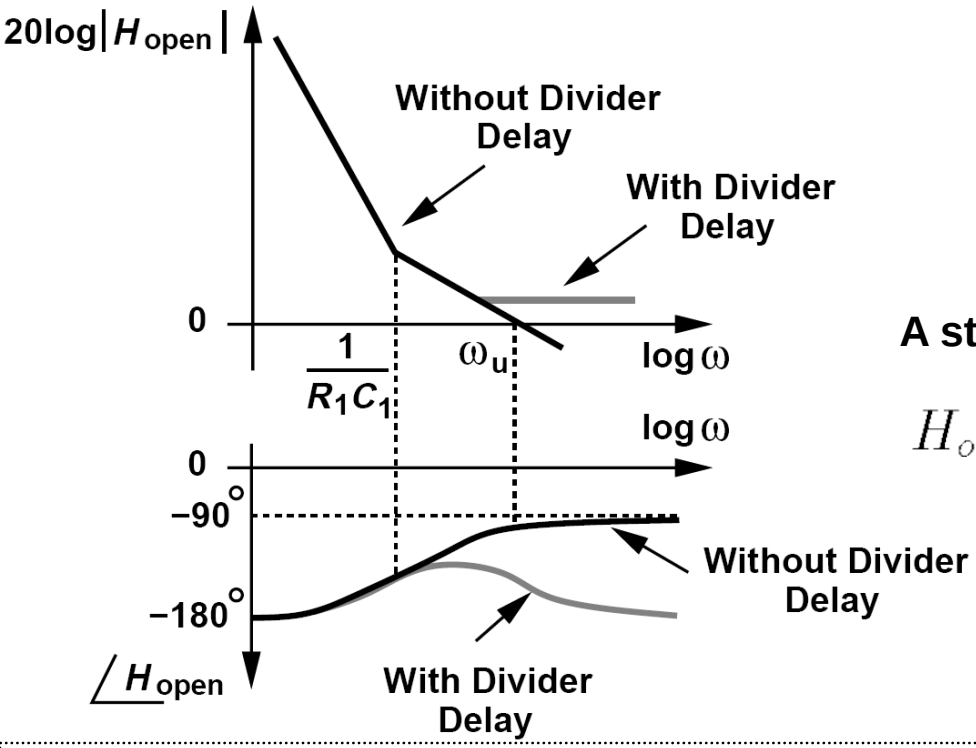
The output frequency range across which the circuit remains locked is given by

$$\Delta\omega_{out} = \frac{\omega_0}{Q}\left(\frac{2}{\pi}\frac{I_{in}}{I_{osc}}\right)$$

The input lock range is twice this value:

$$\Delta\omega_{in} = \frac{\omega_0}{Q}\left(\frac{4}{\pi}\frac{I_{in}}{I_{osc}}\right)$$

Divider Delay and Phase Noise: Effect of Divider Delay



A stage with a constant delay of ΔT

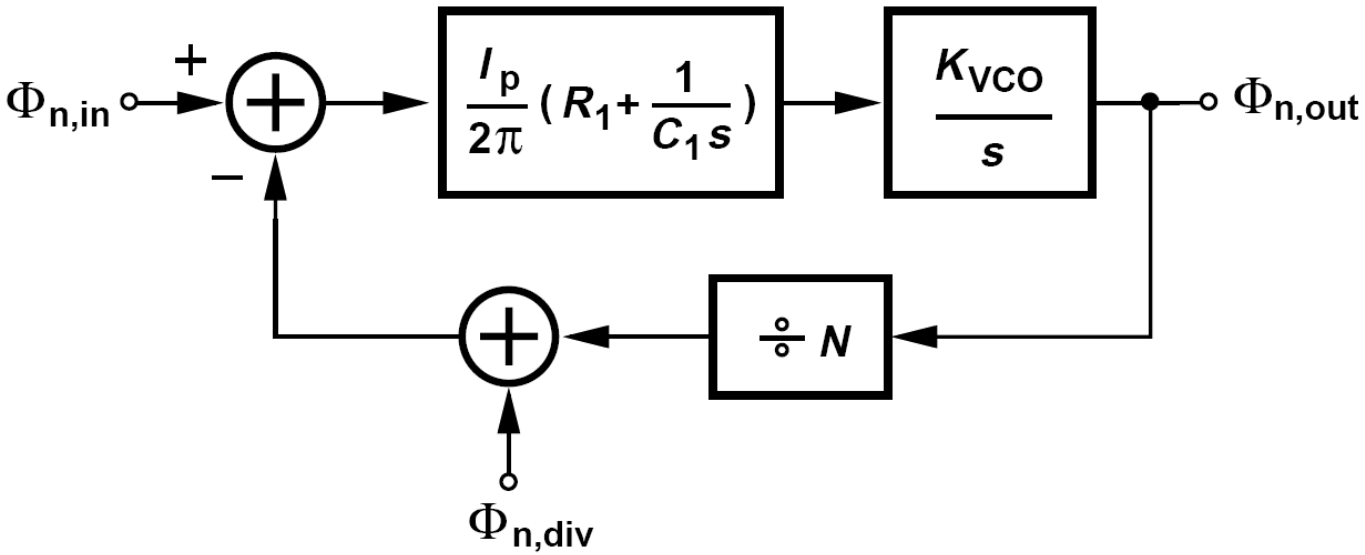
$$H_{open}(s) = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_1 s}\right)\frac{K_{VCO}}{NS}e^{-\Delta T \cdot s}.$$

- **The zero has two undesirable effects: it flattens the gain, pushing the gain crossover frequency to higher values (in principle, infinity), and it bends the phase profile downward.**

This zero must remain well above the original unity-gain bandwidth of the loop:

$$\begin{aligned}\frac{1}{\Delta T} &\approx 5\omega_u \\ &\approx 5(2\zeta^2 + \sqrt{4\zeta^4+1})\omega_n^2\end{aligned}$$

Effect of Divider Phase Noise

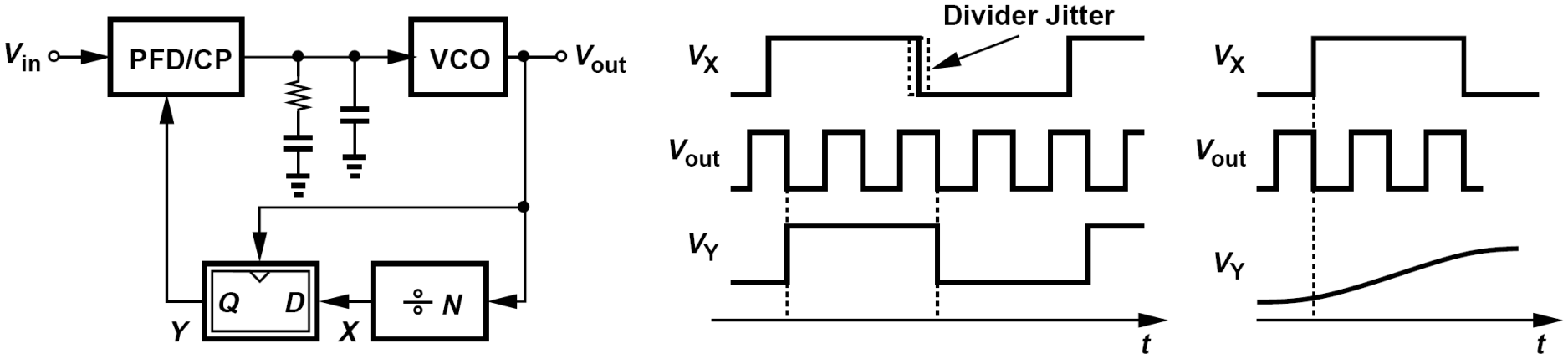


- **The output phase noise of the divider directly adds to the input phase noise, experiencing the same low-pass response as it propagates to ϕ_{out}. In other words, $\phi_{n,div}$ is also multiplied by a factor of N within the loop bandwidth.**

For the divider to contribute negligible phase noise, we must have

$$\phi_{n,div} \ll \phi_{n,in}$$

Use of Retiming FF to Remove Divider Phase Noise



- **If the divider phase noise is significant, a retiming flipflop can be used to suppress its effect.**
- **In essence, the retiming operation bypasses the phase noise accumulated in the divider chain.**

Examples of Retiming to Remove Divider Phase Noise

Compare the output phase noise of the above circuit with that of a similar loop that employs noiseless dividers and no retiming flipflop. Consider only the input phase noise.

Solution:

The phase noise is similar. Invoking the time-domain view, we note that a (slow) displacement of the input edges by ΔT seconds still requires that the edges at Y be displaced by ΔT, which is possible only if the VCO edges are shifted by the same amount.

Does the retiming operation in figure above remove the effect of the divider delay?

Solution:

No, it does not. An edge entering the divider still takes a certain amount of time before it appears at X and hence at Y . In fact, figure above indicates that V_Y is delayed with respect to V_X by at most one VCO cycle. That is, the overall feedback delay is slightly longer in this case.

Integer-N Synthesis Drawbacks

- **Improved resolution always comes at the expense of reduced update rate (ii.e. lower f_{ref})**
- **Lower update rate →lower bandwidth**
- **Larger contribution of the VCO phase noise → larger power**
- **Large settling time → increase channel switching times**
- **Need: Large bandwidth and fine frequency resolution**
  - **Fractional-N Synthesis**

References (I)

[1] S. E. Meninger and M. H. Perrott, "A 1-MHz Bandwidth 3.6-GHz 0.18-μm CMOS Fractional-N Synthesizer Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise," *IEEE J. Solid-State Circuits,* vol. 41, pp.966-981, April 2006.

[2] K. J. Wang, A. Swaminathan, and I. Galton, "Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional-N PLL," *IEEE J. of Solid-State Circuits,* vol. 43, pp. 2787-2797, Dec. 2008.

[3] A. Zolfaghari, A. Y. Chan, and B. Razavi, "A 2.4-GHz 34-mW CMOS Transceiver for Frequency-Hopping and Direct-Sequence Applications," *ISSCC Dig. Tech. Papers,* pp. 418-419, Feb. 2001.

[4] G. Irvine et al, "An Upconversion Loop Transmitter IC for Digital Mobile Telephones," *ISSCC Dig. Tech. Papers,* pp. 364-365, Feb. 1998.

[5] T. Yamawaki et al, "A 2.7-V GSM RF Transceiver IC," *IEEE J. of Solid-State Circuits,* vol. 32, pp. 2089-2096, Dec. 1997.

[6] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology," *IEEE J. of Solid-State Circuits,* vol. 35, pp. 788-794, May 2000.

References (Ⅱ)

[7] C. S. Vaucher, et al, "A Family of Low-Power Truly Modular Programmable Dividers in Standard 0.35-μm CMOS Technology," *IEEE J. of Solid-State Circuits,* vol. 35, pp. 1039-1045, July 2000.

[8] B. Razavi, Y. Ota, and R. G. Swartz, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," *IEEE J. of Solid-State Circuits,* vol. 29, pp.332-339, March 1994.

[9] J. Lee and B. Razavi, "A 40-Gb/s clock and data recovery circuit in 0.18-μm CMOS technology," *IEEE J. of Solid-State Circuits,* vol. 38, pp. 2181-2190, Dec. 2003.

[10] D. D. Kim, K. Kim, and C. Cho, "A 94GHz Locking Hysteresis-Assisted and Tunable CML Static Divider in 65nm SOI CMOS," *ISSCC Dig. Tech. Papers,* pp. 460-461, Feb. 2008.

[11] J. Yuan and C. Svensson, "High-Speed CMOS Circuit Technique," *IEEE J. Solid-State Circuits,* vol. 24, pp. 62-70, Feb. 1989.

[12] B. Chang, J. Park, and W. Kim, "A 1.2-GHz CMOS Dual-Modulus Prescaler Using New Dynamic D-Type Flip-Flops," *IEEE J. Solid-State Circuits,* vol. 31, pp. 749-754, May 1996.

References (Ⅲ)

[13] R. L. Miller, "Fractional-frequency generators utilizing regenerative modulation, " *Proc. IRE,* vol. 27, pp. 446-456, July 1939.

[14] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-μm CMOS technology," *IEEE J. of Solid-State Circuits,* vol. 39, pp. 594-601, Apr. 2004.

[15] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. of Solid-State Circuits,* vol. 34, pp. 813-821, June 1999.

[16] B. Razavi, "A Millimeter-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider," *IEEE J. of Solid-State Circuits,* vol. 43, pp. 477-485, Feb. 2008.

[17] C.-C. Lin and C.-K. Wang, "A regenerative semi-dynamic frequency divider for mode-1 MB-OFDM UWB hopping carrier generation," *ISSCC Dig. Tech. Papers,* pp. 206-207, Feb. 2005.

[18] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. of Solid-State Circuits,* vol. 39, pp. 1415-1424, Sep. 2004.

References

1. B. Razavi, “RF Microelectronics,” 2nd Ed., Prentice Hall, 2012.
2. S. Palermo, ECEN620: Network Theory and Broadband Circuit Design 2012, TAMU.
3. P. Hanumolu, ECE 599, OSU.