



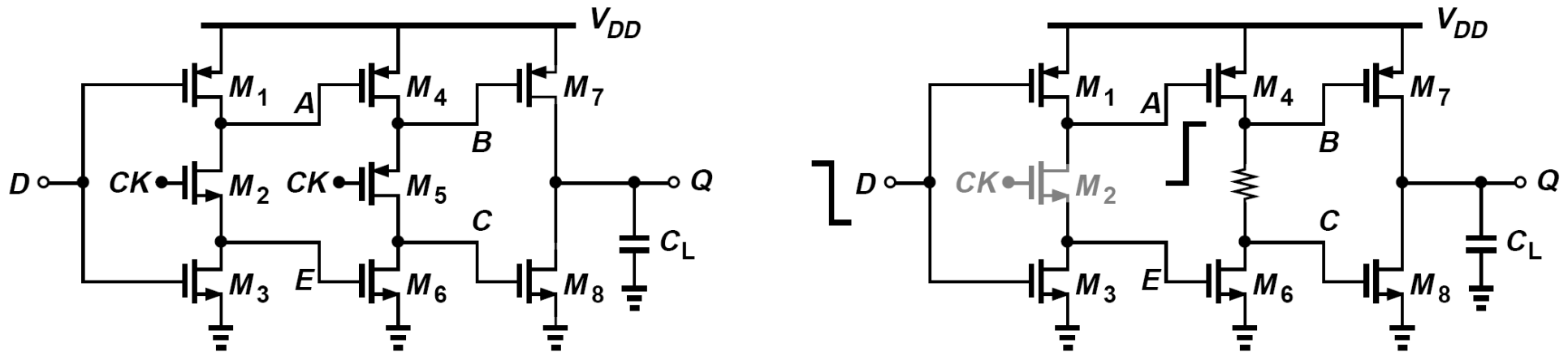
# **ECE518 Memory/Clock Synchronization IC Design**

## **Clock Divider Circuits**

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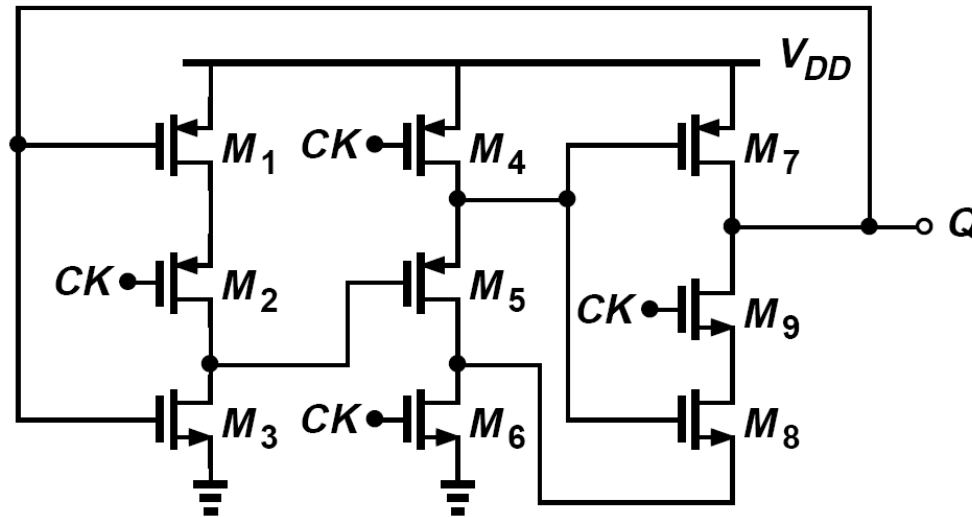
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# True Single-Phase Clocking (TSPC)



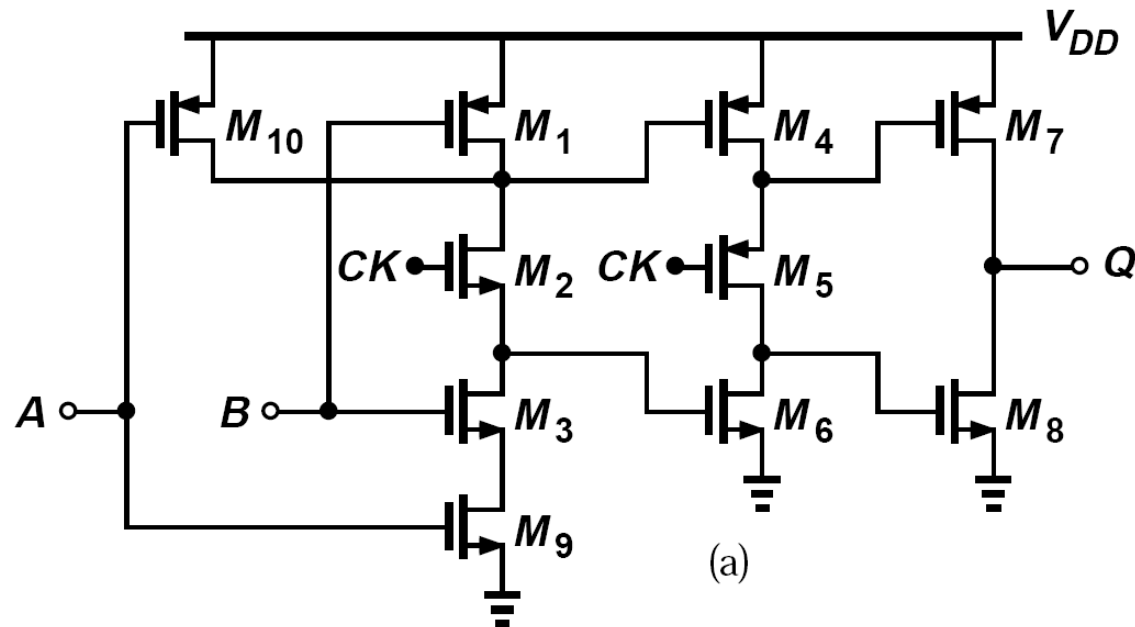
- When  $CK$  is high, the first stage operates as an inverter, impressing  $\bar{D}$  at  $A$  and  $E$ . When  $CK$  goes low, the first stage is disabled and the second stage becomes transparent, writing  $\bar{A}$  at  $B$  and  $C$  and hence making  $Q$  equal to  $A$ . The logical high at  $E$  and the logical low at  $B$  are degraded but the levels at  $A$  and  $C$  ensure proper operation of the circuit.

# TSPC Divide-by-2 Circuit



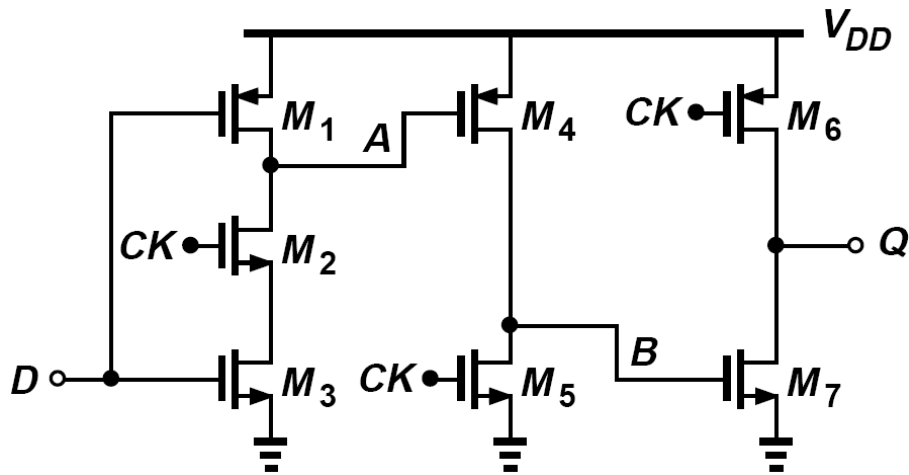
- This topology achieves relatively high speeds with low power dissipation, but requires rail-to-rail clock swings for proper operation.
- The circuit consumes no static power and as a dynamic logic topology, the divider fails at very low clock frequencies due to the leakage of the transistors.

# TSPC ÷2 Incorporating a NAND Gate



- A NAND gate can be merged with the master latch.
- In the design of TSPC circuit, one observes that wider clocked devices raises the maximum speed, but at the cost of loading the preceding stage.

# TSPC Using Ratioed Logic



➤ The slave latch is designed as “ratioed” logic, achieving higher speeds.

The first stage in figure above is not completely disabled when  $CK$  is low. Explain what happens if  $D$  changes in this mode.

**Solution:**

If  $D$  goes from low to high,  $A$  does not change. If  $D$  falls,  $A$  rises, but since  $M_4$  turns off, it cannot change the state at  $B$ . Thus,  $D$  does not alter the state stored by the slave latch.

# References

1. B. Razavi, "RF Microelectronics," 2<sup>nd</sup> Ed., Prentice Hall, 2012.