Homework 6

ECE 5/404 – PLL and High-Speed Link Design

Note: Use Cadence schematic capture and Spectre simulation tools, available on the ENGR servers for the homework problems. Use TSMC 180nm models with $V_{DD} = 1.8\,V$.

Problem 1- PFD Design

Design a transistor-level implementation of a PFD working at $f_{ref} = 100\,MHz$ with a minimum PFD output pulse width of at least $100\,ps$.

1. Show the transistor-level schematic and simulations showing the minimum PFD pulse width specification is satisfied.
2. Plot the phase transfer characteristic over a phase range of $\pm 4\pi$ (*Use your test-bench from HW3*).

This exercise should help you design the PFD for the course project.