

# Homework 5

## ECE 5/404 – PLL and High-Speed Link Design

**Note:** Use Cadence schematic capture and Spectre simulation tools, available on the AMS servers for the homework problems. Use TSMC 180 nm models with  $V_{DD} = 1.8\text{ V}$ .

### Problem 1- Ring VCO Design

Design a voltage-controlled oscillator (VCO) to generate frequencies in the range  $f_{out} = 100 - 500\text{ MHz}$ . Use any suitable ring-based topology for your design.

1. Show the VCO voltage tuning curve ( $f_{out}$  vs  $V_{control}$ ) and find the linearized VCO gain  $K_{VCO}$ .
2. Simulate the changes in the VCO tuning curve as the voltage supply ( $V_{DD}$ ) is varied.
3. Plot the phase noise contribution of the VCO.