ECE518 Memory/Clock Synchronization IC Design

PFD Circuit Implementation

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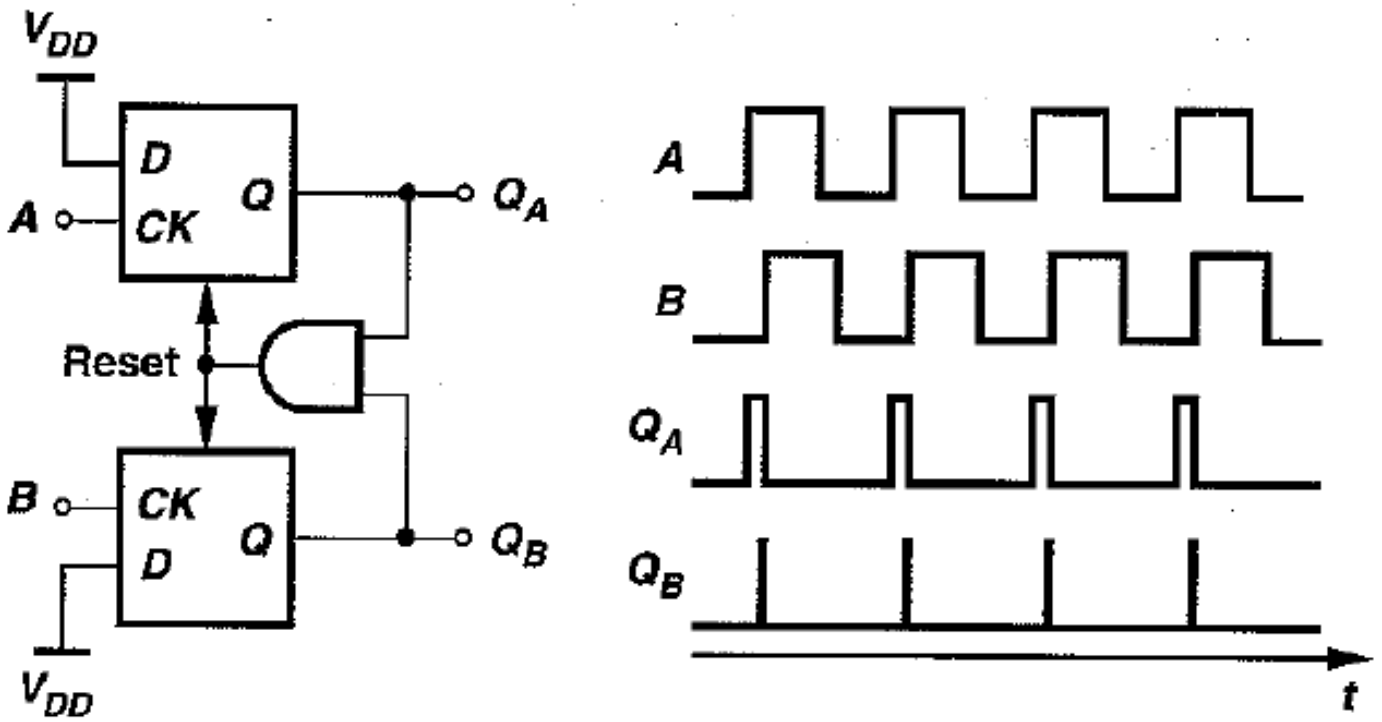
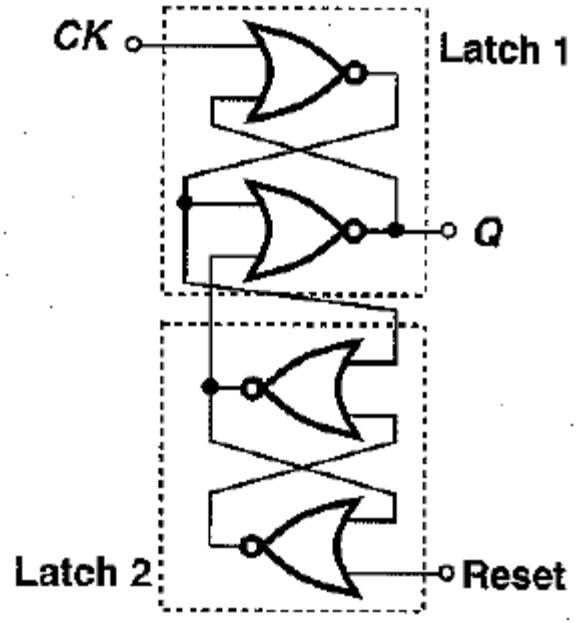
PFD Implementation

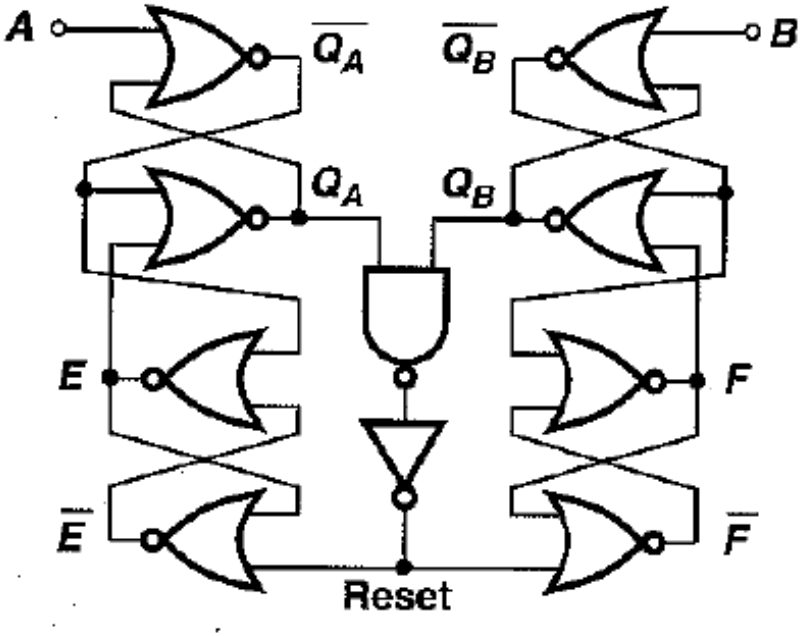


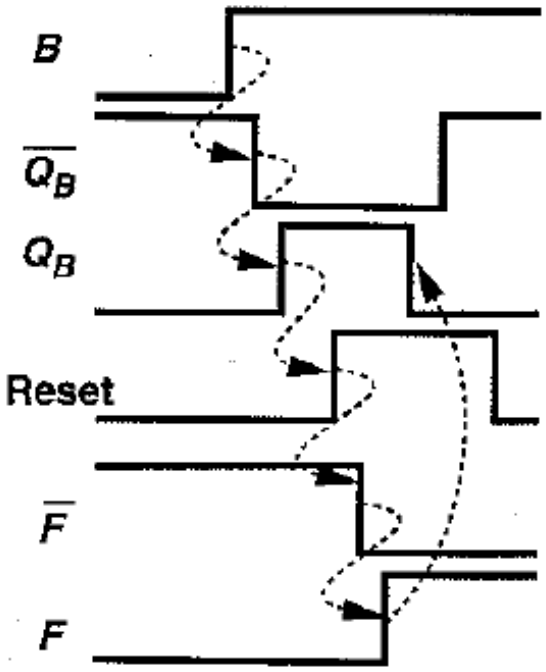
(a)

Compact SR Latch



Gate Level PFD





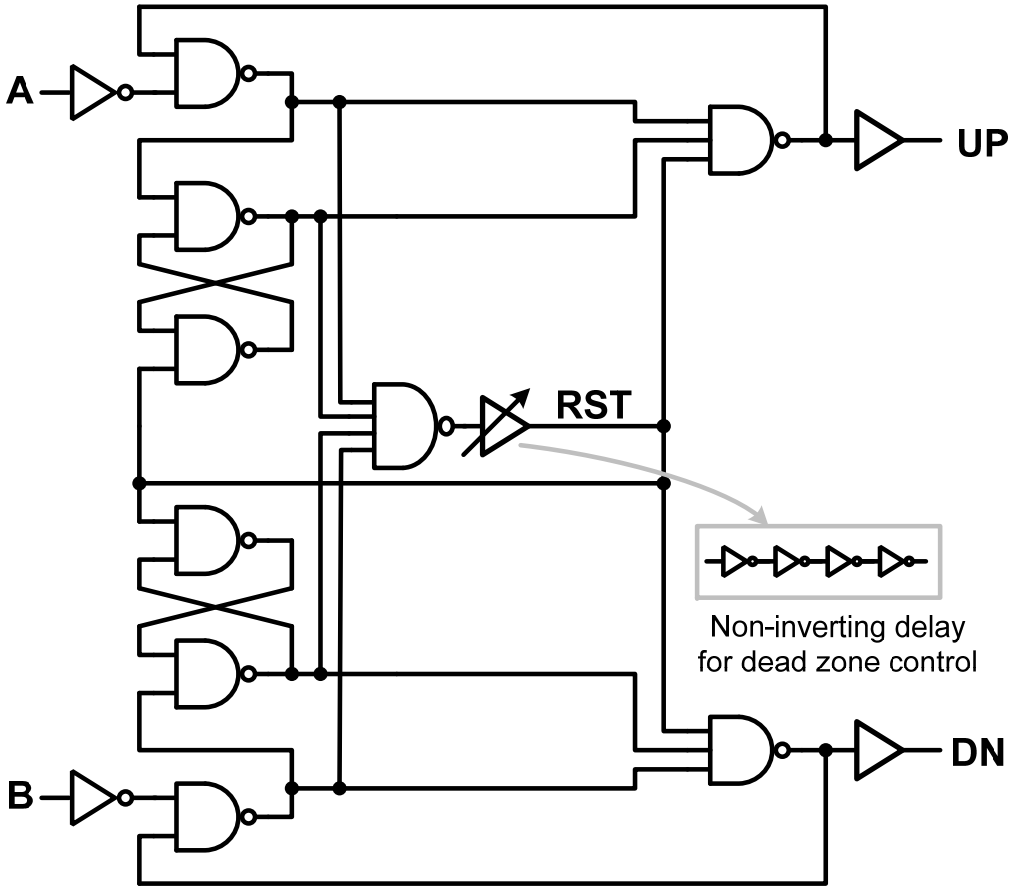
- Since the FF D input is always 1, the logic can be optimized for higher speed

PFD Contd.

- The nominal lock point of the PFD is 0
- Not sensitive to input duty cycle
- Near lock, the propagation of narrow pulses to switch the charge pump can case a PFD “dead zone”
  - Add extra delay in the PFD reset path to prevent dead zone

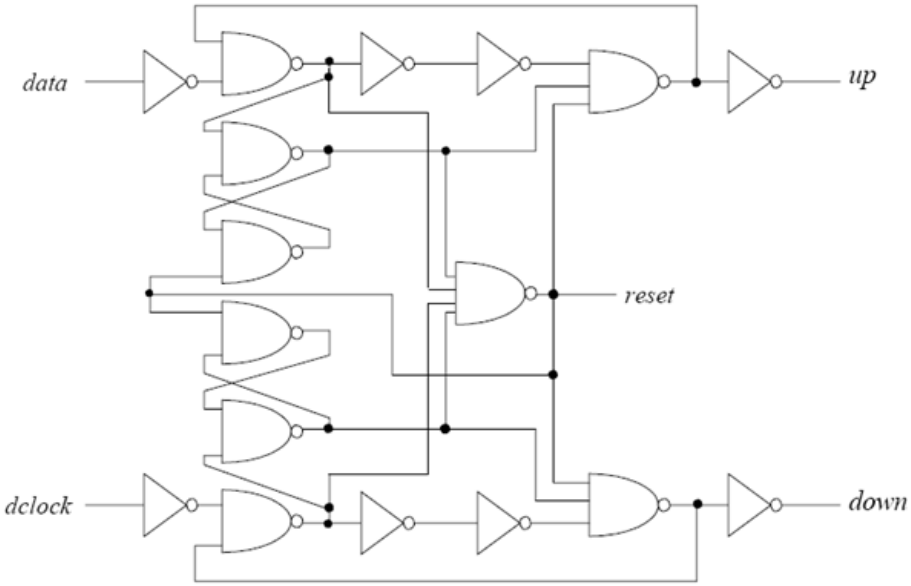
Other PFD Implementations

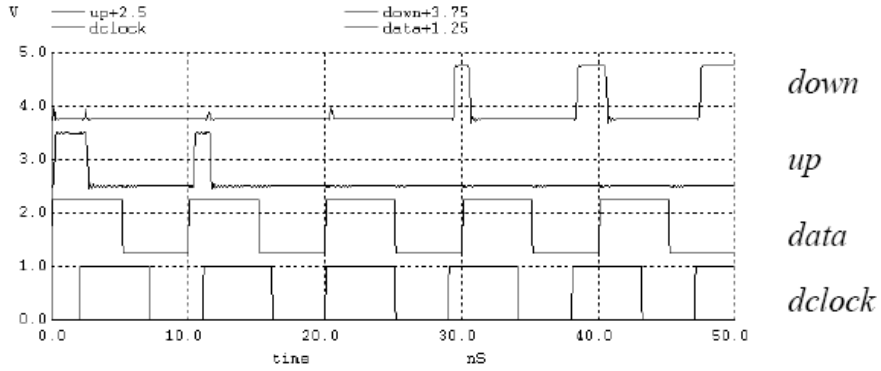
NAND-based PFD



- NAND implementation is preferred in CMOS design

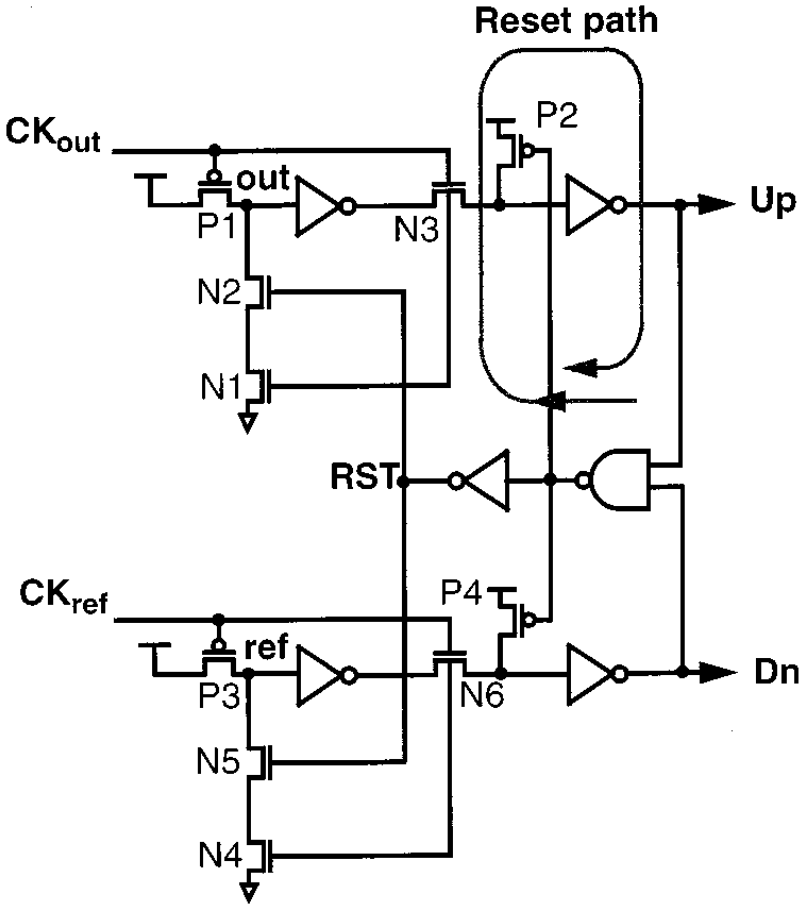
NAND-based PFD

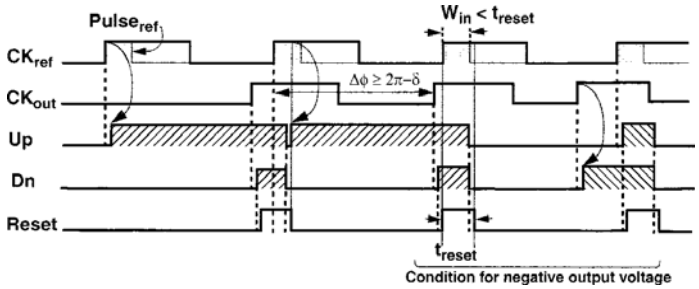


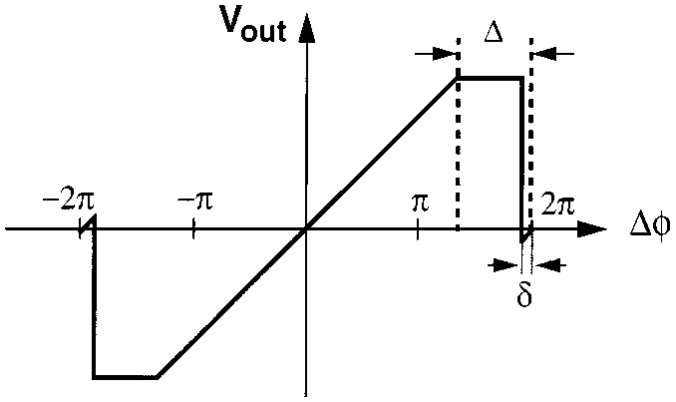


- From the CMOS Book

Pass-Transistor PFD



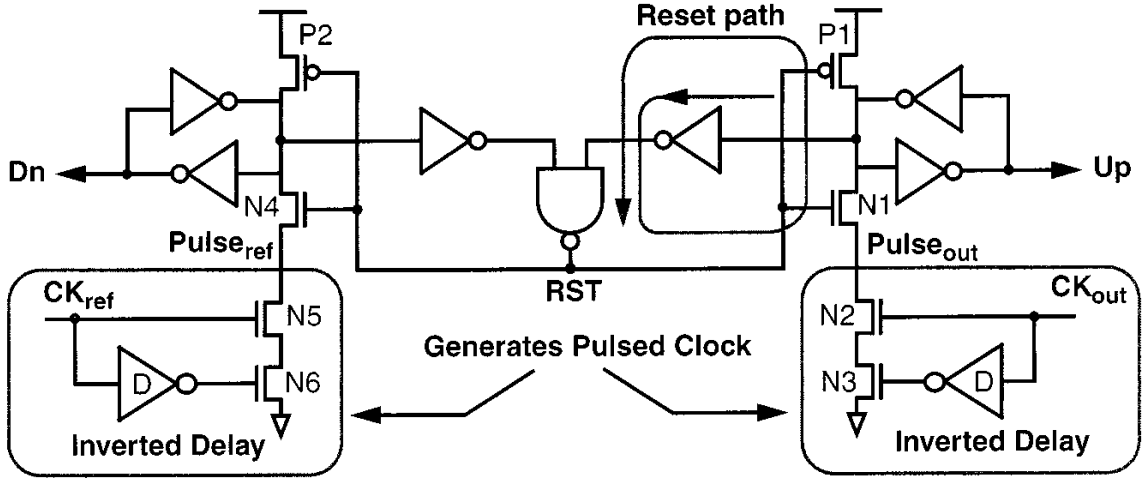


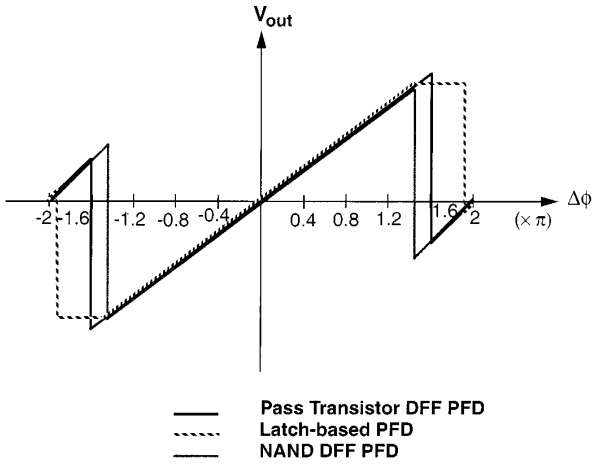


Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops

Mozhgan Mansuri, Dean Liu, and Chih-Kong Ken Yang

Fast Latch-based PFD





Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops

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References

1. B. Razavi, “Design of CMOS Analog Integrated Circuits,” McGraw Hill, 2002.
2. B. Razavi, “RF Microelectronics,” 2nd Ed., Prentice Hall, 2012.
3. R. J. Baker , “CMOS Circuit Design, Layout and Simulation,” 3nd Edition, Wiley-IEEE, 2010.
4. M. Mansuri, D. Liu, C.-K. K. Ken, “Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops,” IEEE JSSC, vol. 37, no. 10, Oct. 2002.