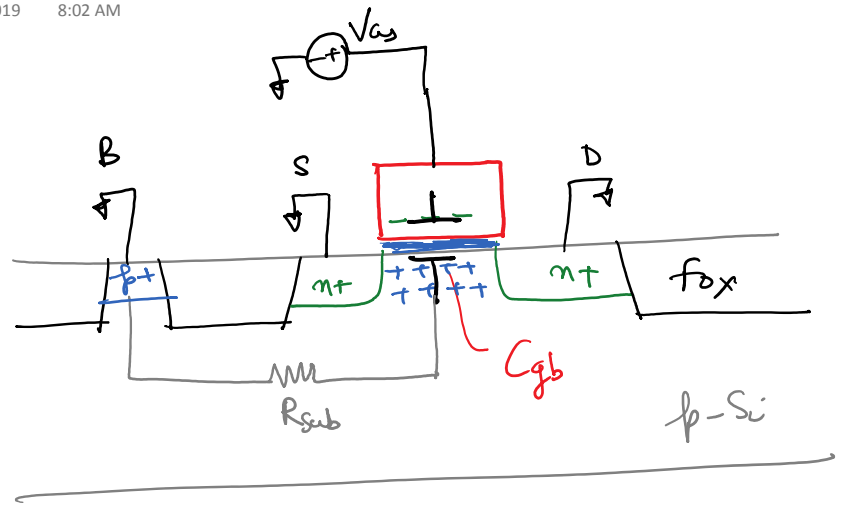
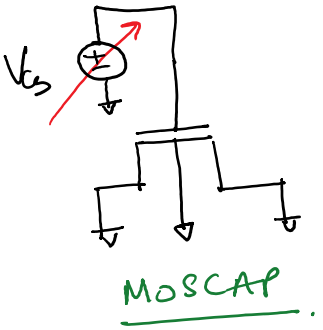
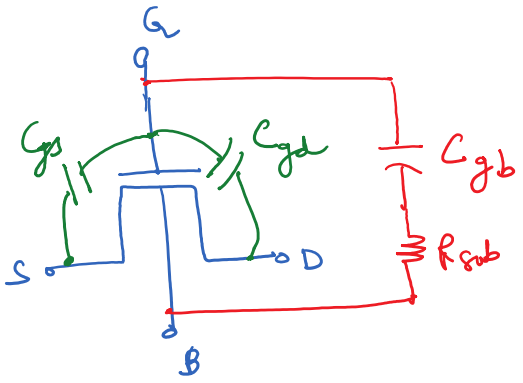
ECE 445 - Lecture 8

Wednesday, February 6, 2019 8:02 AM





Case I: Accumulation: ($V_{GS} < 0$)

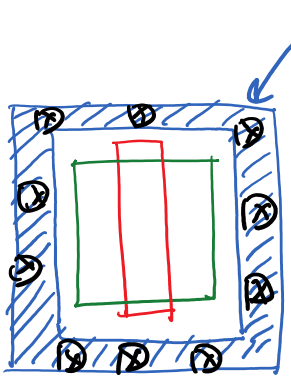


Resistance in series with C_{gb}

↳ makes a poor quality Cap in accumulation

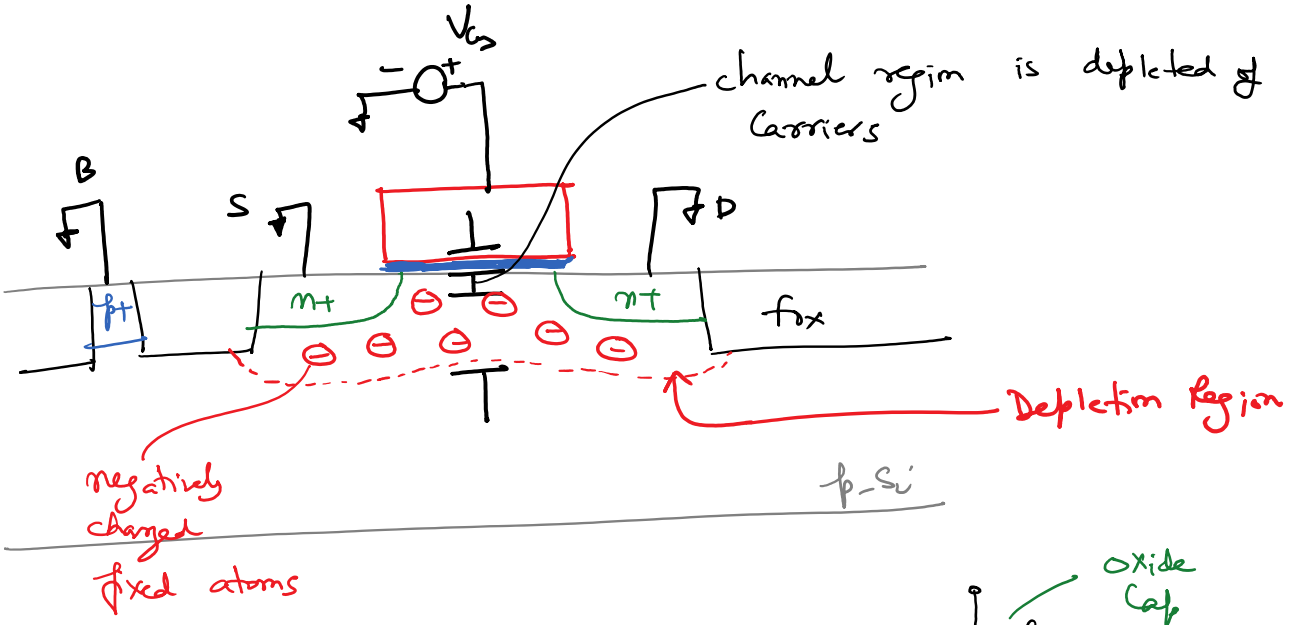
↳ plentiful substrate connections closer to the MOSFET

↳ R_{sub} is reduced due to several contacts in parallel.

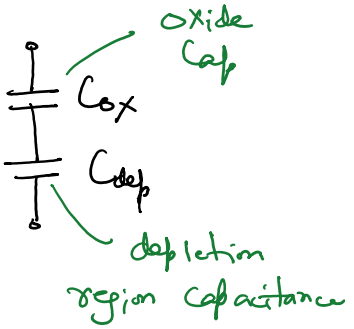


Case II : Depletion

* V_{GS} is increased but not negative enough to cause accumulation and not positive enough to invert the channel.



$$C_{gb} = C_{ox}' W (L - 2L_{diff}) \,||\, C_{depletion} + C_{GBO} \cdot L$$



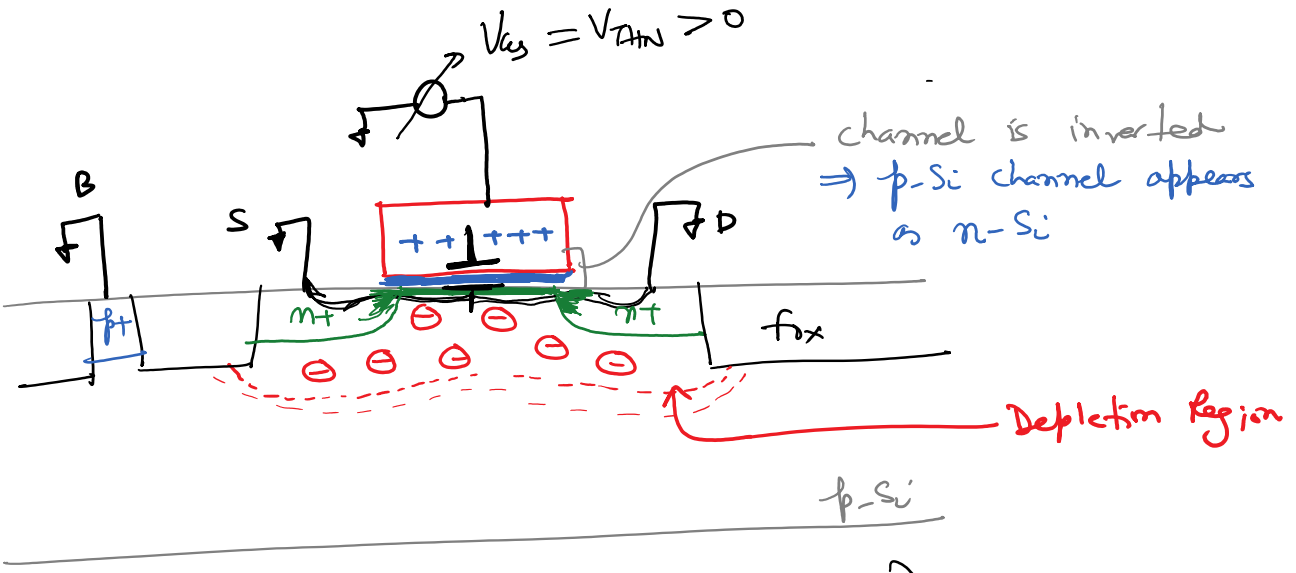
* Surface under the gate oxide is depleted of carriers.

If we further increase V_{GS}

↳ Weak inversion region ⇒ Subthreshold current can flow

Case III : Inversion :

↗ $V_{GS} = V_{TH_N} > 0$



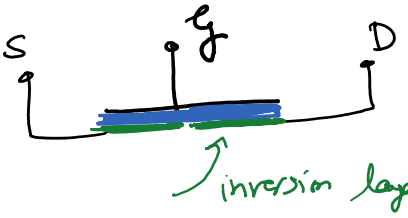
When V_{GS} is sufficiently large ($V_{GS} \geq V_{THN}$)

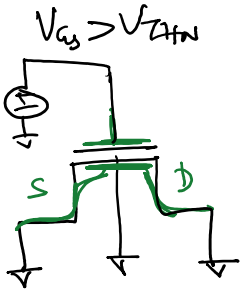
↳ large number of electrons are collected under the gate → channel region is inverted p → n

↳ the SiO_2/Si interface is no longer p-type

↳ n type

↳ These electrons in the channel region under the gate effectively "short" the drain & source in the above figure.





In Inversion:

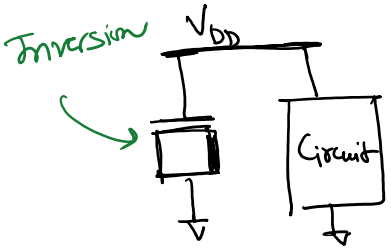
$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox}' W (L - 2L_{diff}) + C_{GSO} \cdot W$$

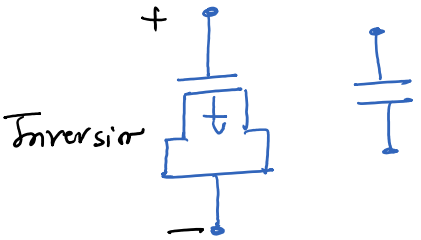
($C_{ox}' W (L - 2L_{diff})$: gate oxide)

$$= \frac{1}{2} C_{ox}' WL - C_{ox}' WL_{diff} + C_{ox}' L_{diff} \cdot W$$

$C_{gs} = C_{gd} = \frac{1}{2} C_{ox}' WL$

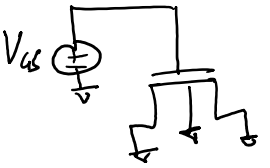
↳ No substrate resistance in the MOS CAP.



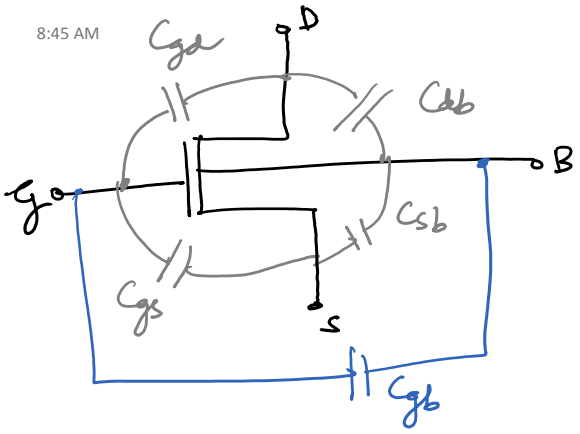


In inversion $C_{gb} = C_{GBO} \cdot L$

Parametric Semiconductor SPA Analyzer



MOSCAP C-V Plot :



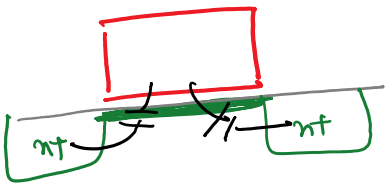
(Strong Inversion)

	Accumulation	Triode	Saturation
C_{gd}	$C_{GDO} \cdot W$	$\frac{1}{2} WL C_{ox}'$	$C_{GDO} \cdot W$
C_{db}	C_{jd}	C_{jd}	C_{jd}
C_{gb}	$C_{ox}' W L_{eff} + C_{GBO} \cdot L$	$C_{GBO} \cdot L$	$C_{GBO} \cdot L$
C_{gs}	$C_{GSO} \cdot W$	$\frac{1}{2} WL C_{ox}'$	$\frac{2}{3} WL C_{ox}'$
C_{sb}	C_{js}	C_{js}	C_{js}

pinch off

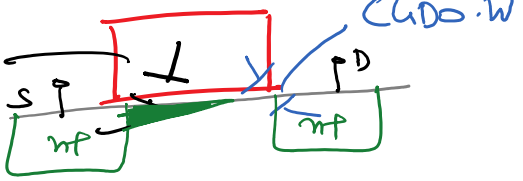
junction capacitances

Triode

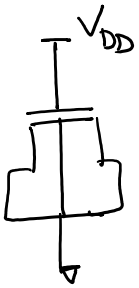


Saturation

$\frac{2}{3} C_{ox}' WL$



Ex 6.1 Decap using NMOS



$V_{GS} = V_{DD} > V_{TH}$

(Inversion)

$\frac{W}{L} = \frac{100}{100}$

DECAPS

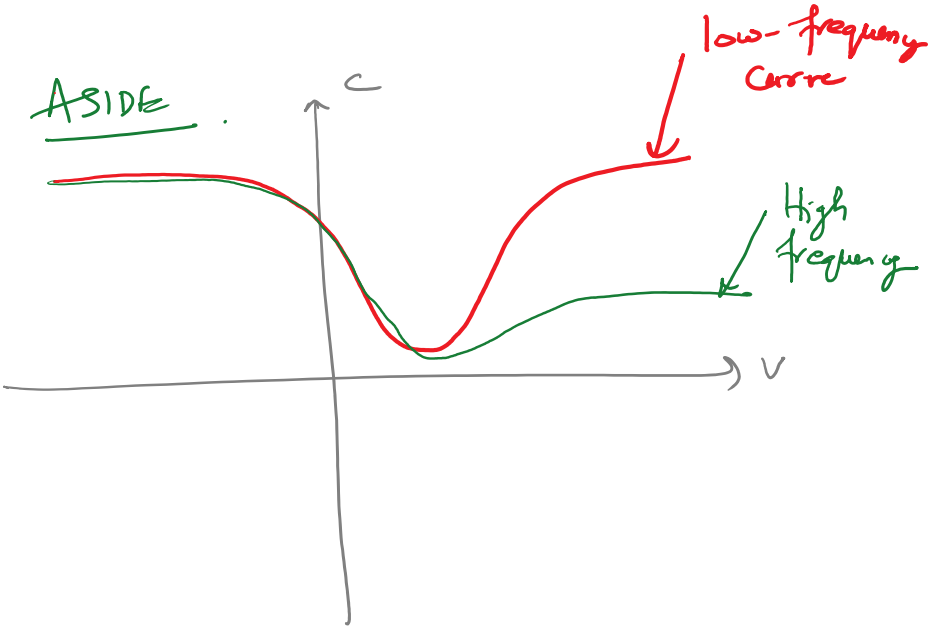
Scale = 1 μm.

$C = C_{ox} WL (scale)^2$

$= 1.75 \frac{fF}{\mu m^2} \times 100\mu m \times 100\mu m$

$= 17.5\ pF$

ASIDE.



Threshold Voltage:

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* When $V_{GS} \simeq V_{THN}$, the Si/SiO_2 (Gate oxide) interface is inverted
  - A channel of electrons is formed under the gate oxide.
  - This channel is built on the top of the depletion region.