ECE 445 - Lecture 7

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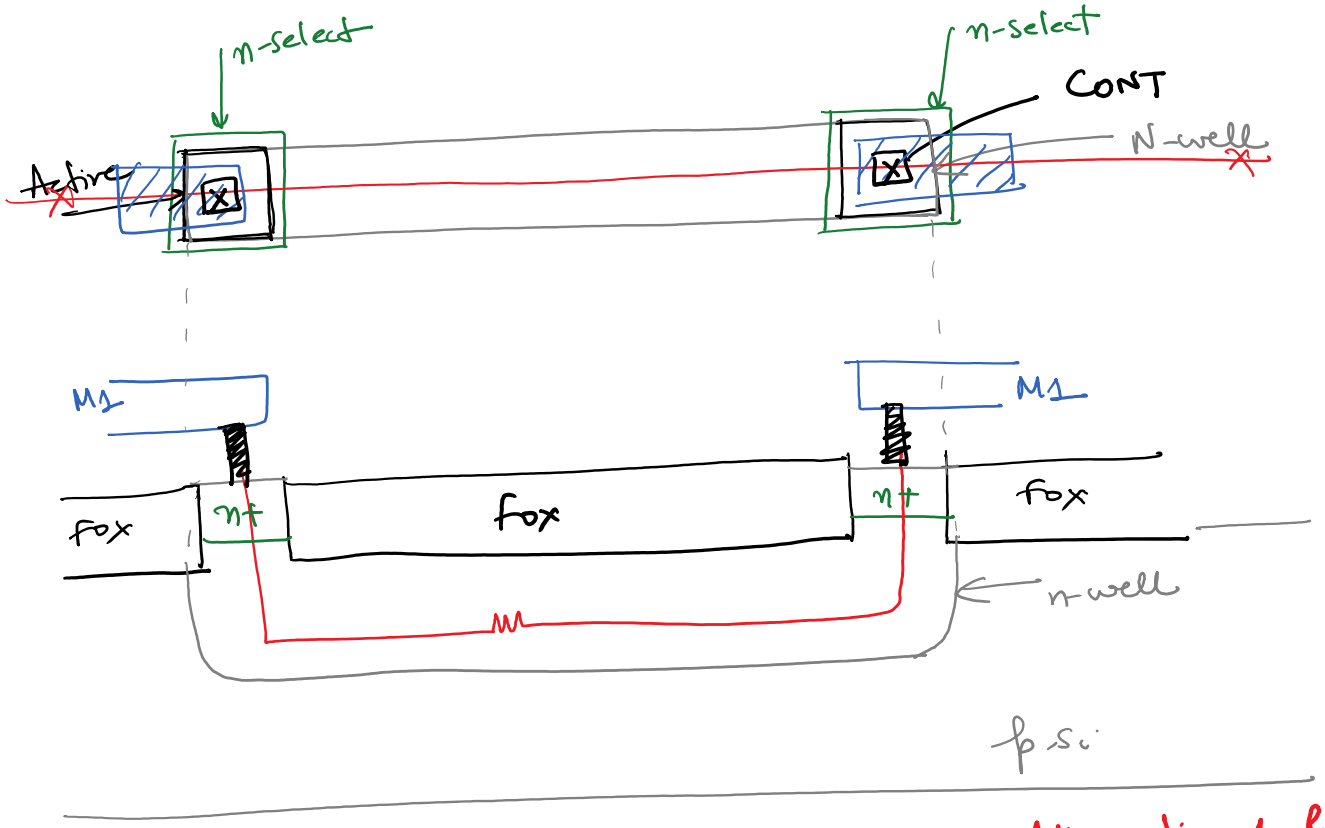
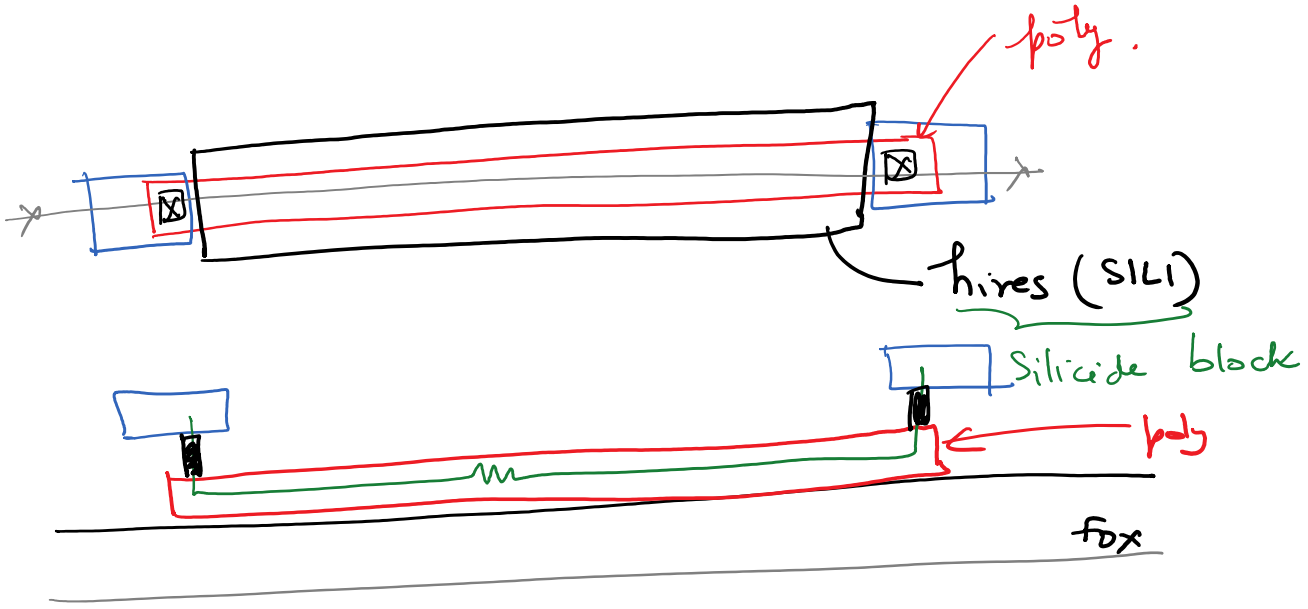
N-well Resistor Layout:

Ohmic Contact



All active & Poly are Silicided by default

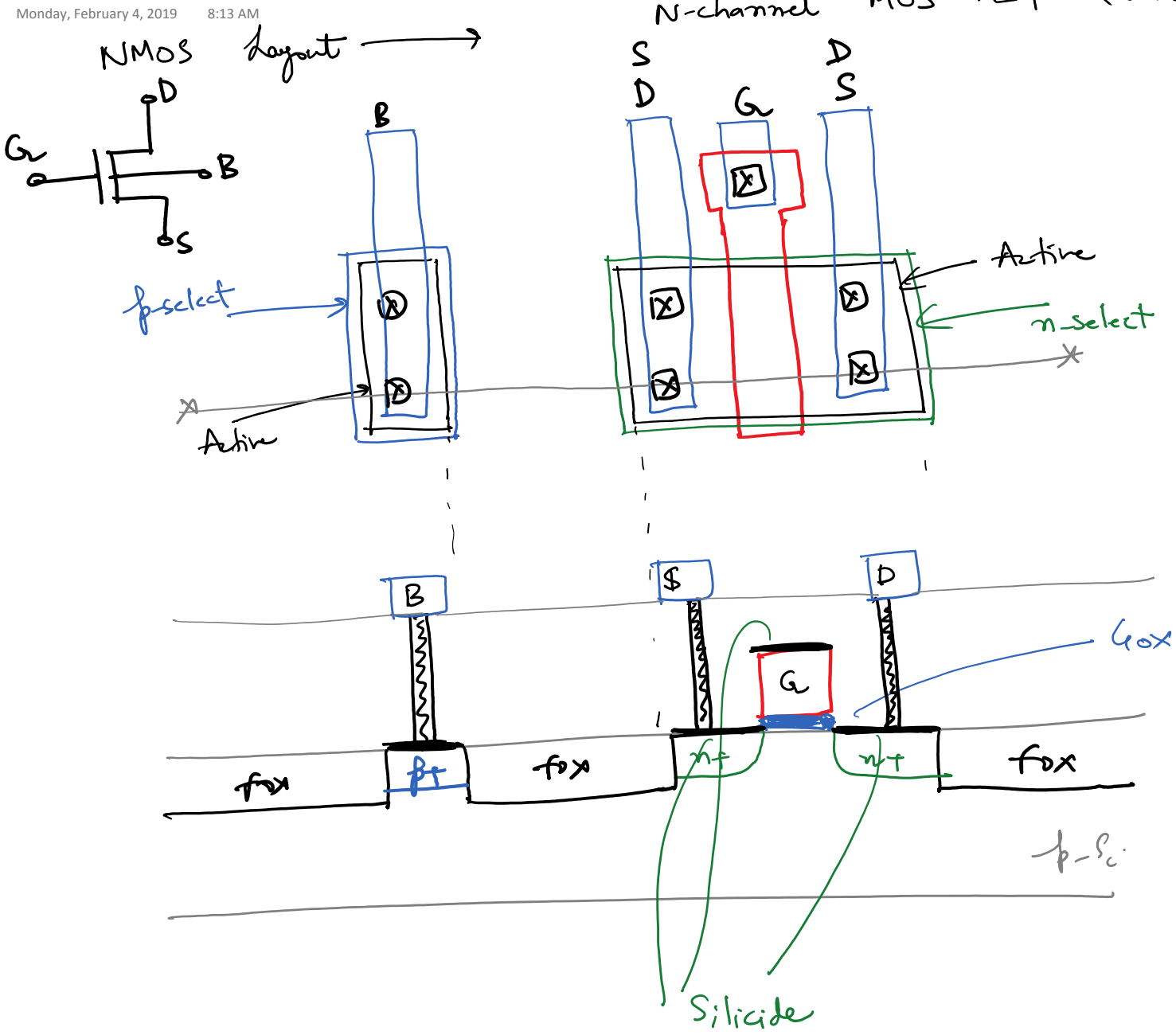
Poly Resistors:



p-si

- Can also dope polysilicon using n-select or p-select layers.

N-channel MOS FET (NMOS)



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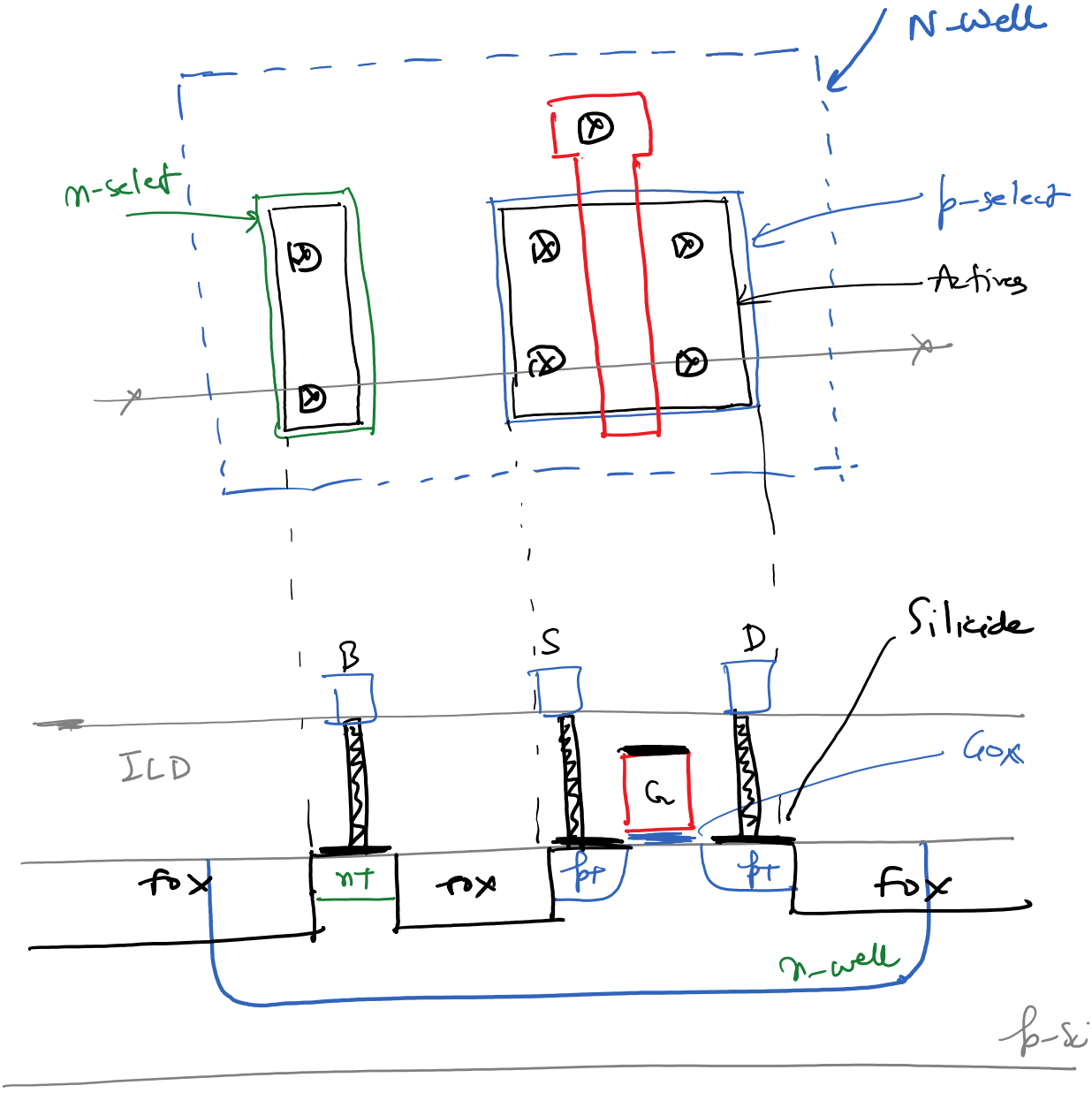
PMOS layout



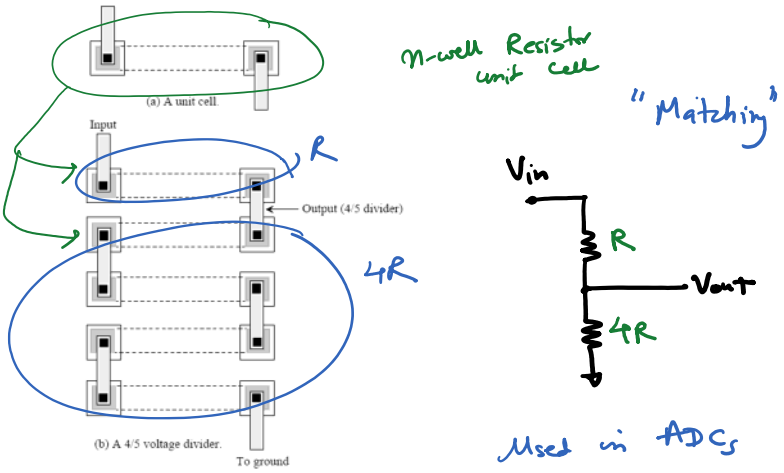


Figure 5.4 (a) Layout of a unit resistor cell, and (b) layout of a divider.

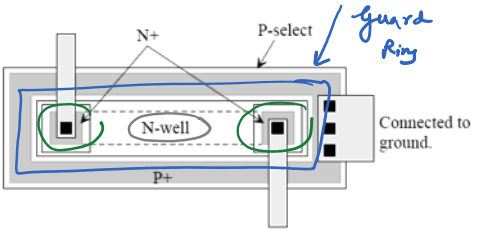


Figure 5.5 Guard ringing an n-well resistor.

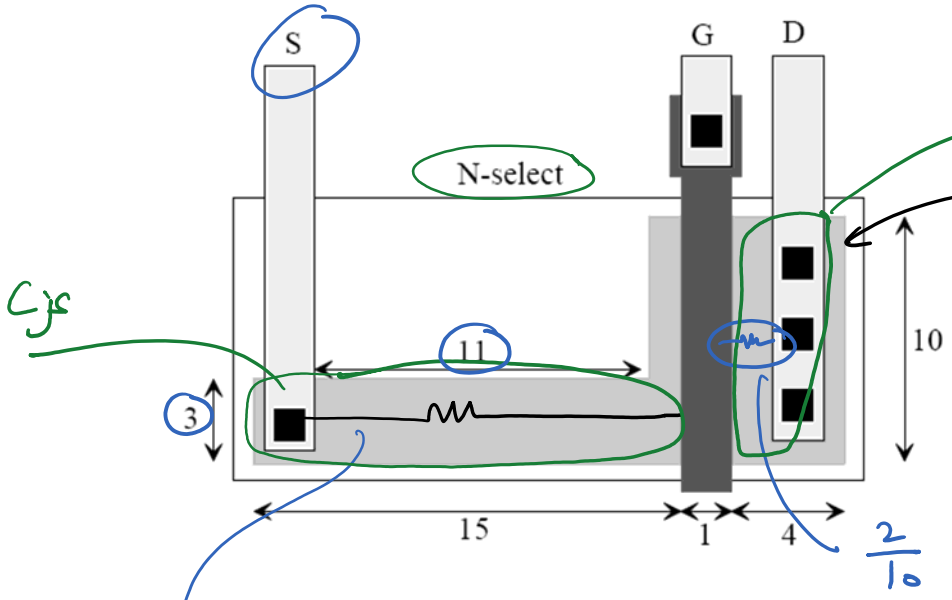


Figure 5.16 Layout of the MOSFET used in Ex. 5.5.

NMOS

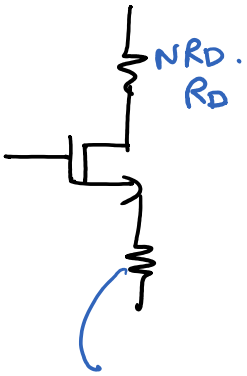
C_{gd}

Active

C_{js}

$NRS = \frac{11}{3}$

$NRD = \frac{2}{10}$



Junction Capacitance

$C_{js} \propto A_S = 15 \times 3 = 45$ (Cj per unit area)

$C_{jsw} \propto P_S = (15+3) \times 2$

Spice instance:

M1 D G S B L=1 W=10 AD=40 AS=45

PD=28 PS=36 NRD=0 NRS=4

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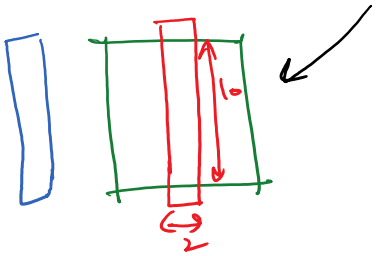
for 65 CMOS scale = 0.3μm

$\frac{W}{L} = \frac{10 \times scale}{2 \times scale} \Rightarrow \frac{W}{L} = \frac{500}{2}$ NMOS Layout

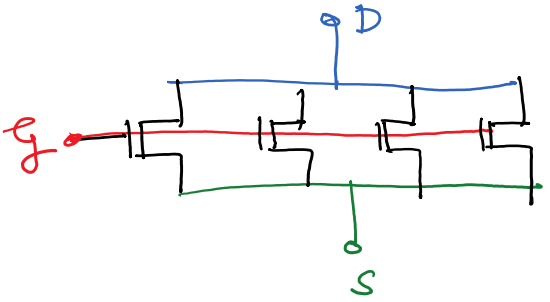
In Cadence, enter absolute values

$\Rightarrow \frac{W}{L} = \frac{3\mu m}{0.6\mu m}$



×50 times

Large Width MOSFETs



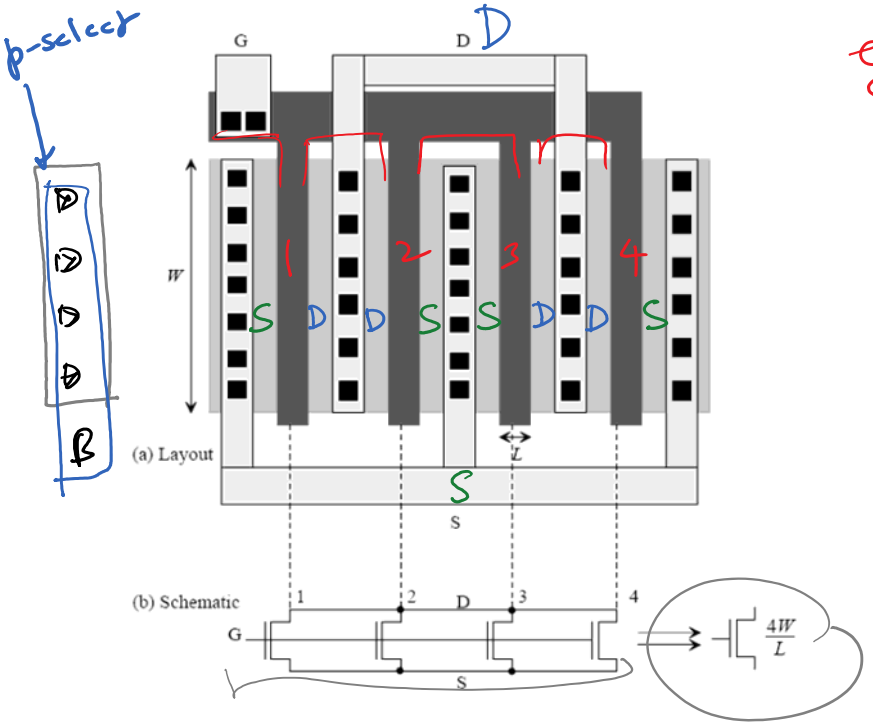
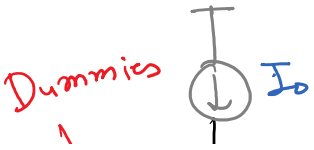
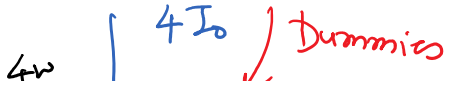
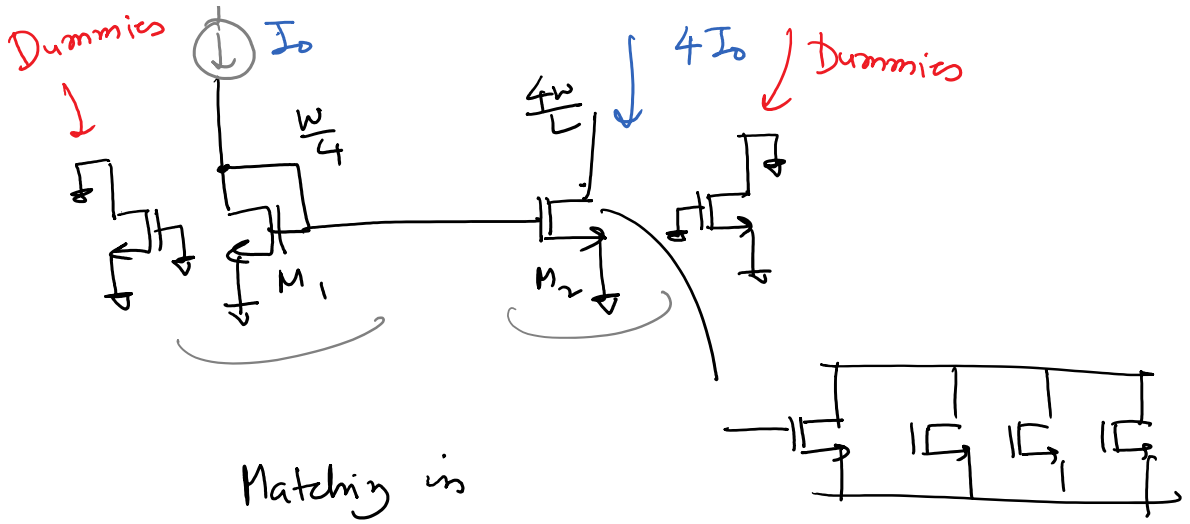


Figure 5.18 Layout and equivalent schematic of a large-width MOSFET.

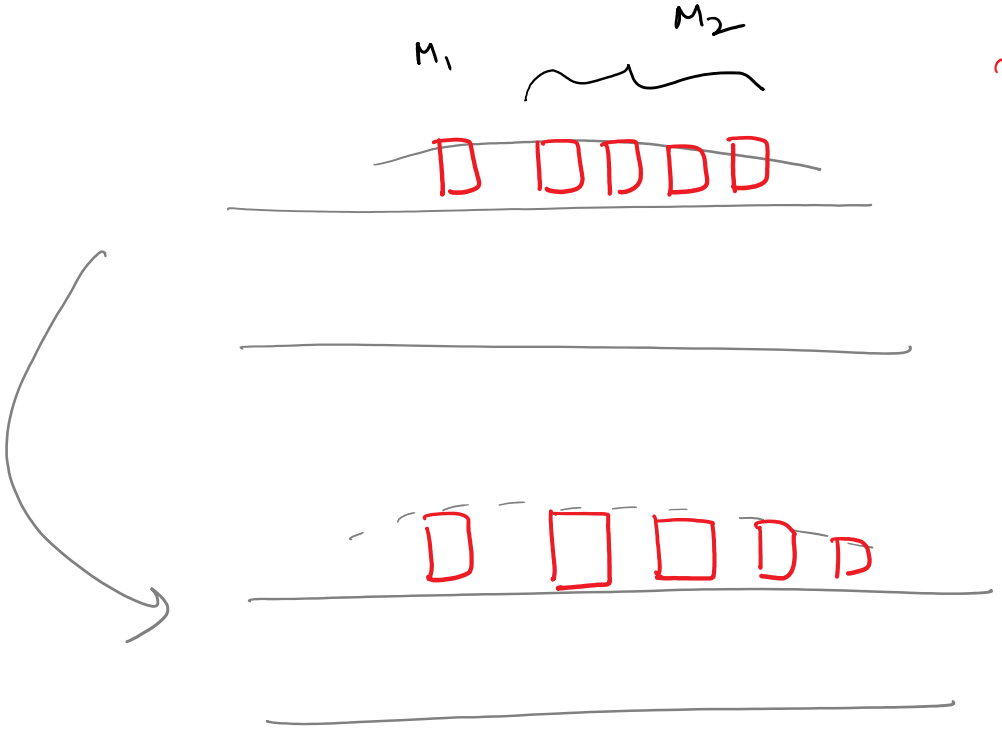






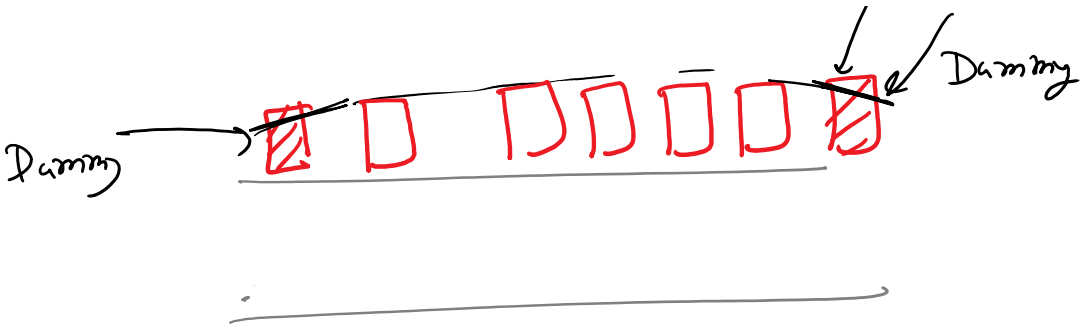
Matching in Analog circuits

* CMOS is planarized using CMP (chemical mechanical polishing process)



with dummy

DISHING DUE TO CMP


Dummy
Dummy

Long Length MOSFET Layout

$\frac{W}{L} = \frac{10}{100}$

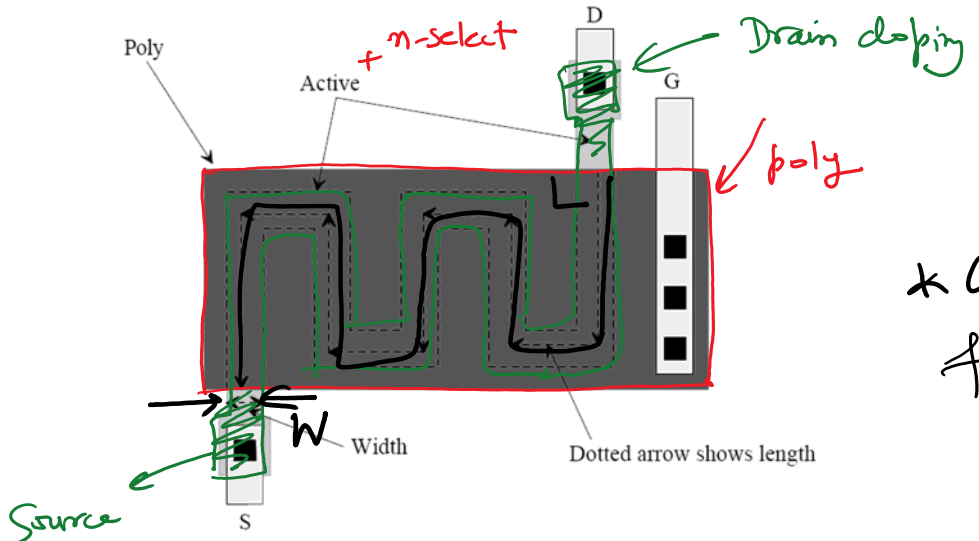
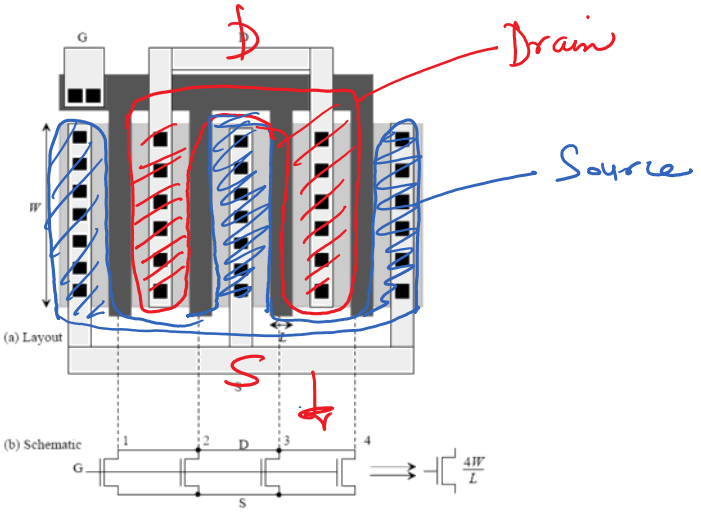


Figure 5.17 Layout of a long-length MOSFET.

* Compact layout for long lengths.



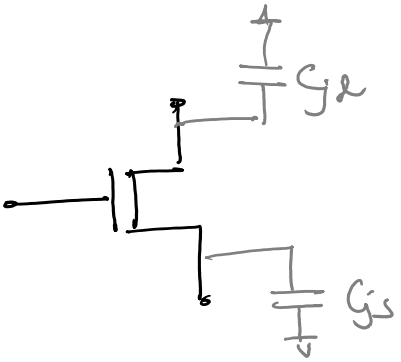
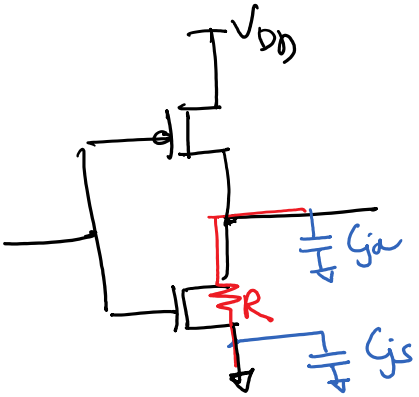


Figure 5.18 Layout and equivalent schematic of a large-width MOSFET.

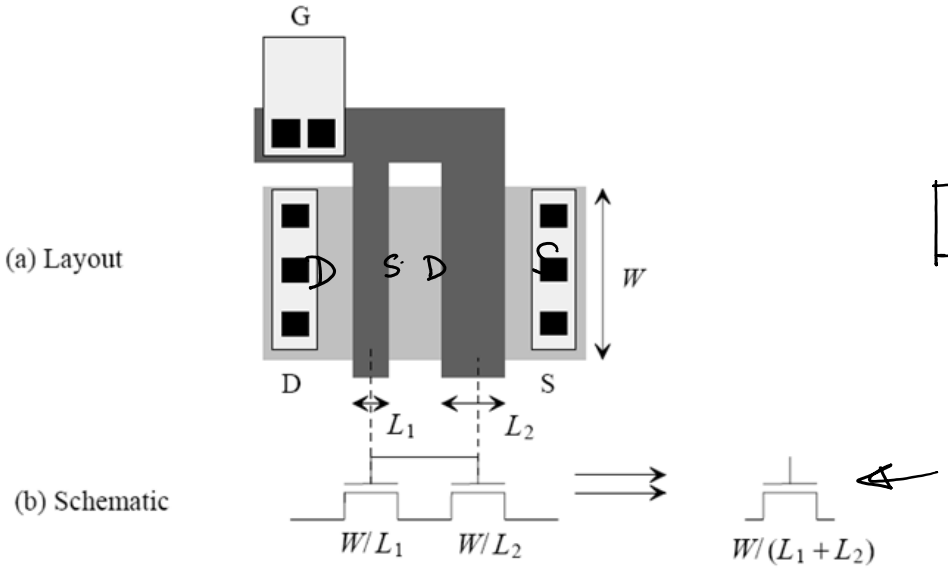
↳ Here source has larger area
↳ higher junction capacitance



$\tau = R \cdot C$

CMOS inverter

⇒ We want larger of the capacitances to be discharged to ground with small switch resistance



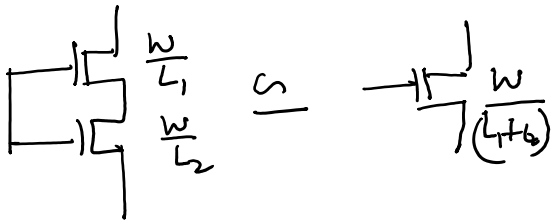


Figure 5.19 MOSFETs in series with gates tied together behave as a single MOSFET with the sum of the lengths.

" Process Integration Engineer "

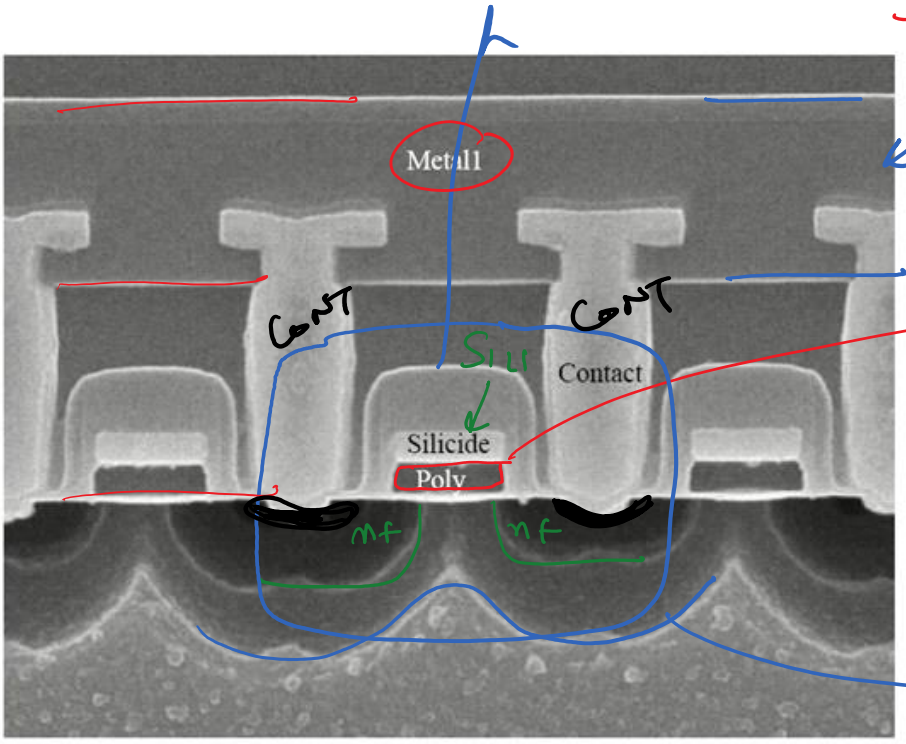


Figure 5.22 SEM image of the cross-section of three MOSFETs.

SEM

Chapter 6 : MOS Physics :

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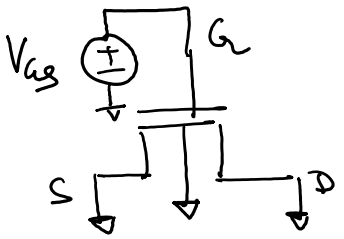
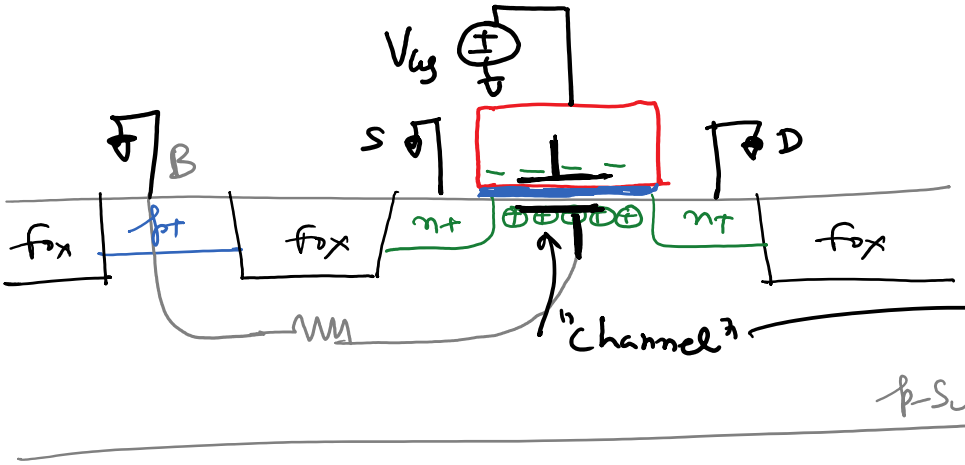




→ under poly gate at the Si & SiO_2 interface

Case I: Accumulation; $V_{GS} < 0$

⇒ mobile holes from the substrate are accumulated under the gate oxide in the channel region

* Capacitance b/w gate and bulk

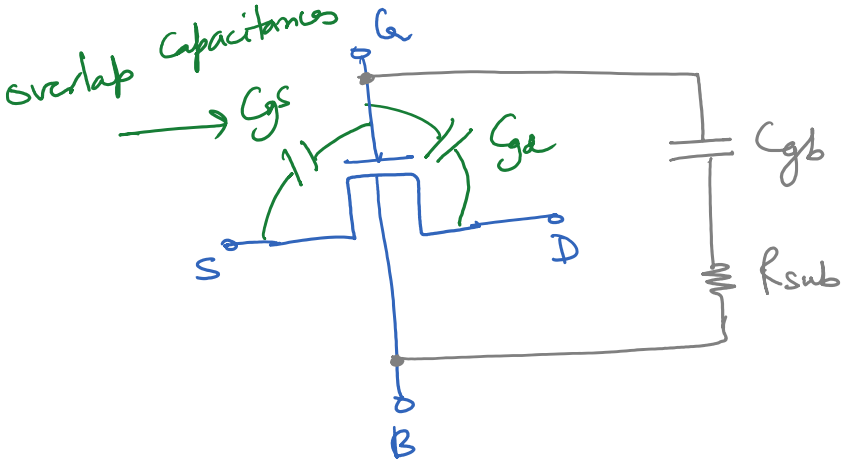
$$C_{gb} = C_{ox}' (L - 2L_{diff}) \cdot W$$

$(L - 2L_{diff}) = L_{eff}$

$$C_{ox}' = \frac{\varepsilon_0 \varepsilon_{rox}}{t_{ox}}$$

ε_{rox} ← permittivity for the gate oxide

t_{ox} ← gate oxide thickness



* MOSFET in Accumulation forms a poor quality Capacitor due to the series resistance.