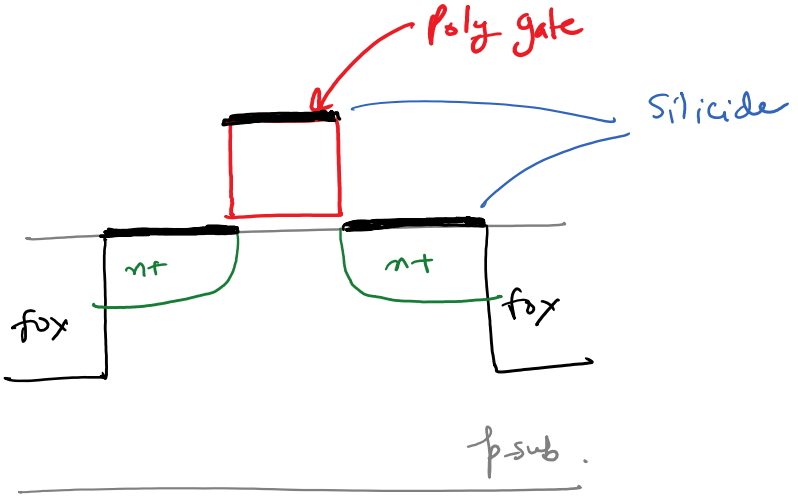
ECE 445 - Lecture 6.

Wednesday, January 30, 2019 8:04 AM

Silicidation: done by default in the CMOS process.



Silicide → Co/W + Si ⇒ semi-metallic layer with higher conductivity.
↳ lower sheet resistance

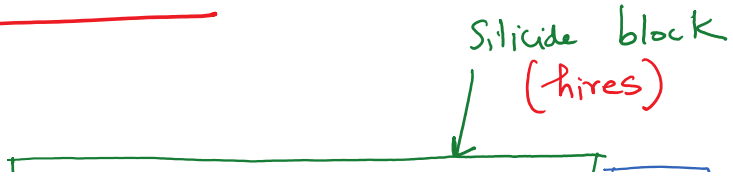
Ex. Poly $R_\square \Rightarrow 200\,\Omega/\square$

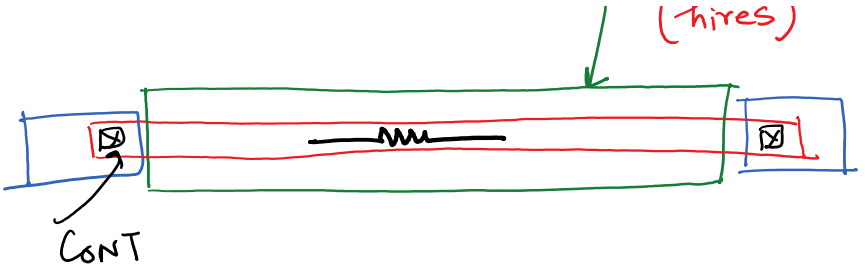
Silicided Poly $R_\square \Rightarrow 5\,\Omega/\square$ ← Can use for short distance routing

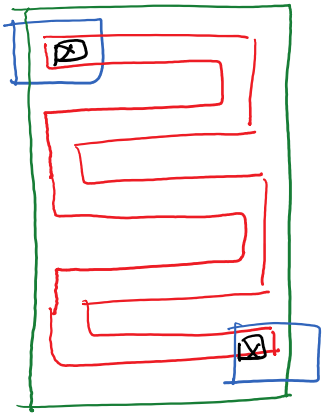
* Silicidation reduces the resistance of wires created using Poly or Active layers.

* Polysilicon makes linear resistors in CMOS process

Polysilicon Resistors:







* hires or SILI layer blocks silicidation in the enclosed region

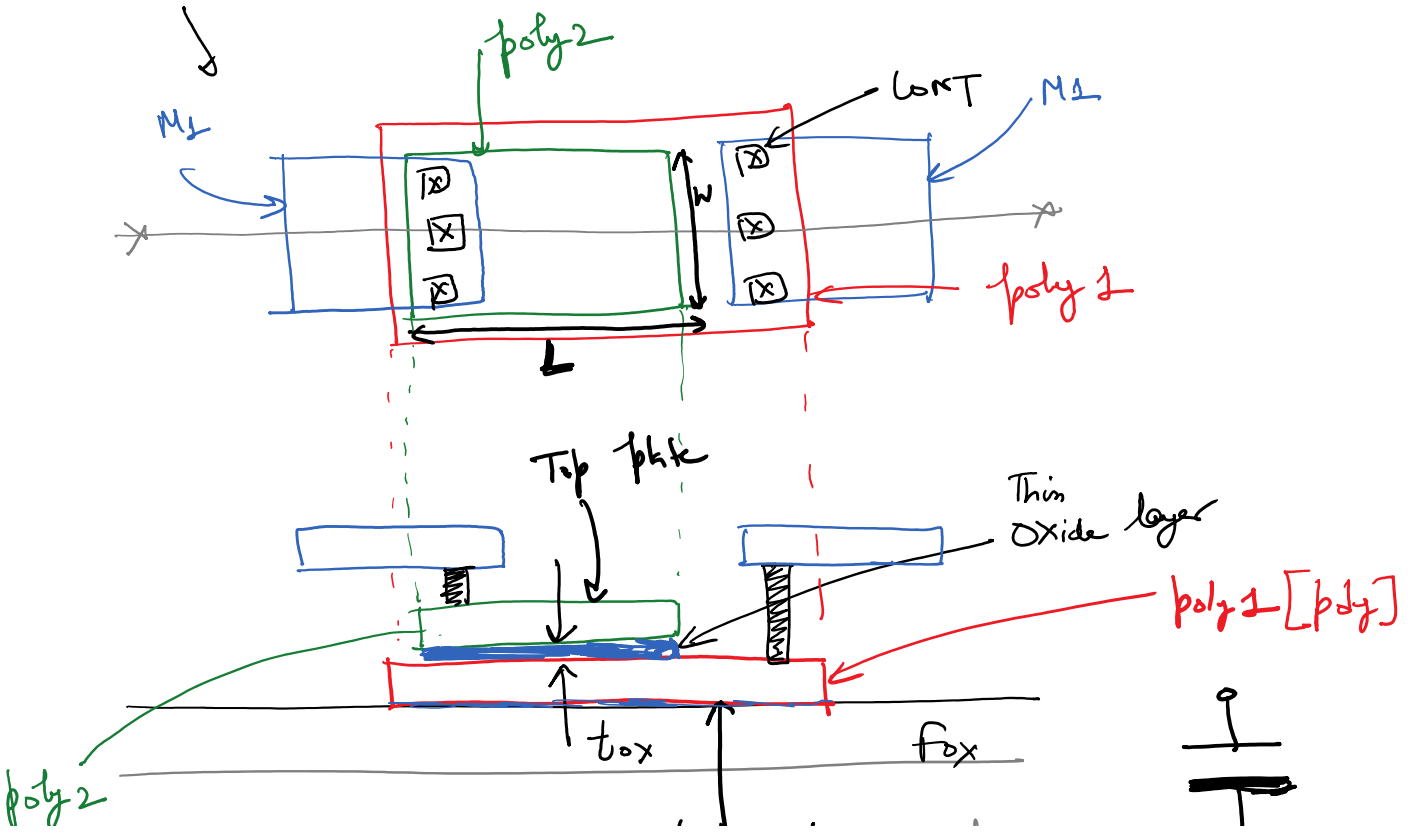
↳ All poly resistors are made without silicide.

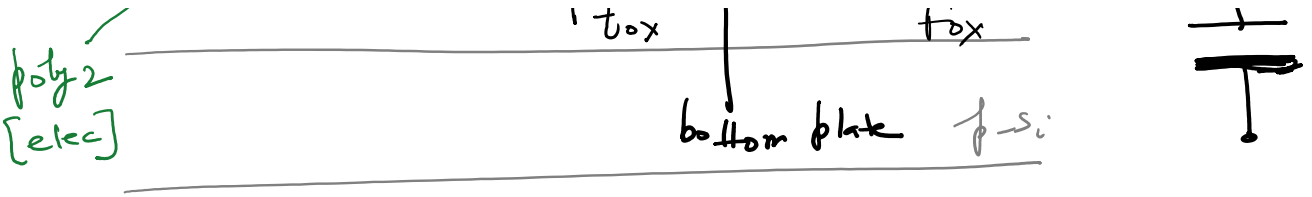
Poly-poly Capacitors :

⇒ C5 is a dual poly process

poly1 & poly2 are used to realize capacitors.

In Cadence poly1 → poly (bottom plate)
poly2 → elec ← Electrode (top plate)





$$C = C_{ox}' A = C_{ox}' \cdot W \cdot L \cdot (\text{scale})^2$$

scale = 0.3 μm

100 50

$$C_{ox}' = \frac{\varepsilon_0 \cdot \varepsilon_{oxide}}{t_{ox}}$$

Cap per unit area (constant for the procss)

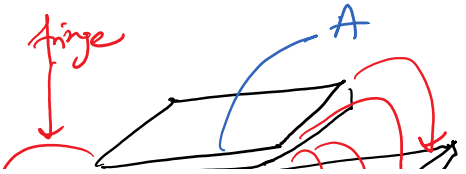
$\varepsilon_0 = 8.85 \frac{aF}{\mu m}$ ← permittivity in vaccum

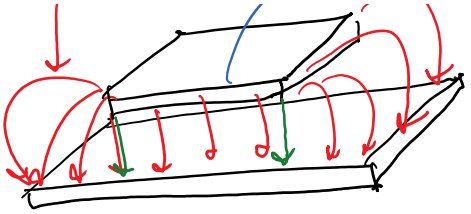
$\varepsilon_{ox} \simeq 3.97$ for SiO_2

CMOS tech	t_{ox}	C_{ox}'
1 μm	200 Å	1.75 $fF/\mu m^2$
50 nm	14 Å	25 $fF/\mu m^2$

from CMOS book

$C = C_{ox}' \cdot W \cdot L \cdot (\text{scale})^2$ ignoring the fringe effects

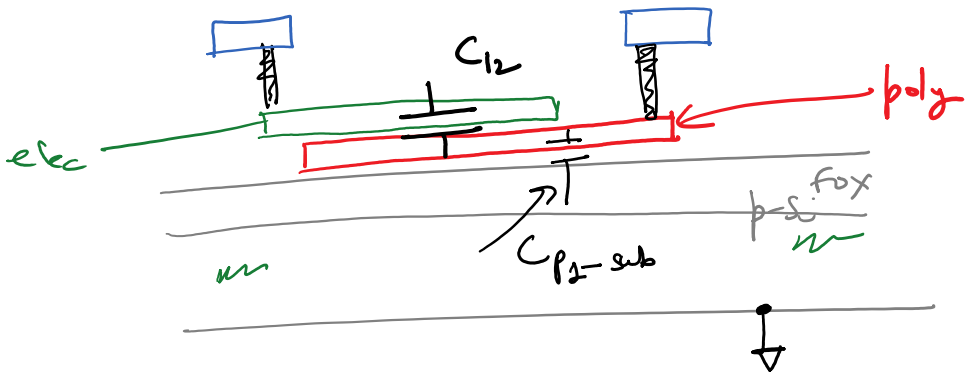


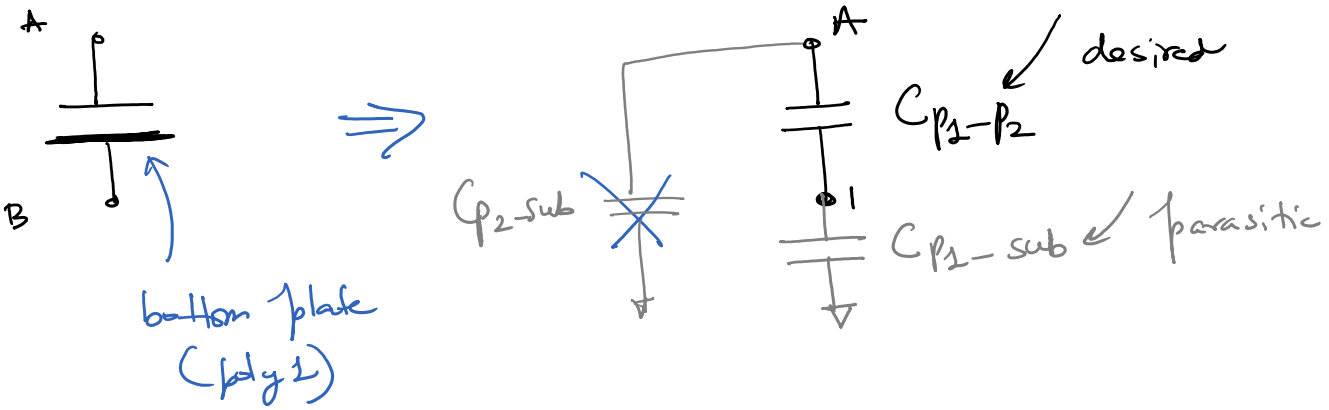


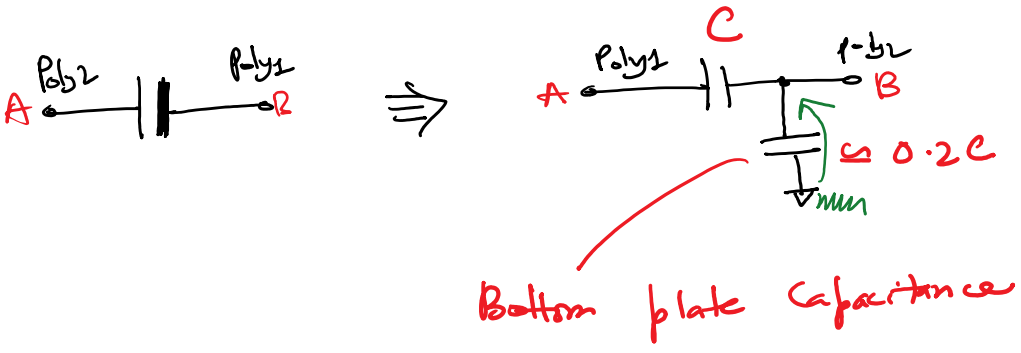
On chip ⇒ Capacitance
resistance

<1% variation in R+C on the same chip

But from chip to chip ±20% variation in R & C values.

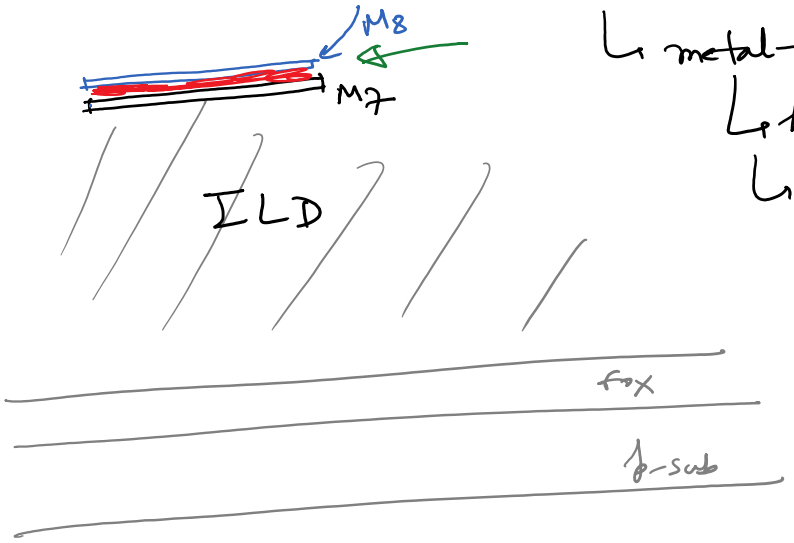






In Advanced process :

MiM Capacitors



MiM Capacitors

↳ metal-insulator-metal Capacitors

↳ highly linear

↳ no substrate noise coupling

MOSFETs :

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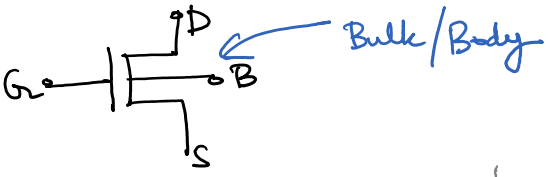
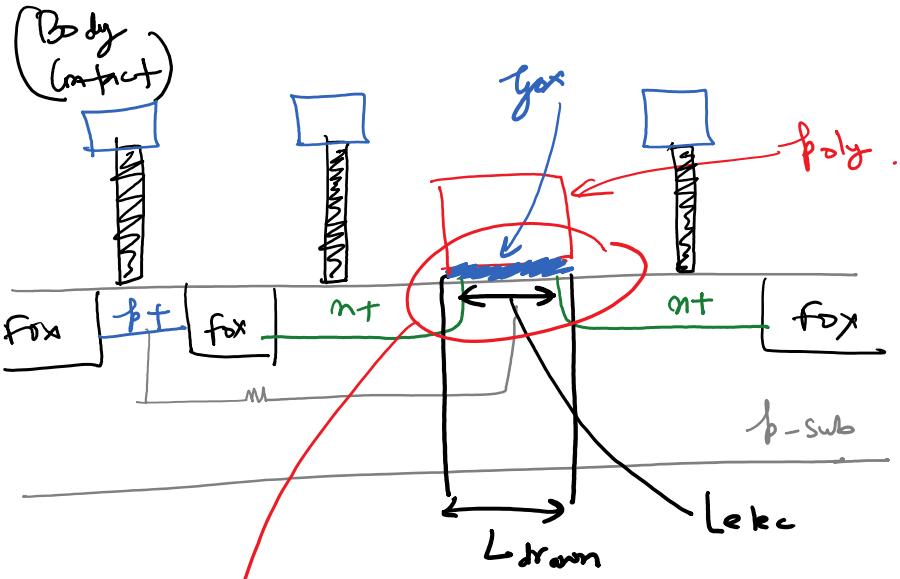
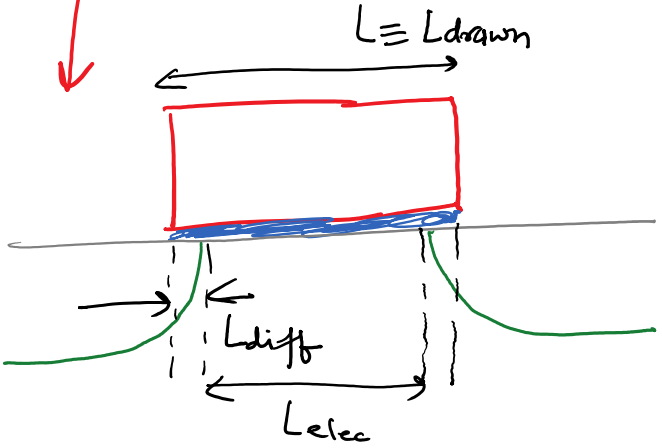


ion implantation

↳ Thermal Annealing





Lateral Diffusion

$$L_{elec} = L_{drawn} - 2 L_{diff}$$

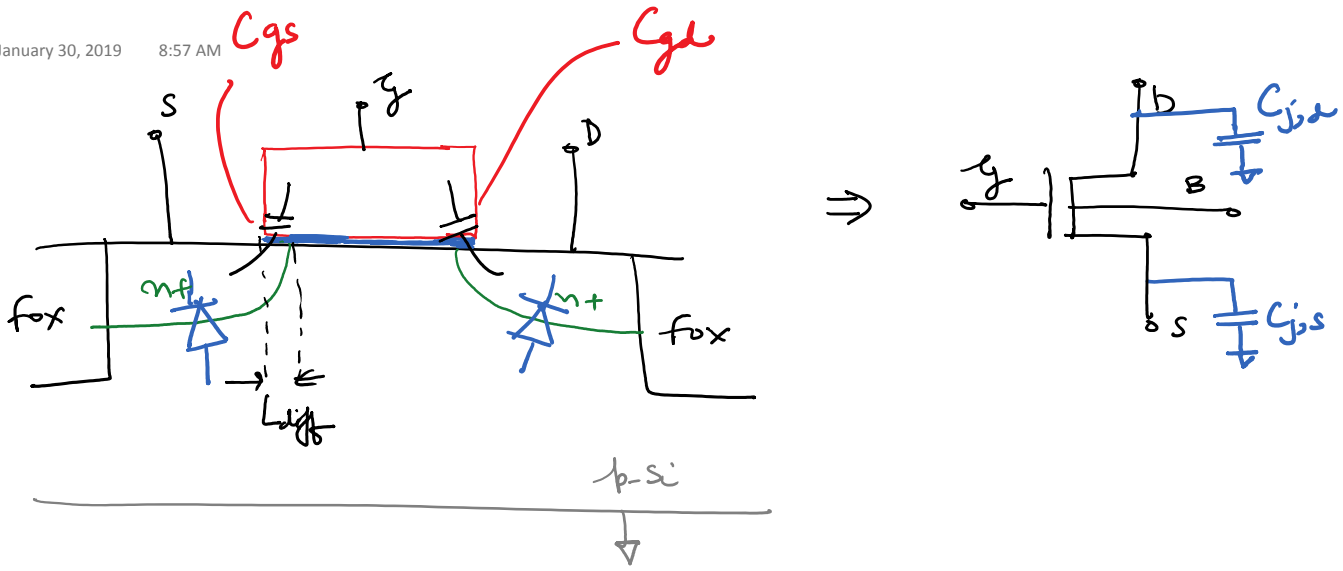
Oxide Encroachment:

* fox is not precisely patterned and encroaches into the active area and thus reduces the active opening along the width.

Effective width

$$W_{eff} = W_{drawn} - 2W_{enc}$$

↳ We can take care of W_{enc} by bloating the masks while processing.



Junction Capacitance

$$C_{jsd} = \underbrace{\frac{C_j \cdot A_{s,d}\,(scale)^2}{\left(1 + \frac{V_{(S,D)B}}{PB}\right)^{m_j}}}_{\text{bottom area}} + \underbrace{\frac{C_{jsw} \cdot P_{s,D}\,(scale)}{\left(1 + \frac{V_{(S,D)B}}{Pb_{SW}}\right)^{m_{jsw}}}}_{\text{sidewall capacitance}}$$

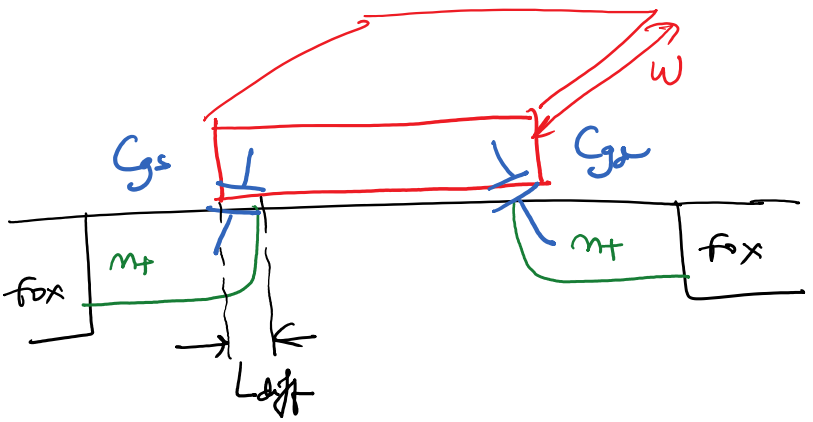
C_j = zero bias depletion capacitance - bottom

C_{jsw} = " " " " - sidewall

PB, Pb_{SW} } Built-in potential for bottom / sidewall

$V_{(S,D)B} \Rightarrow V_{SB}$ V_{DB} source or drain to body voltage difference

Overlap Capacitances :



$$C_{gs} = C_{ox}' \cdot L_{diff} \cdot W = C_{GSO} \cdot W$$

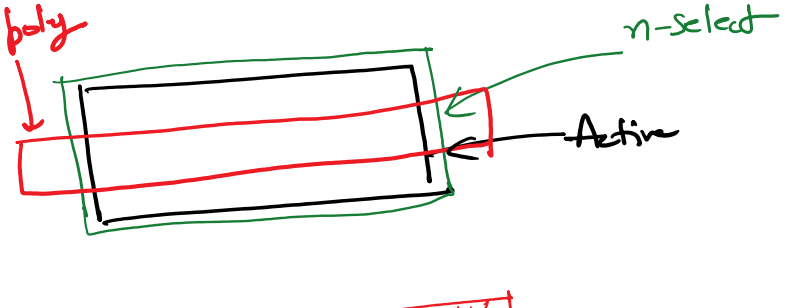
$$C_{gd} = C_{ox}' \cdot L_{diff} \cdot W = C_{GDO} \cdot W$$

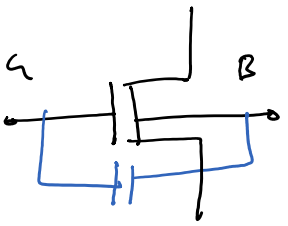
C_{GSO} ⇒ Gate Source overlap Capacitance parameter

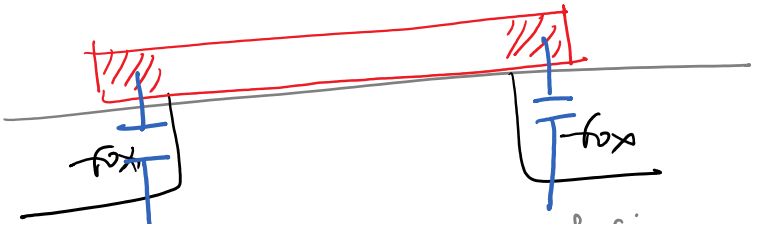
C_{GDO} ⇒ Gate Drain " " "

↳ in BSIM model for the MOSFET

C_{GBO} ⇒ Gate poly extension over the field region

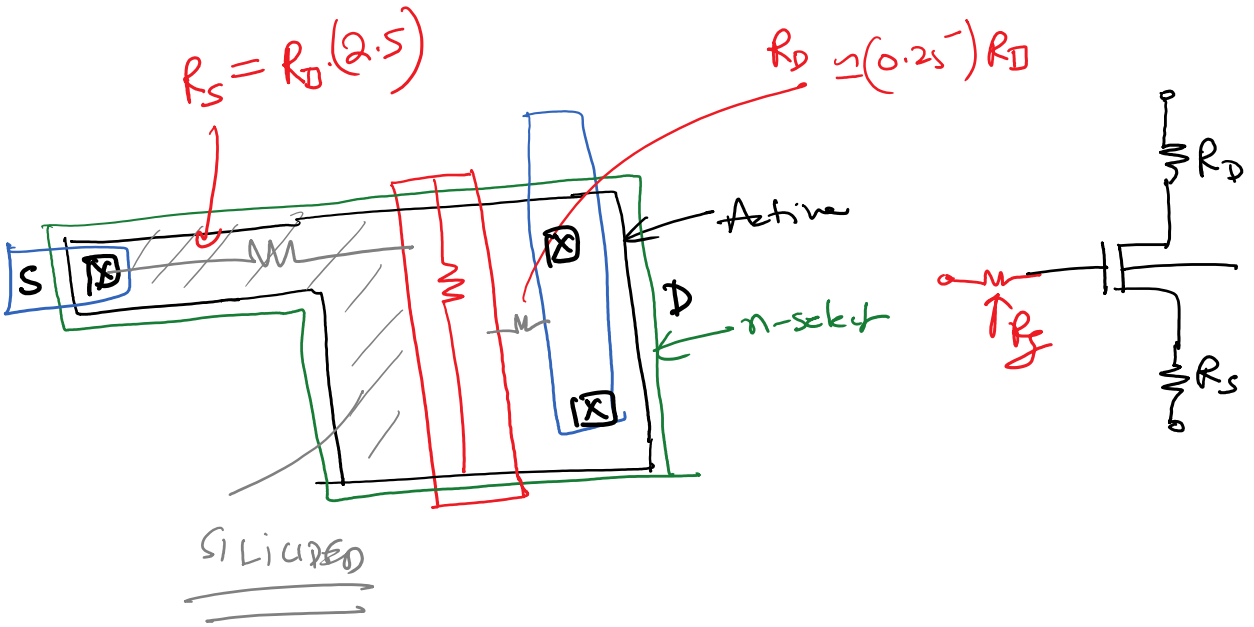






$C_{gb} = C_{GBO} \cdot L$


tox
p-si


$R_S = R_D \cdot (2.5)$
$R_D = (0.25^{-}) R_D$
S
D
Active
n-select
R_D
R_S
R_f
Silicided