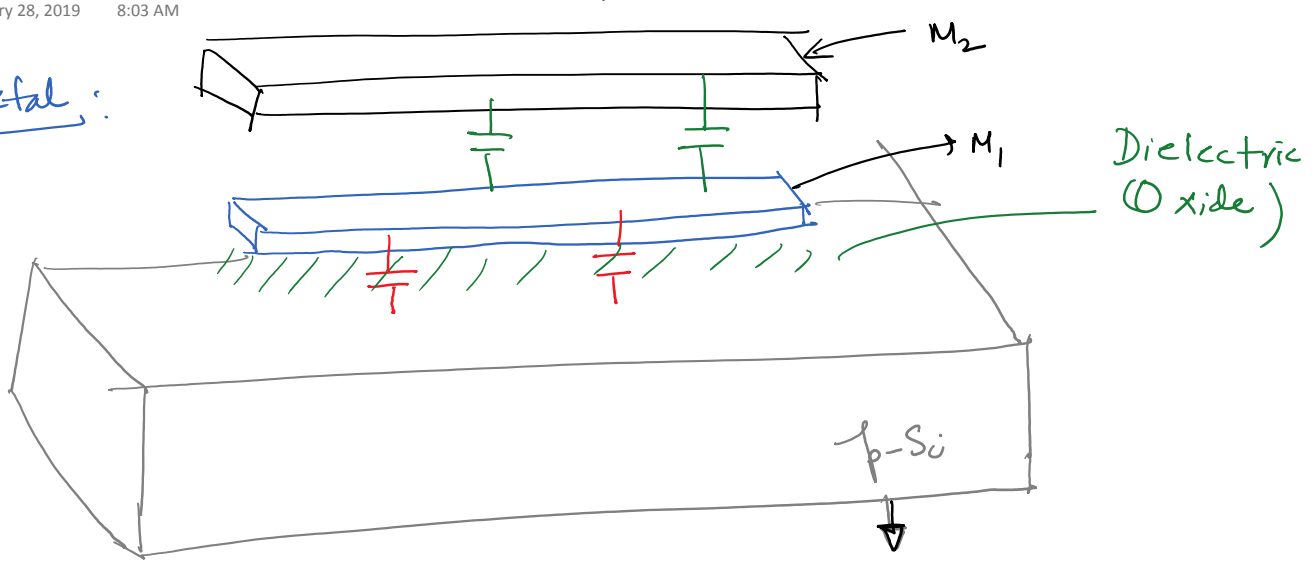
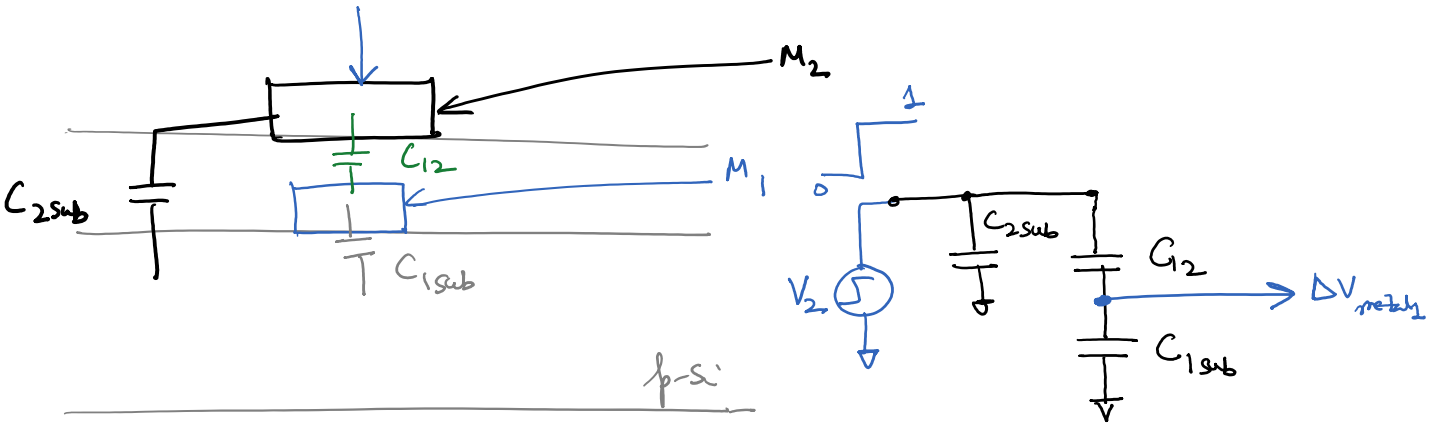
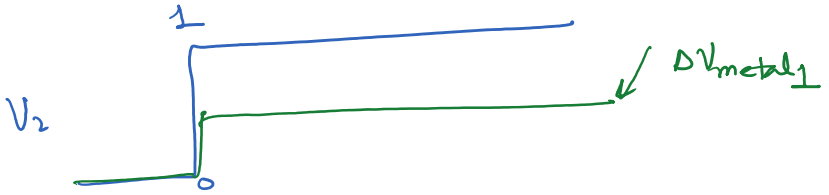
ECE 445 - Lecture 5.

Monday, January 28, 2019 8:03 AM

Metal:

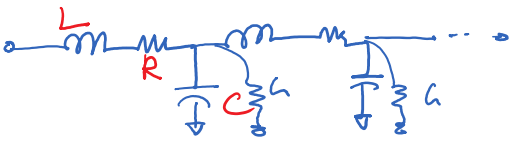


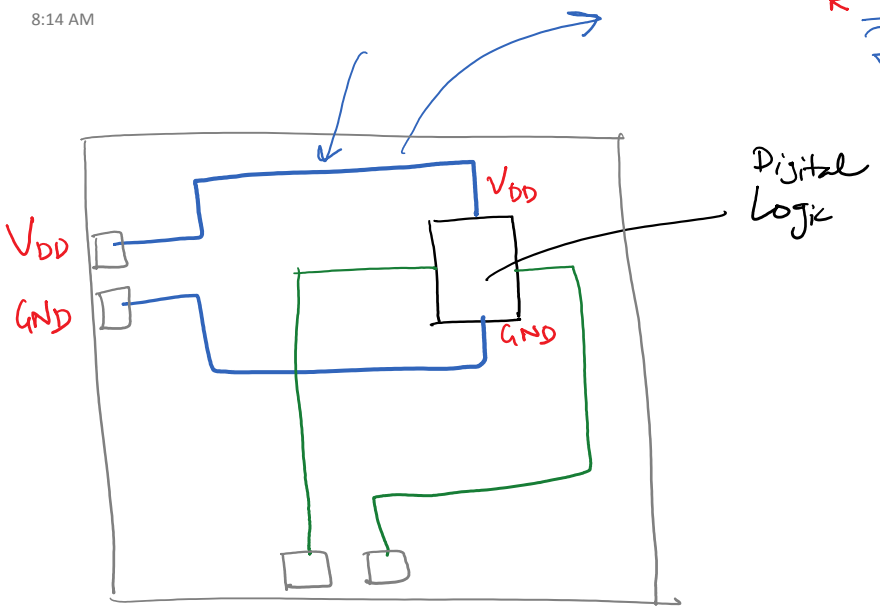


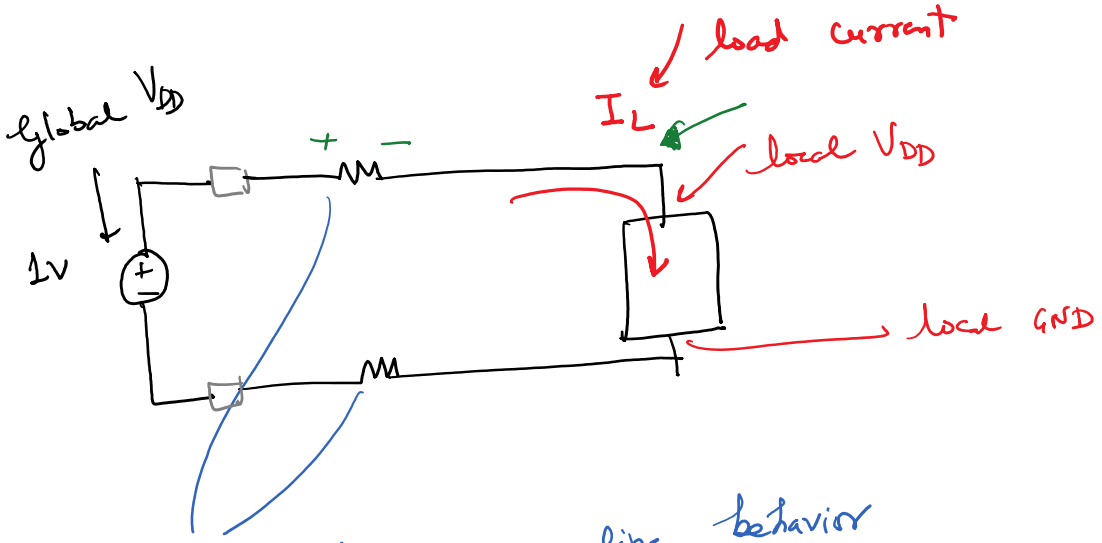


* Cross coupling or Crosstalk due to Metal-metal

Capacitance.







⇒ Assume RC transmission line behavior

$L = 10\ mm$

$N = \frac{10\ mm}{150\ mm} = 0.15\ \mu m$

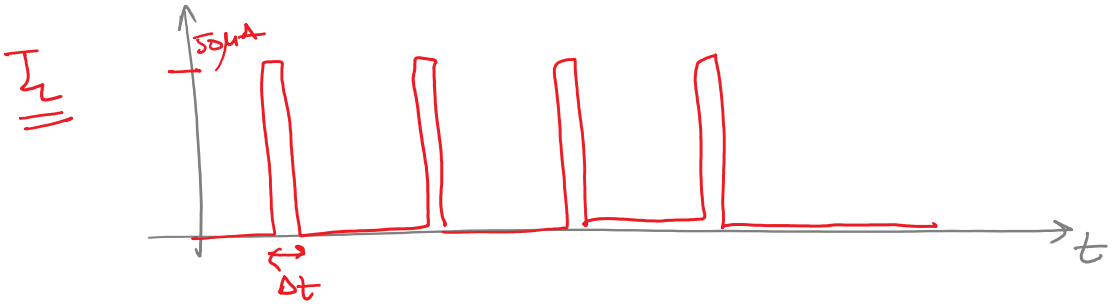
$R_\square = 0.1\ \frac{\Omega}{\square}$

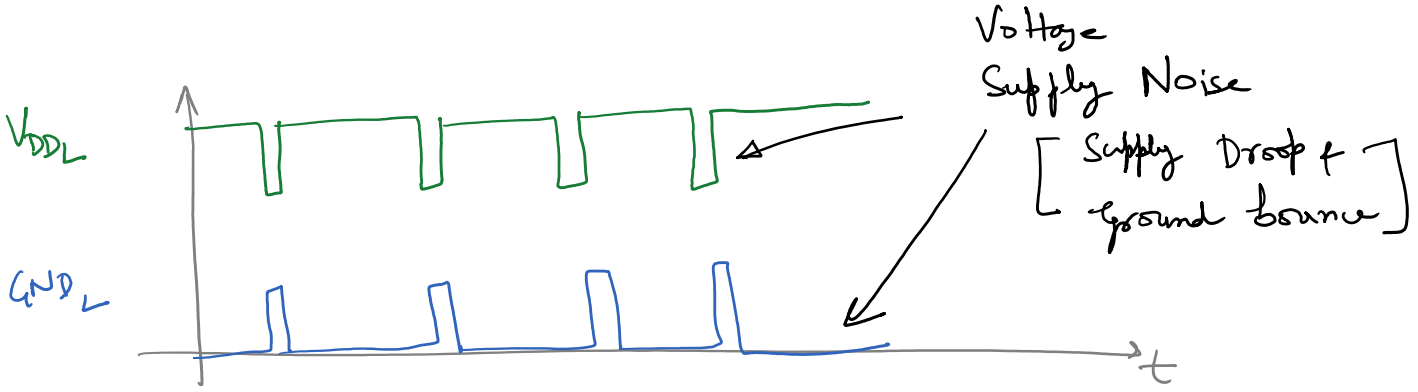
$R_W = 0.1 \times \frac{10 \times 10^{-3}}{150 \times 10^{-9}} = 6.67\ k\Omega$

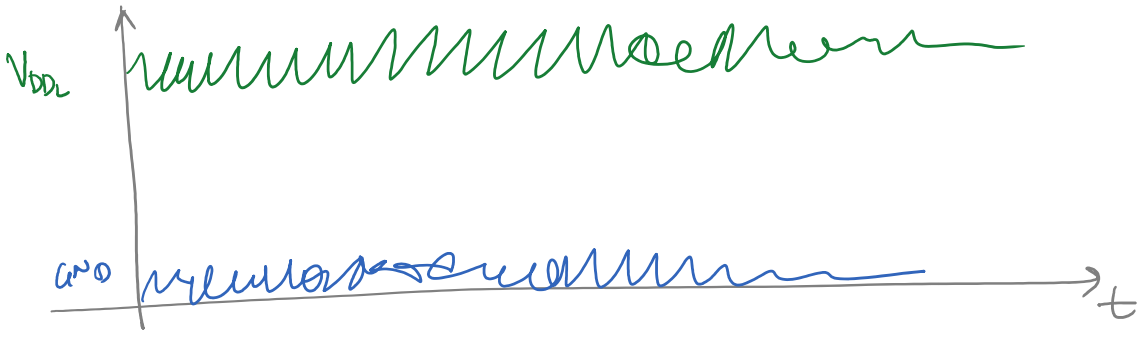
DC: $I_L = 50\mu A$

local $V_{DD} = V_{DD,L} = V_{DD} - I_L \cdot R_W = 667mV$

local $GND = GND_L = 0 + I_L \cdot R_W = 333mV$

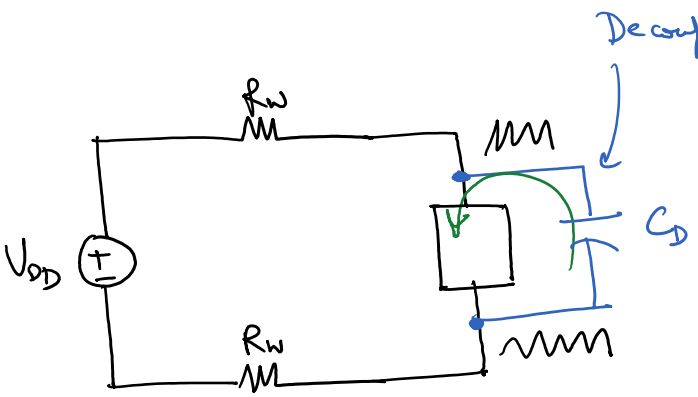


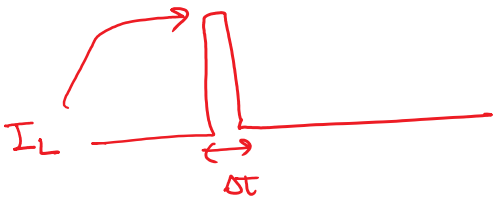




ASICs ⇒ Power & Signal Integrity Tools

Decoupling Capacitors





Assuming that the instantaneous charge is entirely provided by the cap C_D

$$\Delta Q = I_L \cdot \Delta t$$

$\Rightarrow$

$$\Delta Q = I_L \cdot \Delta t = C_D \cdot \Delta V$$

$\Rightarrow$

$$\Delta V = \frac{I_L \cdot \Delta t}{C_D}$$

ripple in the supply voltage between local V_{DD} & GND.

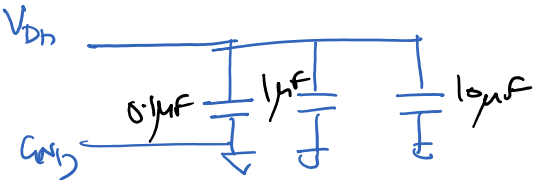
Ex. $I_L = 50\mu A$, $\Delta t = 10ns$

$\Delta V \leq 10\,mV$

$\Rightarrow \quad C_D > \frac{I_L \cdot \Delta t}{\Delta V} = 50pf$ typically is 1pf

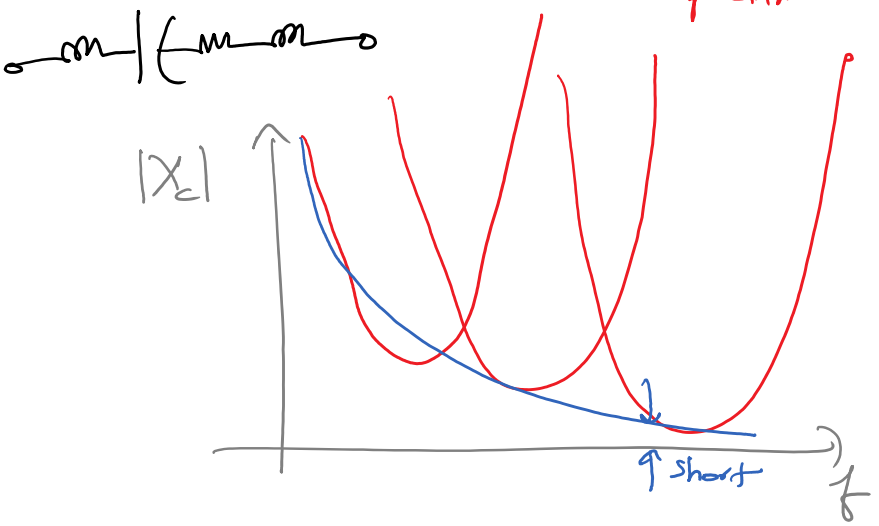
"MOSCAP"

* High-Speed Digital Design: A book of Black Magic



Surface Mount.

$Z = \frac{1}{j\omega c}$



Rule of thumb ⇒

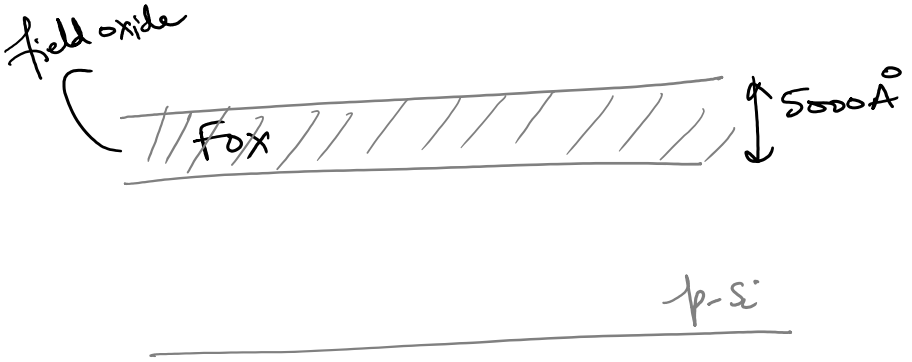
<1Ω impedance with the capacitor at the frequencies of interest for decoupling.

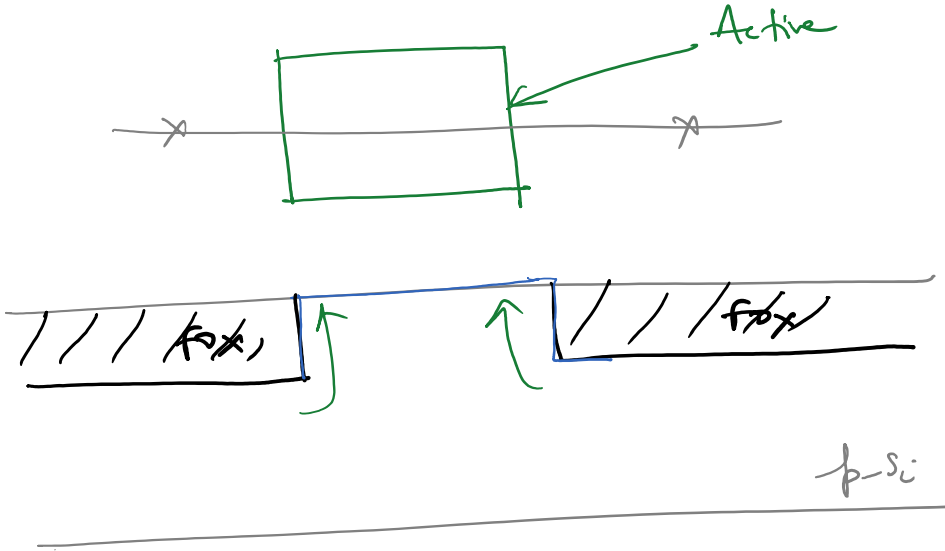
Monday, January 28, 2019 8:47 AM

Chapter 4: Active Layers

n-well
M1, M2, M3. ---
Via 1,2
glass

"Active layer"

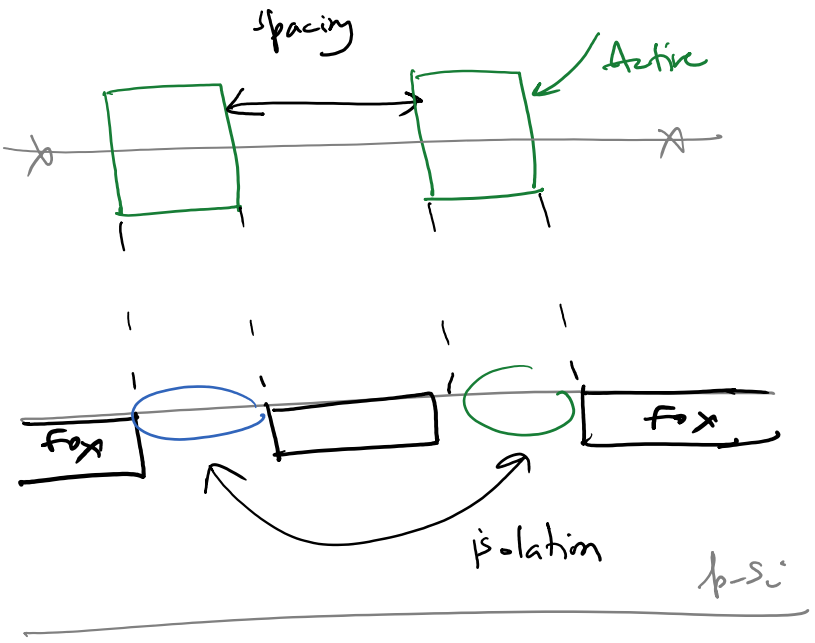




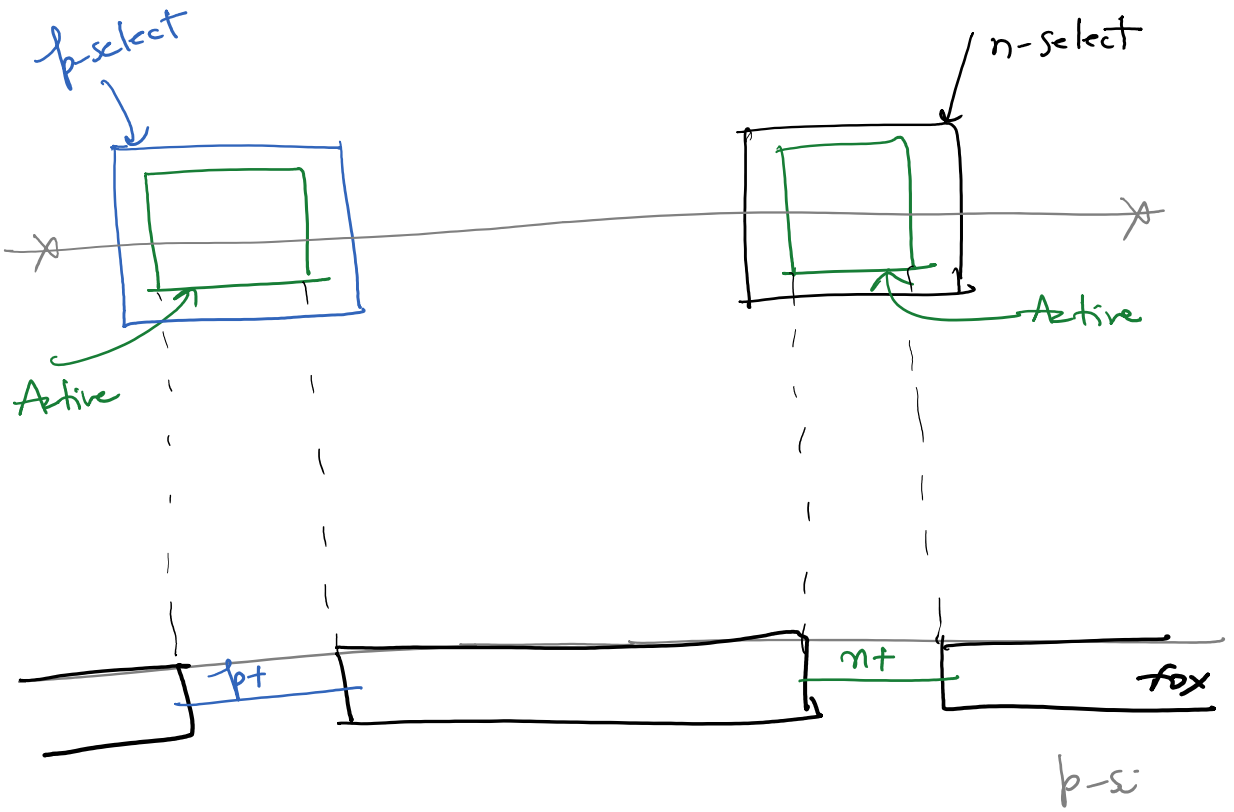
* Active layer opens a region in the field oxide
  ↳ where all transistors are created.

* FOX is used to isolate devices from one another

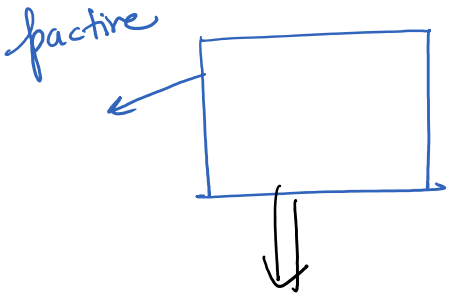
↳ thick enough to keep interaction of adjacent areas to a minimum.

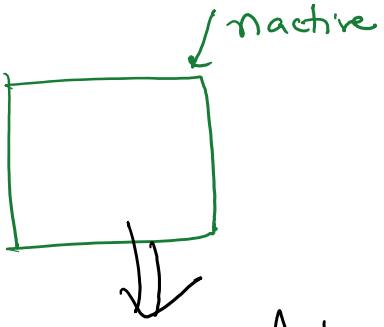


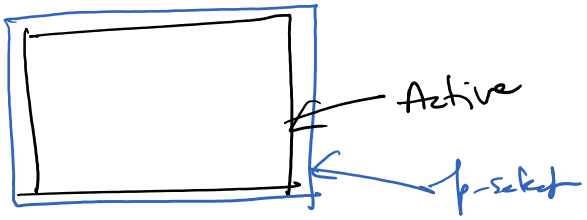
p and n select layers:

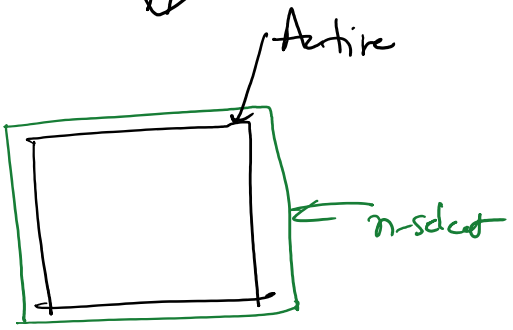


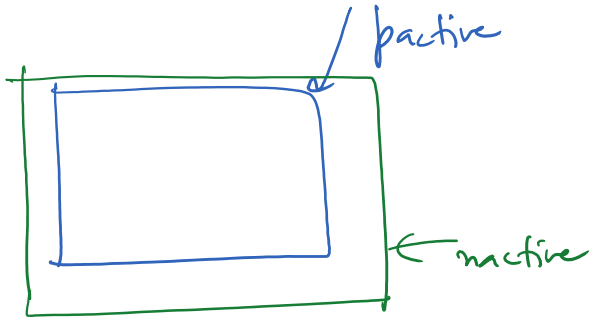
In Cadence







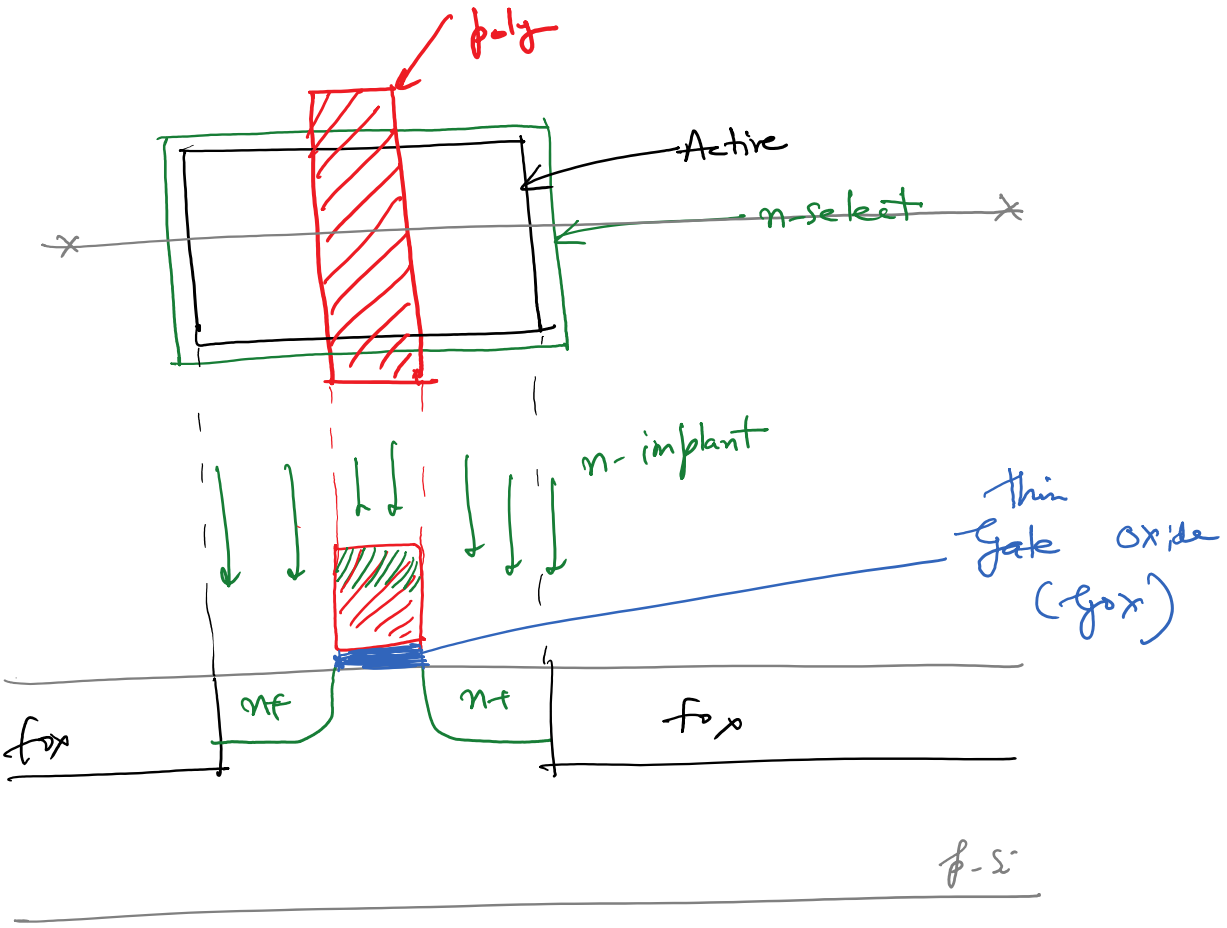



pactive
nactive

Poly Layer:

polysilicon layer is used for MOSFET formation

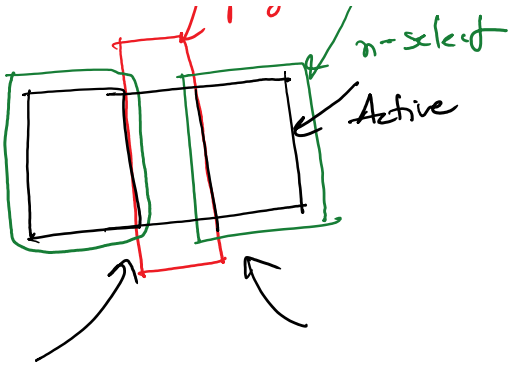
↳ "Poly" acts as a "mask" for the drain/source implants.

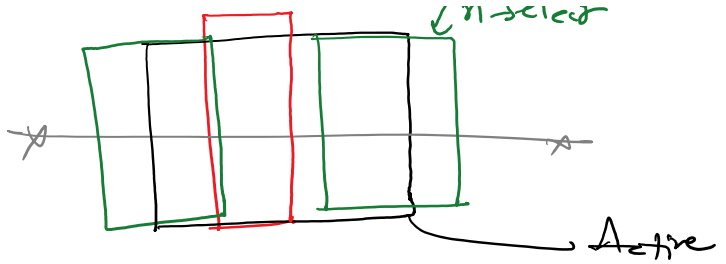


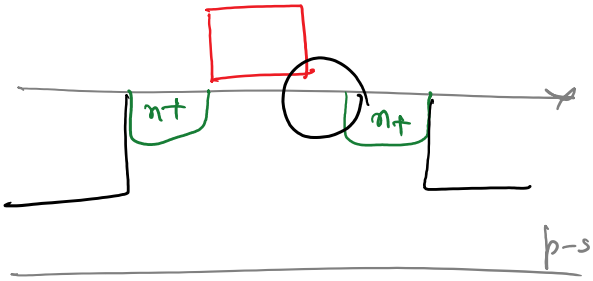
* Self-aligned gate process.

→ Poly over Active ⟹ MOSFET!

Problem Layout





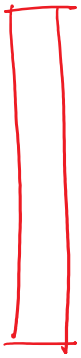


* Mask Misalignments

↳ poly overlap of source-drain region is not controllable

↳ Self-aligned gate is used by default.

poly.



* poly can be used like a wire for routing.
  - ↳ poly and active regions are "Silicided" by default.

Silicide => Cobalt or Tungsten + Silicon/polysilicon