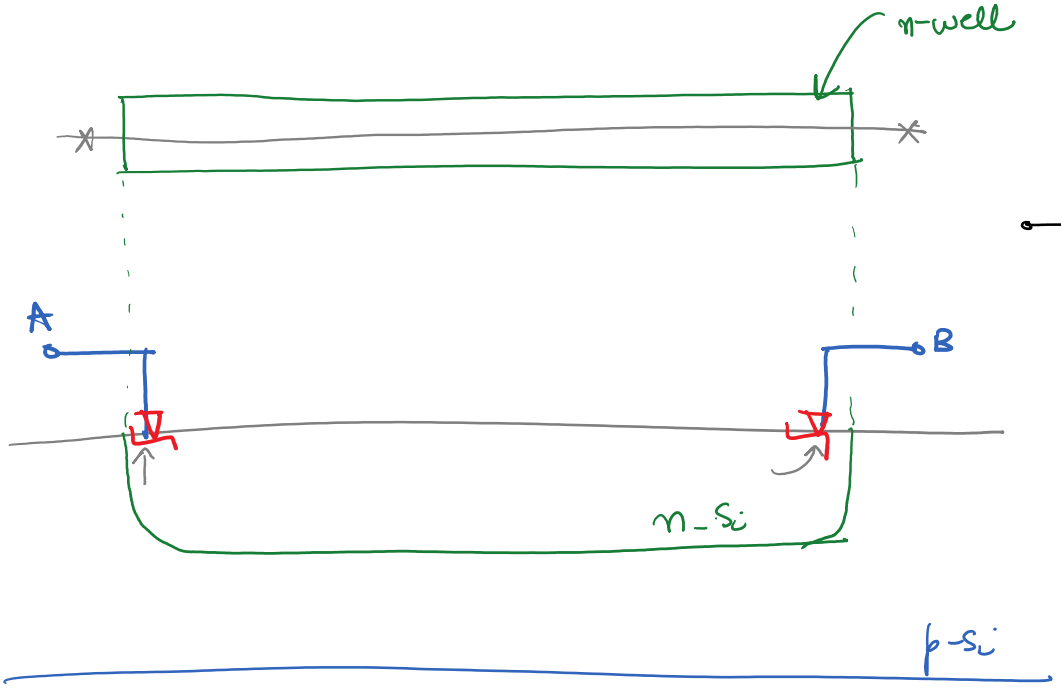
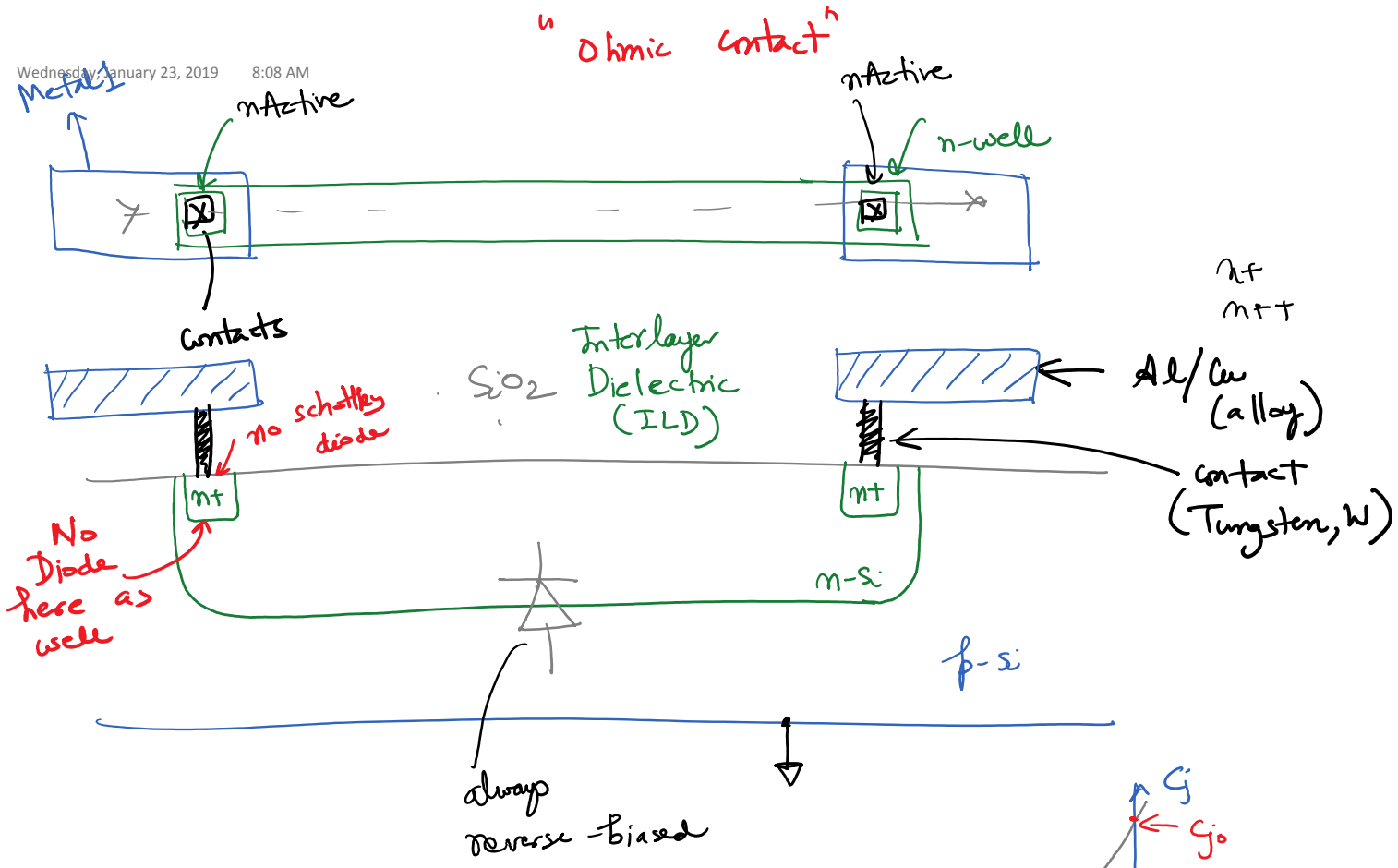
ECE 445 – Lecture 4

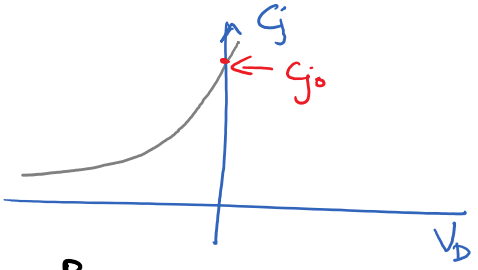
Wednesday, January 23, 2019 8:02 AM

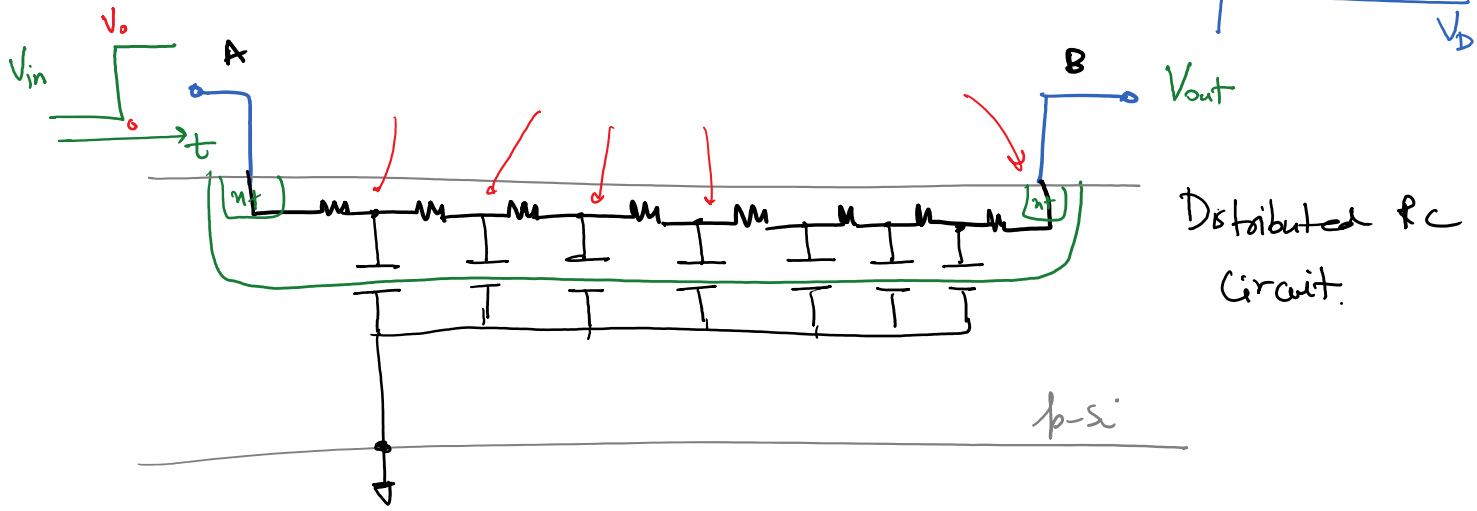


Non-ohmic contact

* Metal in contact with moderately or lightly doped Si forms a metal-semiconductor diode (schottky diode).

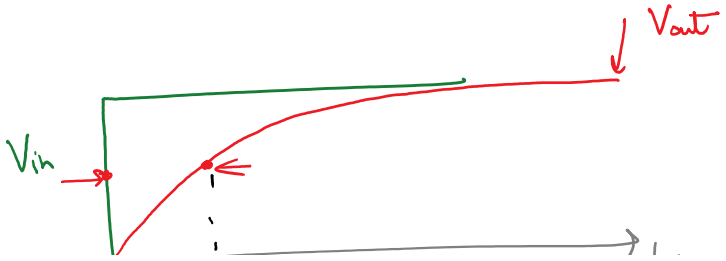




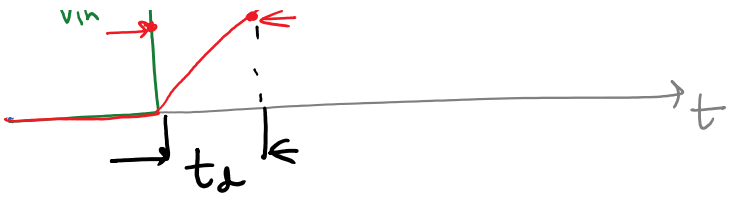


Distributed RC Circuit

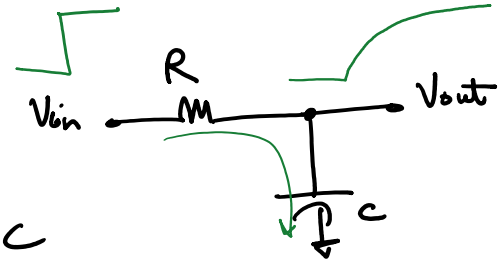
* forms an RC transmission line



RC charging waveform

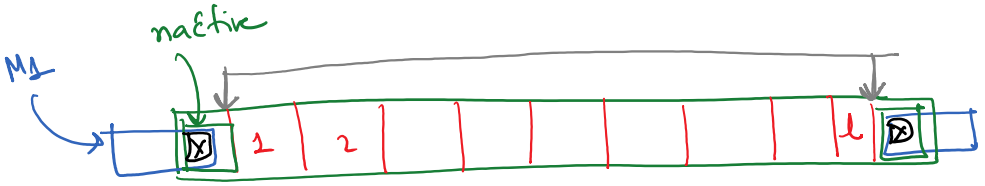


* Lumped RC circuit



$$t_d = 0.7RC$$

Distributed RC Delay :



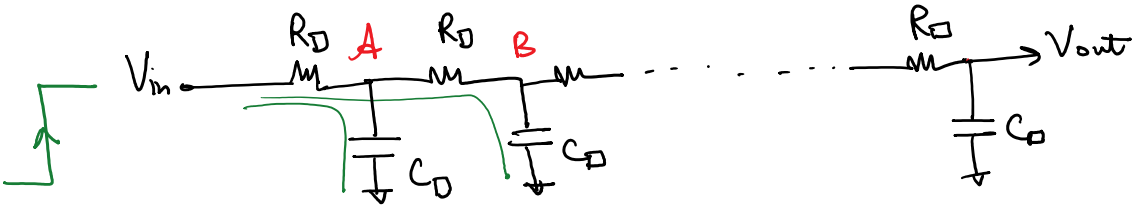
l squares

Resistance per unit square

$R_\square$

$C_\square$

↑ Capacitance p.u. square



delay to node-A $\Rightarrow$ $t_{dA} = 0.7 R_\square C_\square$

" " node-B $\Rightarrow$ $t_{dB} = 0.7 (R_\square C_\square + \overline{2R_\square} C_\square)$

Elmore delay

delay after l-sections $\Rightarrow$

$$t_{de} = 0.7 \left[R_\square C_\square + 2R_\square C_\square + 3R_\square C_\square + \cdots + lR_\square \cdot C_\square \right]$$

$$= 0.7 R_\square C_\square \left(\sum_{n=1}^{l} n \right)$$

$\rightarrow \frac{l(l+1)}{2} \approx \frac{l^2}{2}$ for a large-l

$$\simeq 0.7 R_D C_D \cdot \frac{l^2}{2}$$

$$= 0.35 R_D C_D l^2$$

$$= 0.35 (R_D \cdot l) \times (C_D \cdot l)$$

($R_D \cdot l$): ref resistance; ($C_D \cdot l$): total capacitance

$$\boxed{t_d = 0.35 \cdot R_{tot} \cdot C_{tot}}$$

(not $0.7 RC$) ?

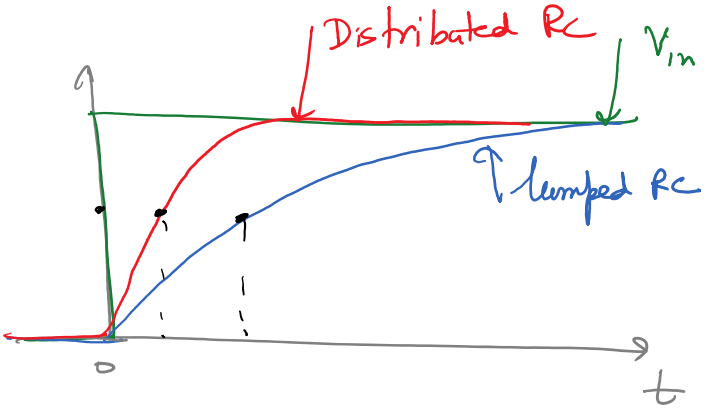
↳ because of the distributed nature of the RC line.

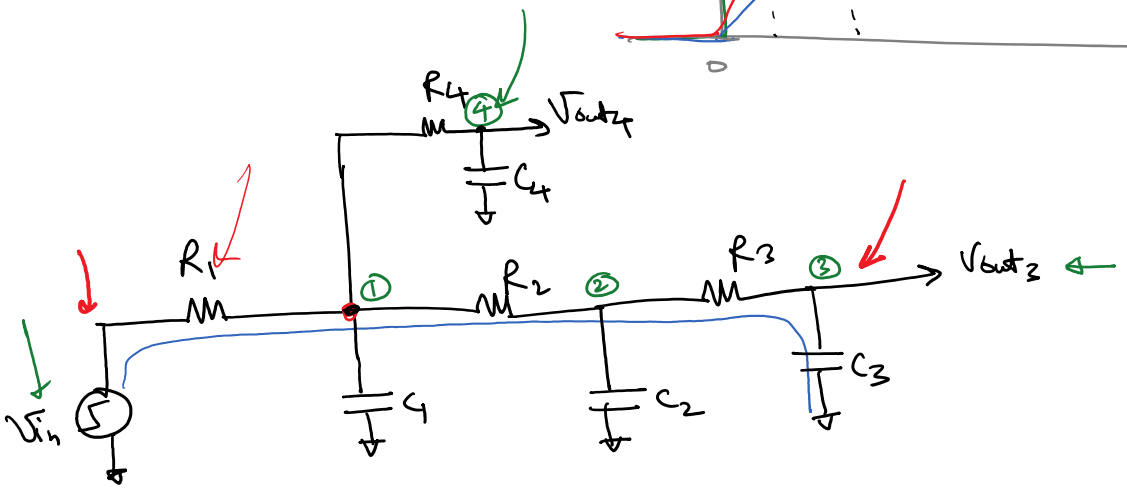
$= \frac{1}{2}$ of the lumped RC delay

90% rise time

$t_r \simeq 1.1 R_{tot} C_{tot}$

Elmore Delay :





Elmore delay to any node i of an RC tree is given by

$$T_{D_i} = \sum_{k=1}^{N} R_{ki} \cdot C_k$$

Where $N \Rightarrow$ total number of nodes in the tree

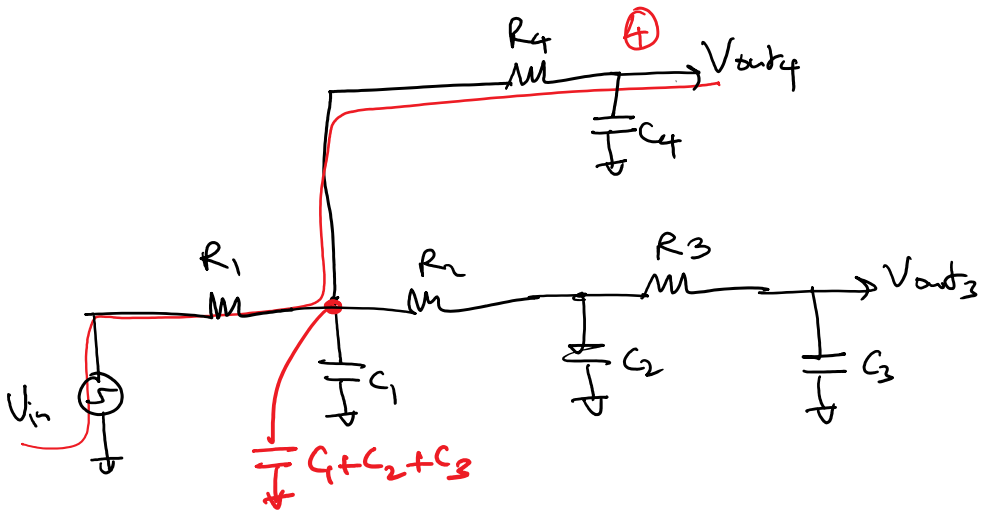
$C_k =$ Capacitance on node-k

$R_{ki} =$ Resistance between the input and node 'k' in common with the path between the input and node i.

Elmore delay

$$T_{D_3} = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + R_1C_4$$

Not $(R_1+R_4)C_4$



No loops

$$T_{D_4} = R_1C_1 + R_1C_2 + R_1C_3 + (R_1+R_4)C_4$$

* In RC trees, capacitance on branches away from the path

to the output are lumped as if they were present at the branching point on the path

* Relation between propagation delay and the Elmore delay?

$t_d = 0.7 \times T_D$

↑ Elmore delay

90% rise time $t_r = 2.2 \times T_D$

ASIC → Application Specific IC

↑

FPGA →

Cadence / Synopsys

ASIC Design flow → Synthesis

↳ Custom Design flow

Nwell active — later

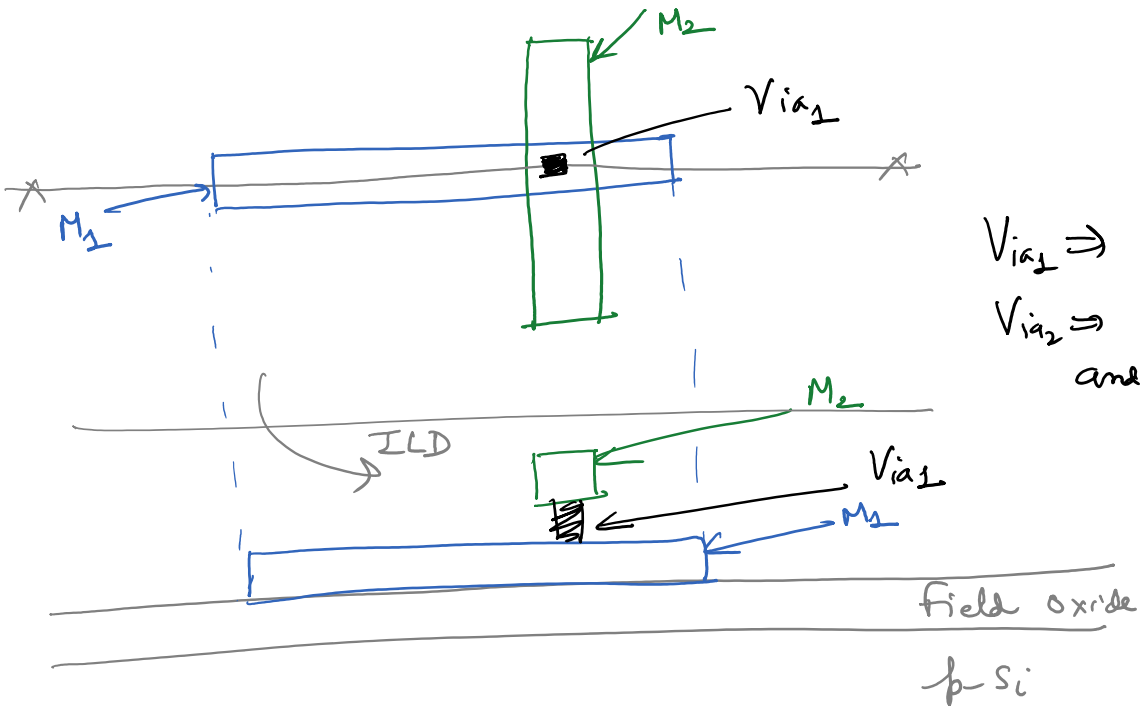
Metal layers :

⇒ Used to connect circuit elements and to the I/O

↳ several layer of Metals → Metal stack

On Semi C5 ⇒ 3-Metal

≥ 8 layers in Commercial CMOS.



Via_1 ⇒ M_1 & M_2

Via_2 ⇒ M_2 & M_3

and so on

Metal layer properties

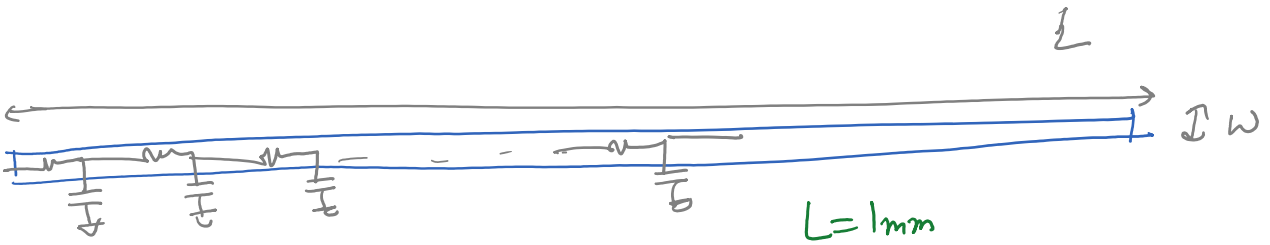
* Delay
* Electromigration (degradation of metal wires)

* characterized by the sheet resistance

$R_S \simeq R_\square$ is much lower than n-well resistance

$\simeq 0.1 \frac{\Omega}{\square}$

* Contact (via) resistance $\simeq$ 10-50 Ω/per via



$L = 1mm$
$W = 200nm$
$R_S = 0.1\,\Omega/\square$

$$R = R_S \cdot \frac{L}{W} \equiv R_\square \frac{L}{W}$$

$$= 0.1 \times \frac{10^{-3}}{200 \times 10^{-9}} = 500\Omega$$

Capacitance [Table 3.1]

$$C_{tot} = \underbrace{(1000 \times 0.2)}_{\text{area}} \times 23 \frac{aF}{\mu m^2} + \underbrace{(2000 + 0.4)}_{\text{perimeter}} \times 79 \frac{aF}{\mu m}$$

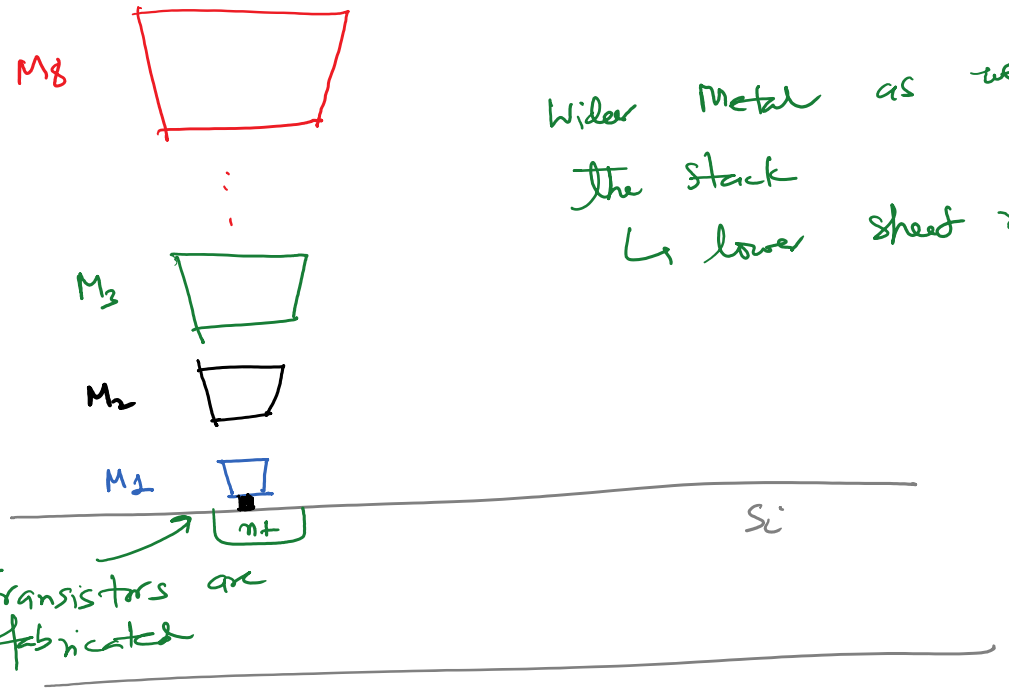
$\rightarrow = 162\ fF$

$\Rightarrow$ Distributed RC delay in the metal wire 10^{-12} s

⇒ Distributed RC Delay in one

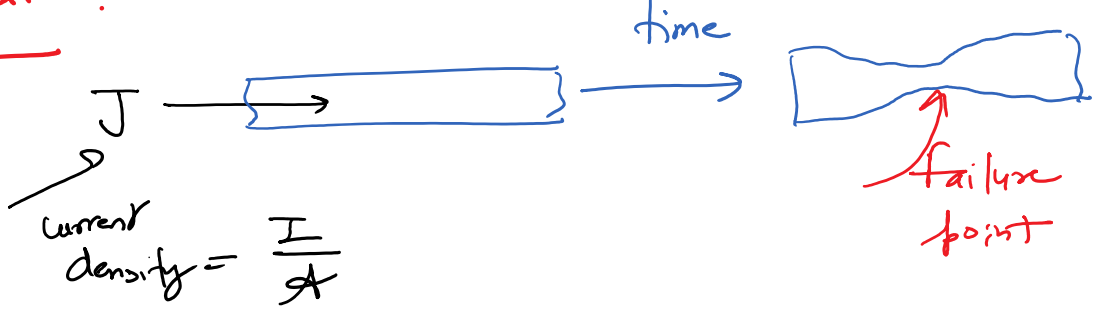
$$t_d = 0.35 \cdot R_{tot} \cdot C_{tot}$$

$$= 0.35 \times 500 \times 162\,ff = \underline{28\,ps} \quad (10^{-12}\,s)$$



Wider Metal as we go higher in the stack
↳ lower sheet resistance

Electromigration:



Process datasheet ⇒ J ← max. current density is set by Electromigration

⇒ Wider wires for large currents