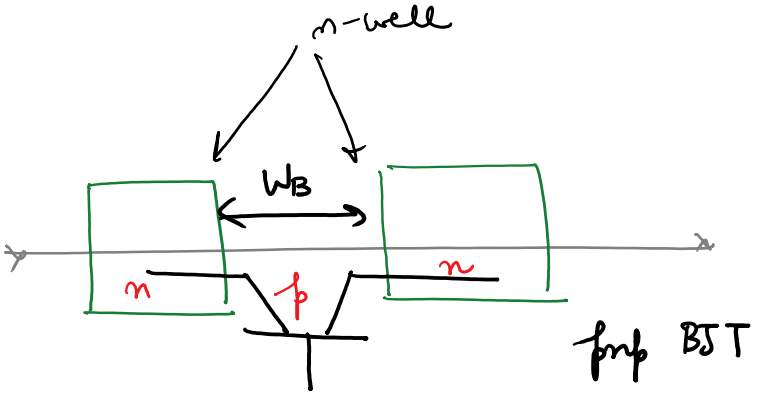
ECE 445 - Lecture 3

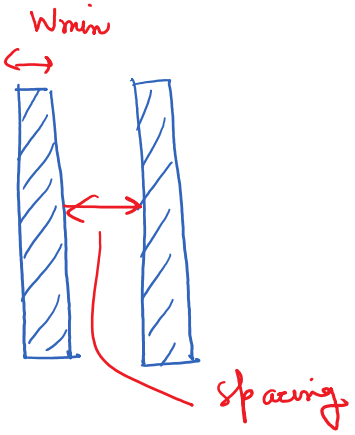
Wednesday, January 16, 2019 8:02 AM

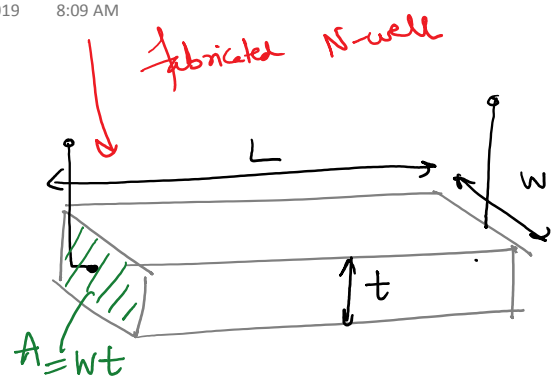


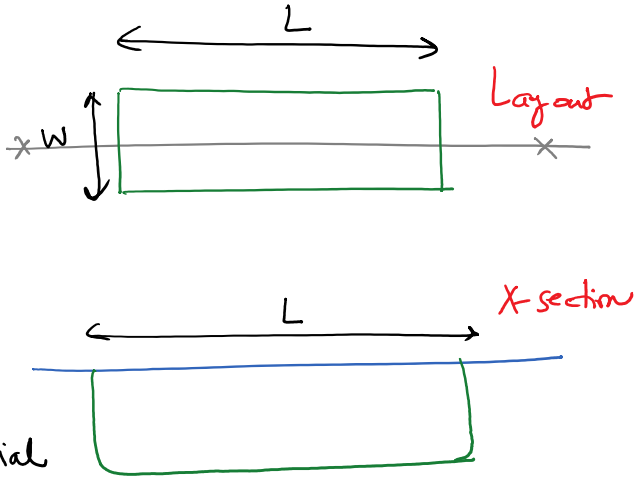
pnp BJT

$W_B \uparrow \Rightarrow \beta \downarrow$

* Minimum spacing rules
  - Design rules set by the process and device engineers to guarantee proper operation of the fabricated circuits







resistivity, ρ ⇒ property of the material (Si) and doping

$$R = \rho\frac{L}{A} = \rho\cdot\frac{L}{W\cdot t} = \underbrace{\left(\frac{\rho}{t}\right)}_{R_\square}\cdot\frac{L}{W} = R_\square\cdot\frac{L}{W}$$

$R_\square$ → sheet resistance

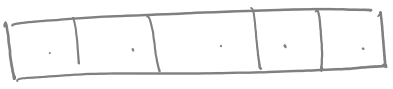
$$R_\square = \frac{\rho}{t}$$

Ex. N-well resistor

$10\,\mu m$ (W) × $100\,\mu m$ (L)

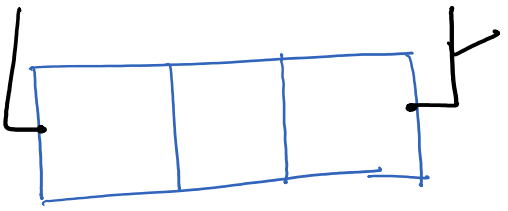
$R_\square = 2\,k\Omega$ / square

$$R = R_\square\cdot\frac{L}{W} = 2k\Omega\times\frac{100\,\mu m}{10\,\mu m} = 20k\Omega$$



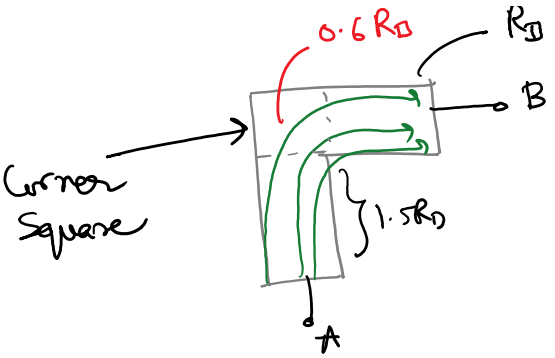
R = # of □'s × $R_\square$

$= 5R_\square$



$R = 3R_\square$

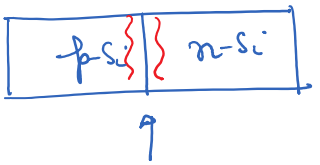
Resistance value is defined by the $\left(\frac{L}{W}\right)$ ratio or the number of squares



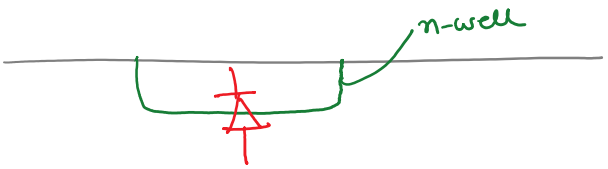
$\Rightarrow \quad 2.5R_D + 0.6R_D = 3.1R_D$

ECE 310

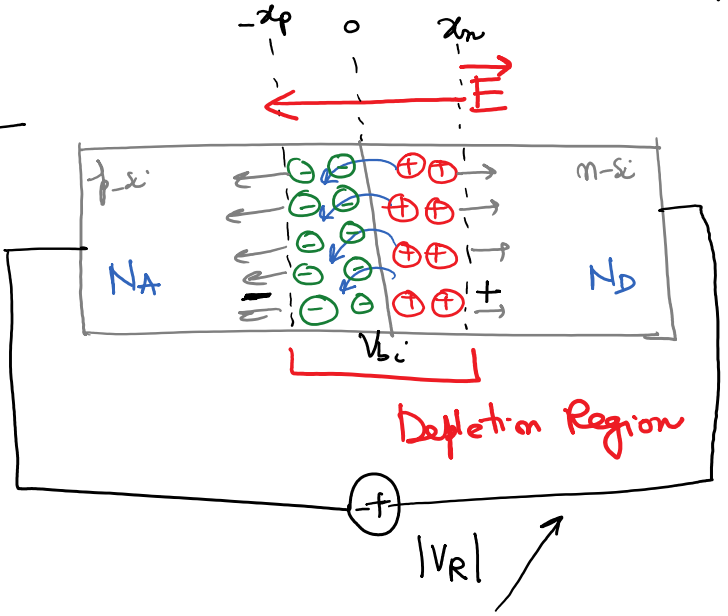
PN Junctions:

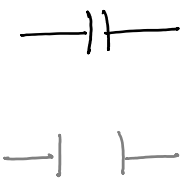


q



Reverse-Bias Condition





$C = \frac{\varepsilon \varepsilon_r A}{d}$

In Equilibrium:

$np = n_i^2$ — $n_i \Rightarrow$ intrinsic carrier density

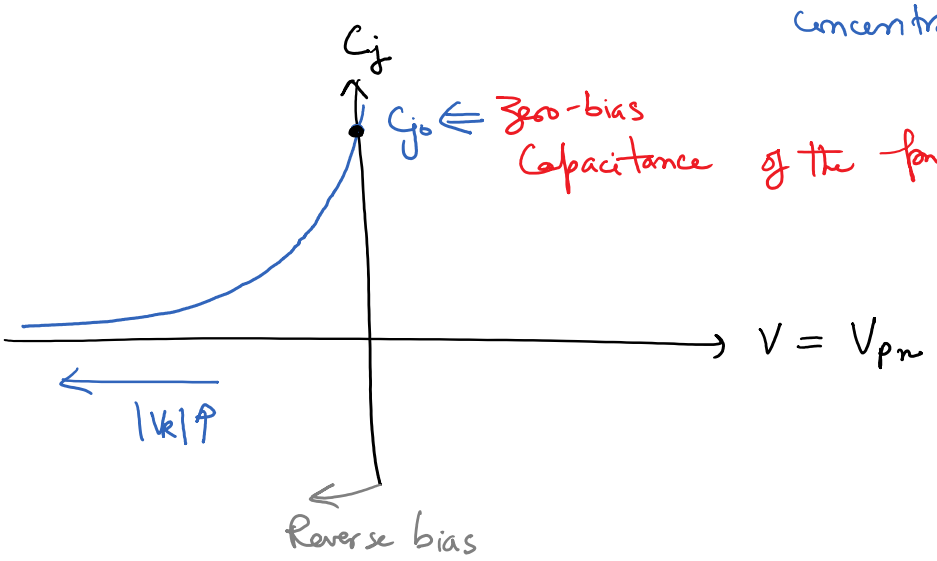
- n: free electron density
- p: hole density

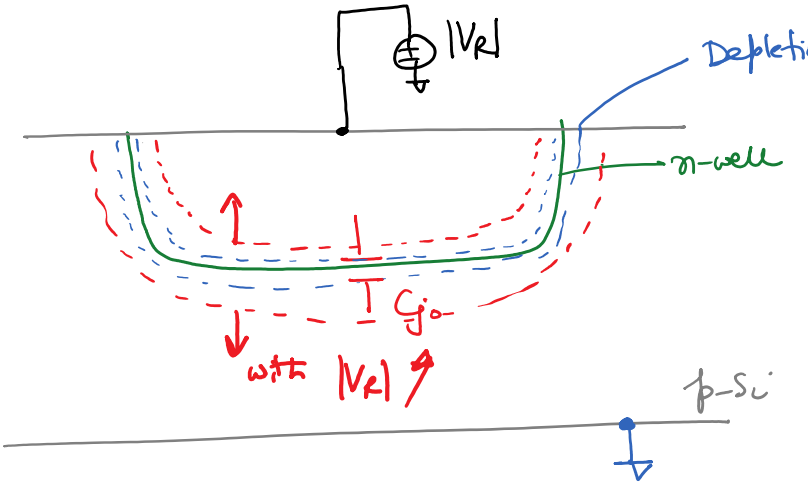
Built-in potential, $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$

$N_A \Rightarrow$ Acceptor type Doping concentration (p-Si)

$N_D \Rightarrow$ Donor type Doping.

Concentration (n-Si)

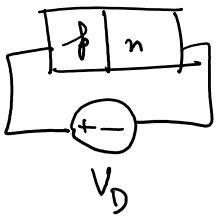




$C_j \downarrow$ as $|V_R| \uparrow$

$$C_j = \frac{C_{j0}}{\left(1 + \frac{|V_R|}{V_{bi}}\right)^m}$$

$$= \frac{C_{j0}}{\left(1 - \left(\frac{V_D}{V_{bi}}\right)\right)^m}$$



C_{j0} ⇒ Zero-bias Capacitance at the pn junction

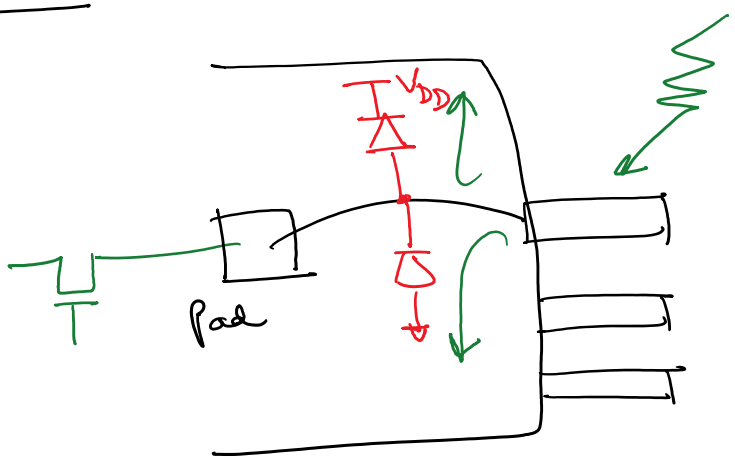
V_D ⇒ voltage across the diode

m ⇒ grading coefficient of the junction

V_{bi} ⇒ built-in potential of

the pn junction

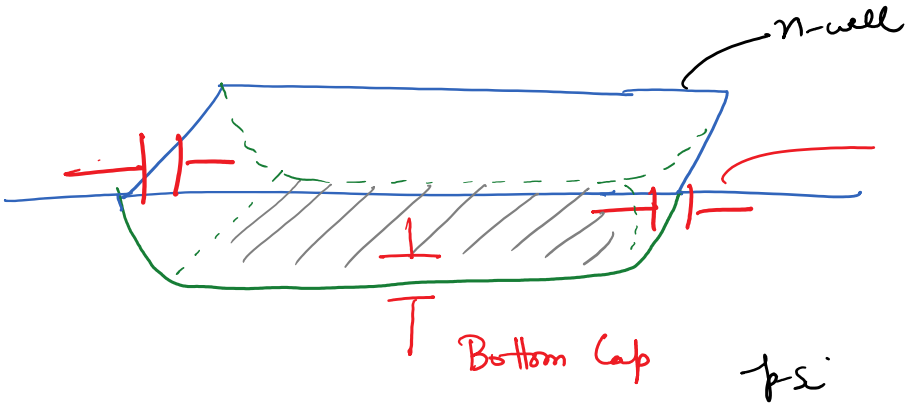
ESD: Electrostatic Discharge



ESD Diode.

⇒ Part of the I/O Design

n-well resistance used here



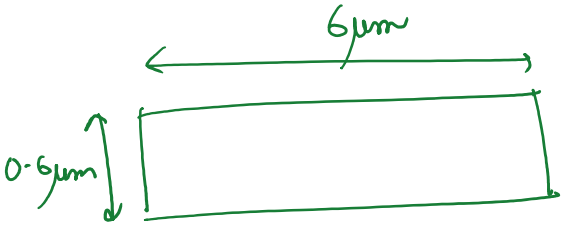
psi

$$C_j = \frac{C_{jb}}{\left(1-\frac{V_D}{V_{bi}}\right)^m} + \frac{C_{js}}{\left(1-\frac{V_D}{V_{bi}}\right)^m}$$

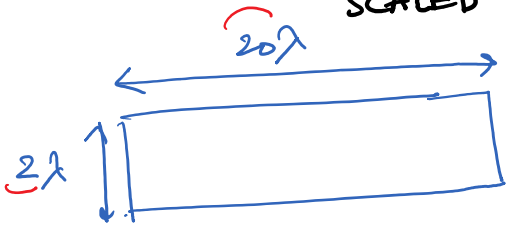
$C_{jb} = \frac{Cap}{Area} \times$ bottom-area $= Cap\left(\frac{fF}{\mu m^2}\right) \times (L \times W)$

$C_{js} = \left(\frac{Cap}{length}\right) \times$ (perimeter of the n-well) $= Cap\left(\frac{fF}{\mu m}\right) \times (2L + 2W)$

CADENCE



SCALED RULES (BOOK)



$\lambda \Rightarrow$ process scaling factor

On Semi: CS, $\lambda = 0.3\mu m$

from the Book:

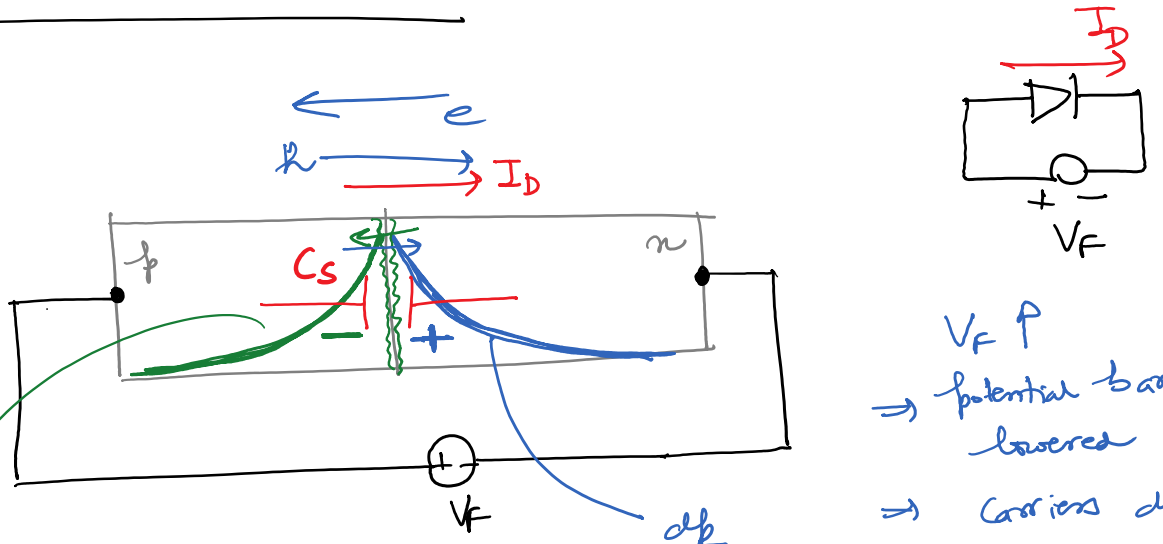
Using scaling factor (λ)

$C_{jb} = \frac{Cap}{Area} \times (scale)^2$. (bottom area in relative quantities)

$G_{ob} = \frac{Cap}{Area} \times (\quad)$

$G_{os} = \left(\frac{Cap}{clay\,Th}\right) \times (Scale) \times \text{Perimeter}$

Forward bias Diode :



V_F ↑

⇒ potential barrier is lowered

⇒ Carriers diffusing

$\frac{dn}{dx}$

Concentration gradient for electrons

$\frac{dp}{dx}$

concentration gradient for the holes

Stored Charge (electrons + holes at the interface)

$$\Rightarrow \boxed{C_s = \frac{I_D}{n V_T} \cdot \tau_T}$$

Storage Capacitance

I_D = fwd bias current

$n \Rightarrow$ diode parameter

$V_T = \frac{kT}{q} \Rightarrow$ Thermal voltage

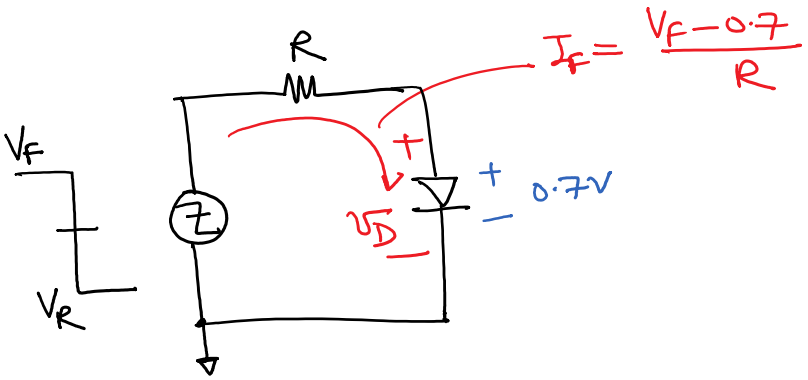
$\tau_T \Rightarrow$ transit time

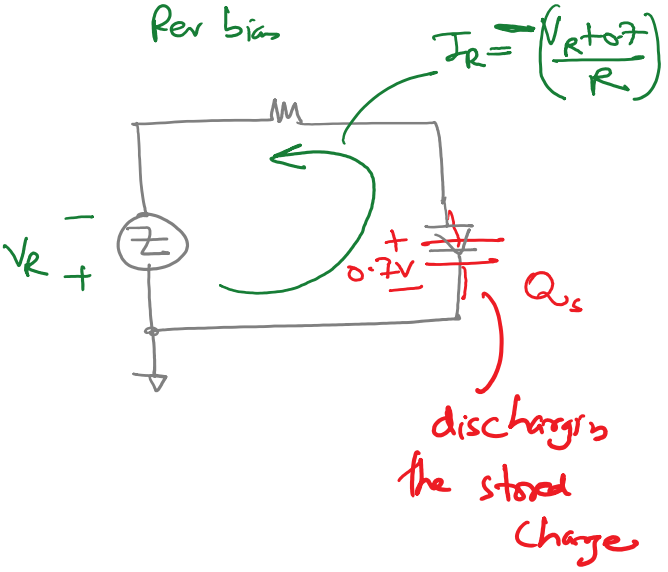
↳ ≃ 10 μs in Si

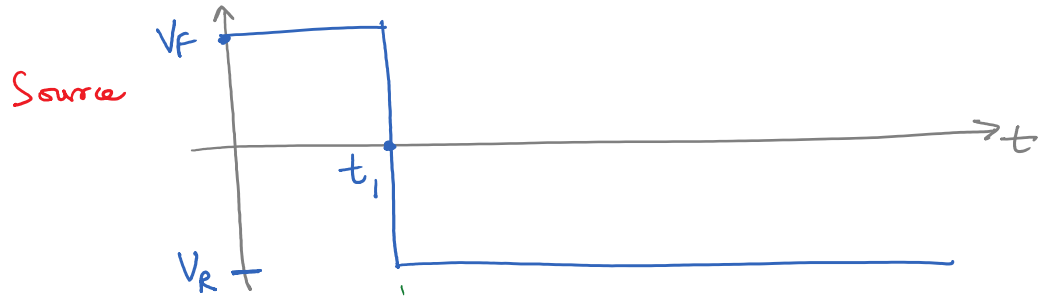
$$Q = C_s V_F$$

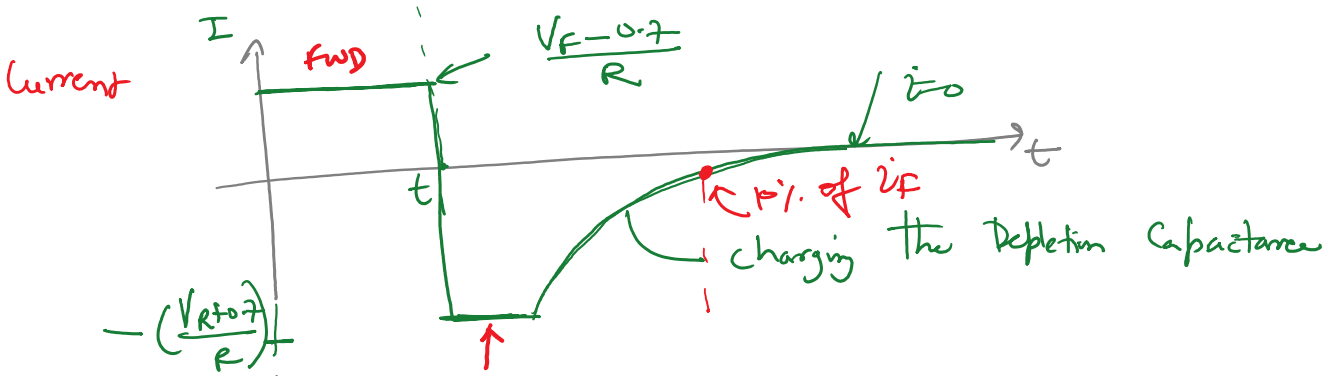
$C_s \gg C_{j,depletion}$

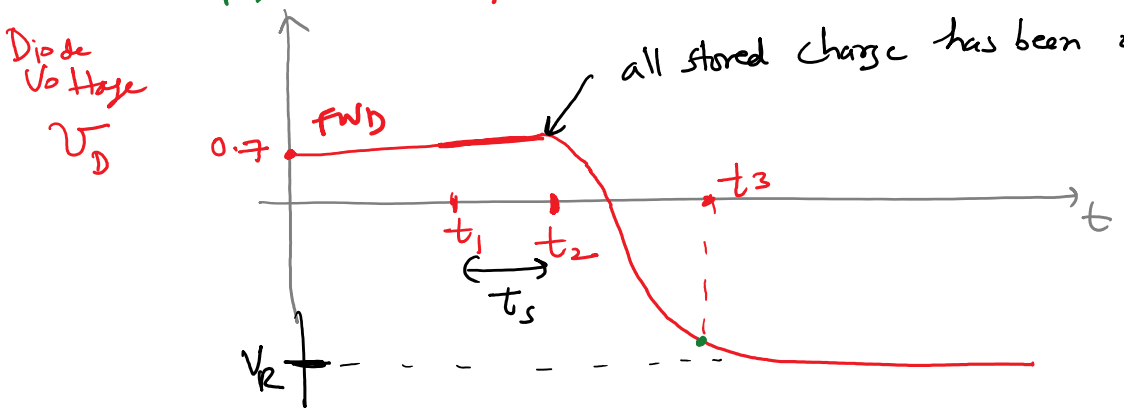
Reverse Recovery of Diode











$t_s = t_2 - t_1$ ∈ Storage time

i.e. time taken to remove storage charge

$t_{rr} = t_3 - t_1$ ⇐ reverse recovery time

$$t_s = \tau_T \cdot \ln\left(\frac{i_F - i_R}{-i_R}\right)$$