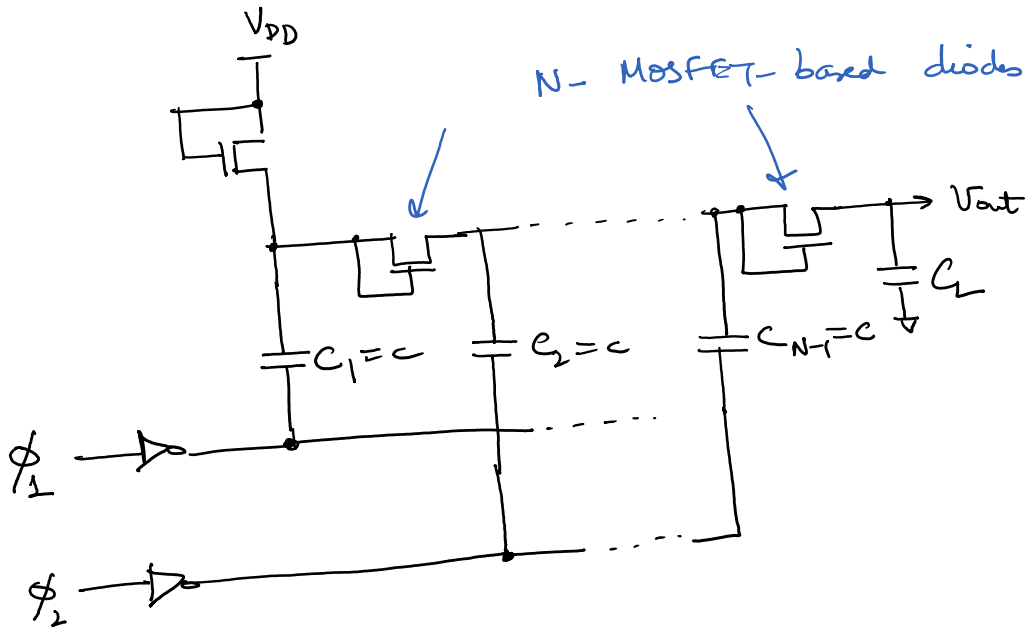
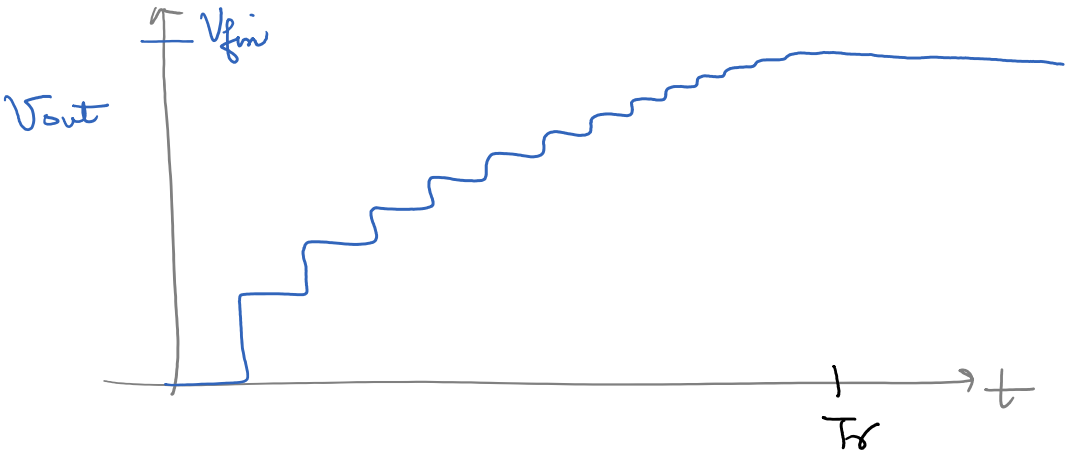
ECE 445 – Lecture 26

Wednesday, May 1, 2019 8:06 AM

N-stage charge pump





$T_r \Rightarrow$ ramp-up time

$$T_r = \frac{\ln\left[1 - \frac{V_{fin} - (V_{DD} - V_{TH})}{N(V_{DD} - V_{TH})}\right]}{\ln\left(\frac{1}{1 + \frac{C}{C_L}}\right)} \cdot T_{CLK}$$

$$V_{fin} = N\left(V_{DD} - V_{THN}\right)$$

↳ includes body effect

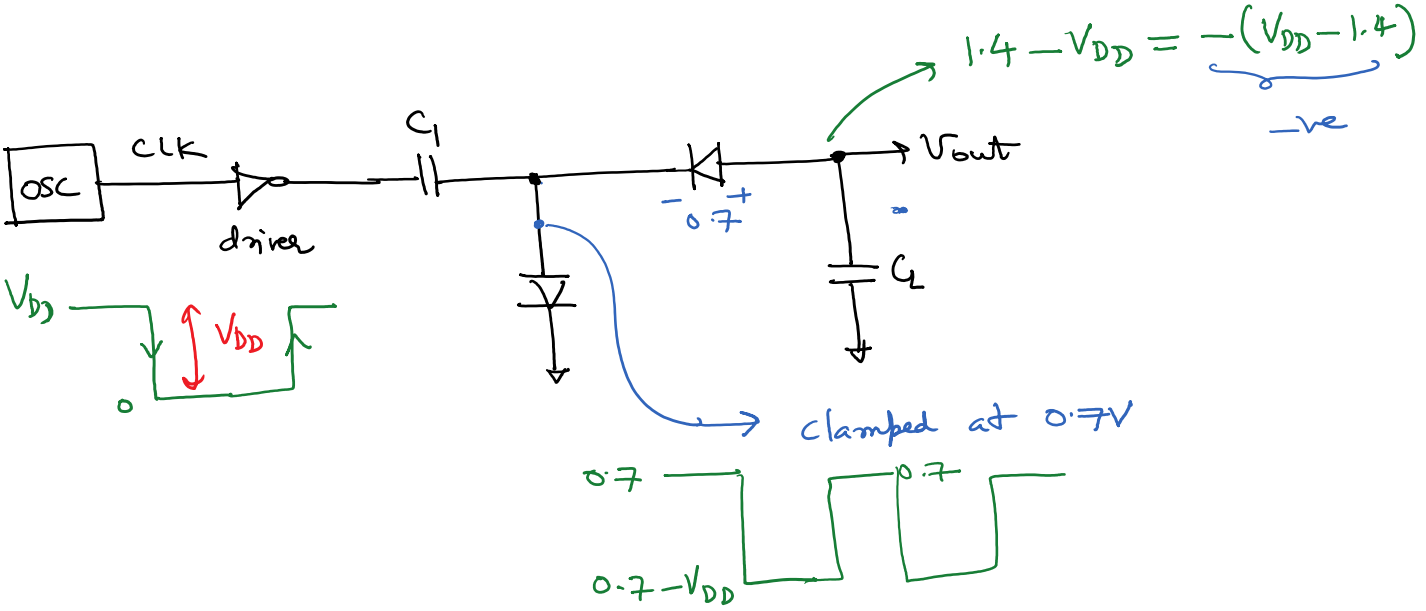
* Undesired $N \cdot V_{THN}$ drop can be mitigated by using a four-phase design.

Negative Voltage Charge pump:

* negative voltages are used in many applications
  - DRAM
  - digital logic with reduced leakage

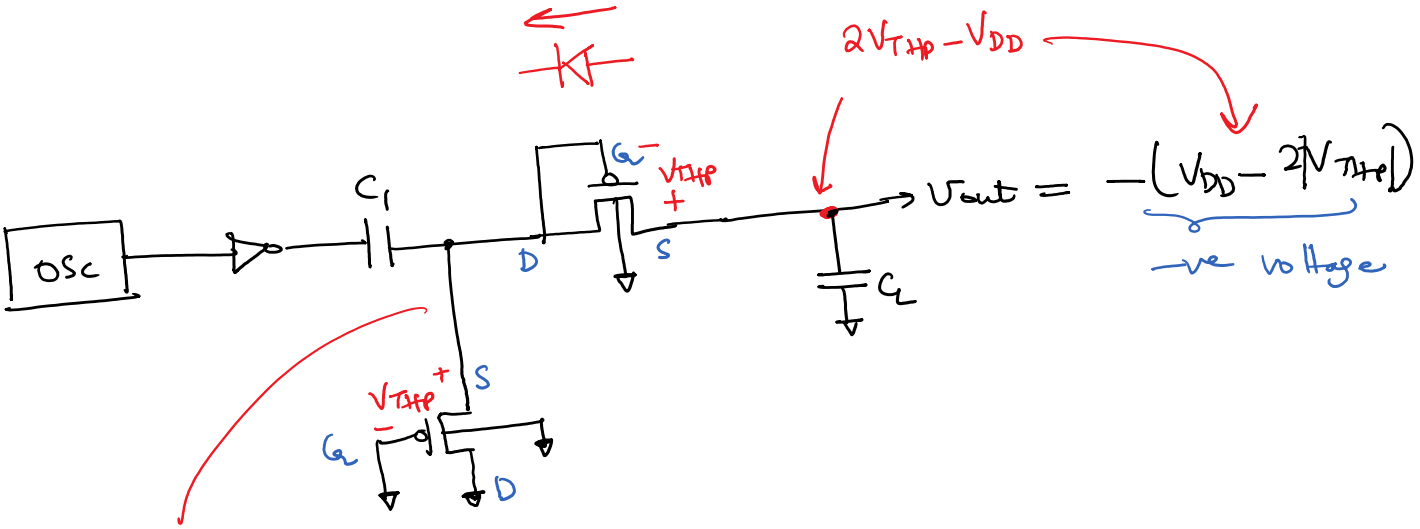
$V_{SB} \uparrow \rightarrow V_{THN} \uparrow \Rightarrow$ negative voltages (−0.5 V) for the bulk.

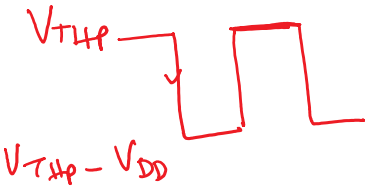
$V_S - V_B \rightarrow -ve$

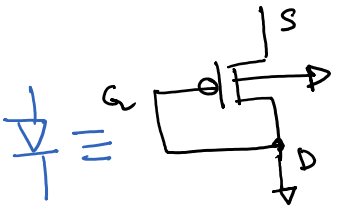


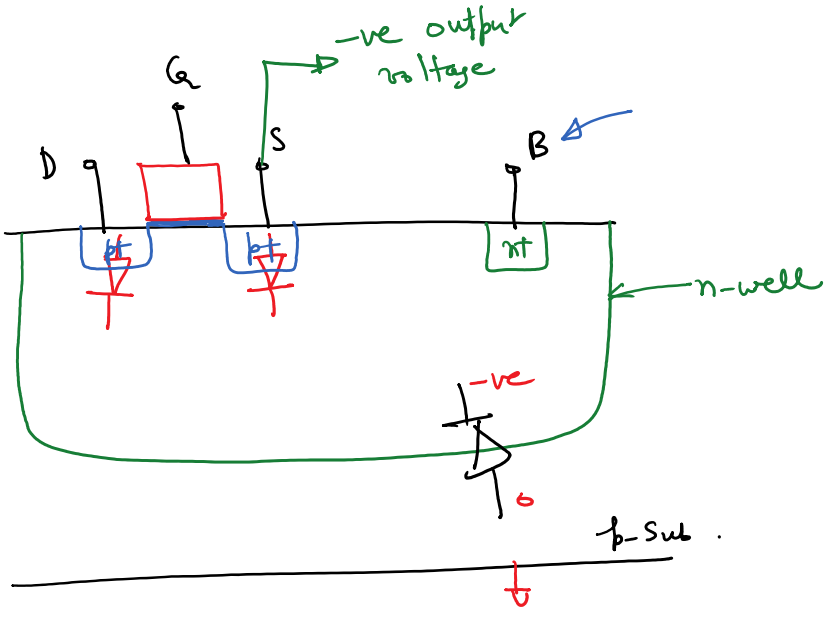
* Can't use NMOS as the negative voltage will forward bias the source/drain diods.
  - use PMOS

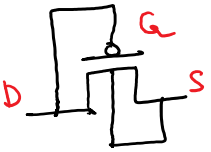
$2V_{THP} - V_{DD}$











* If we connect the n-well (body) to source
  ⇒ Body is negative
  ↳ n-well diode can turn on ✗

* If we connect the body to V_{DD} ✗
  ↳ very large body effect

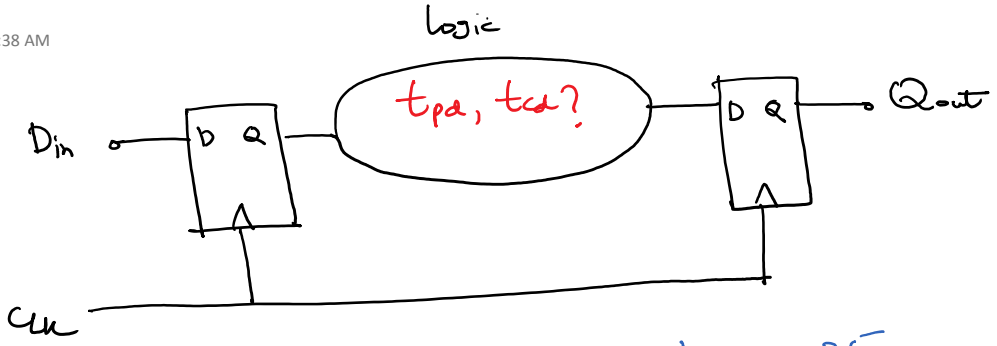
* As a compromise, its best to connect body to the ground ✓
  ↳ don't have severe body effect

In CS- 0.5µm CMOS ⇒ $V_{DD} = 5V$, $V_{THP} = 1V$

$\Rightarrow V_{out} = -3V$

$V_{DD} = 2.5V$
↳ $V_{out} = -0.5V$

Ex.



$t_{setup} = 100ps$

$t_{hold} = 50ps$

$t_{ccq} = t_{pcq} = 25ps$

$f_{clk} = 2GHz \longrightarrow T_{clk} = \frac{1}{2 \times 10^9} = 500ps$

Max-delay constraint:

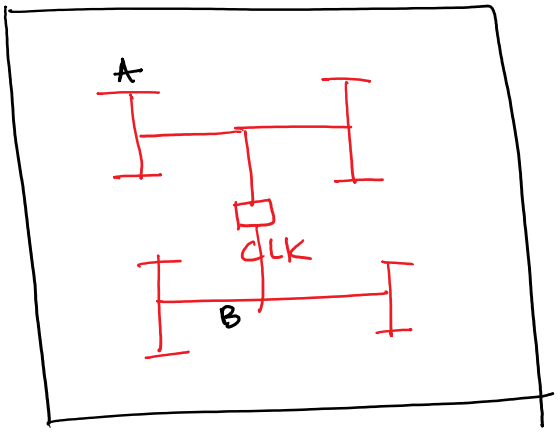
$$t_{pd} \leq T_{clk} - (t_{setup} + t_{pcq})$$
$$= 500ps - 100ps - 25ps$$
$$= 375ps$$

Min-delay constraint:

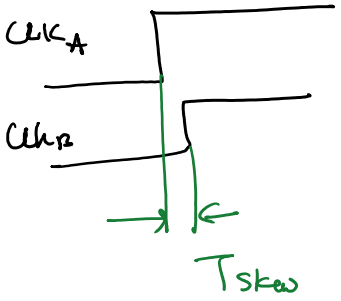
$$t_{cd} \geq t_{hold} - t_{ccq}$$ independent of clock
$$= 50ps - 25ps$$
$$= 25ps$$

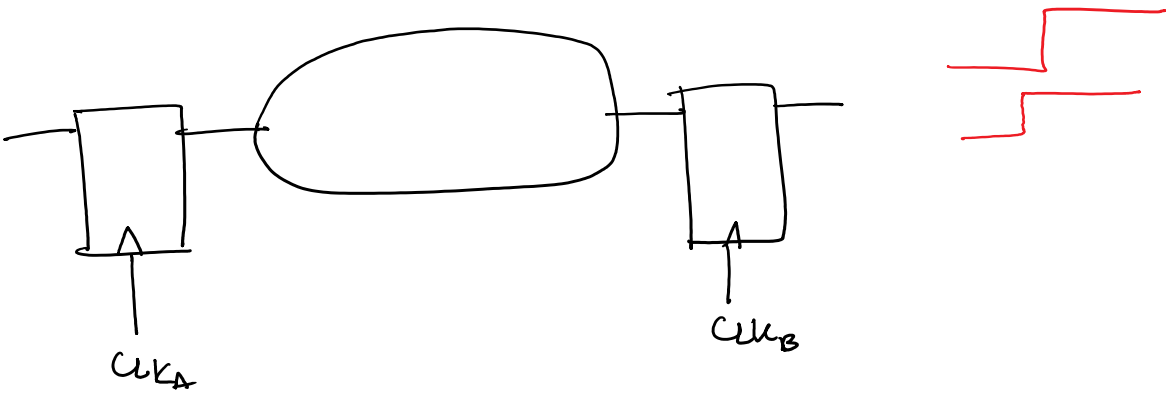
Clock Skew:

clock Tree



Clock skew.





Worst case Skew estimates:

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} - T_{skew})$$

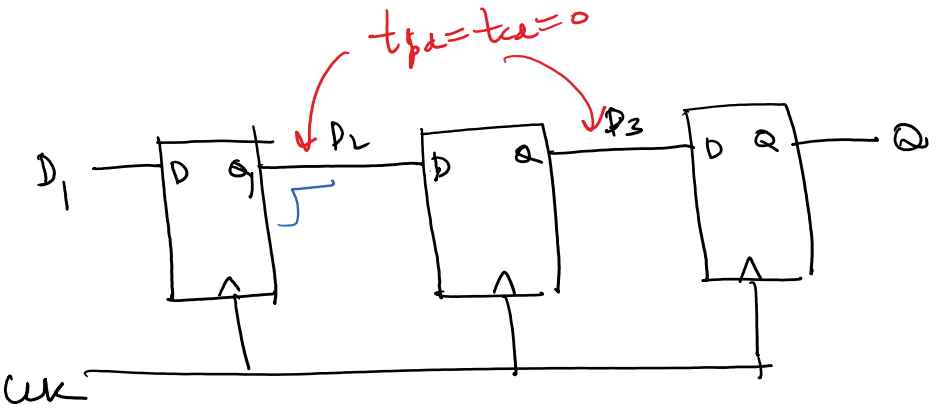
$$t_{cd} \geq t_{hold} - t_{ccq} + T_{skew}$$

t_{pd} ↓ t_{cd} ↑ with skew.

$\Rightarrow T_{skew} = 25ps$

$t_{pd} = 375 - 25 = 350ps$

$t_{cd} = 25 + 25 = 50ps$



Shift register.

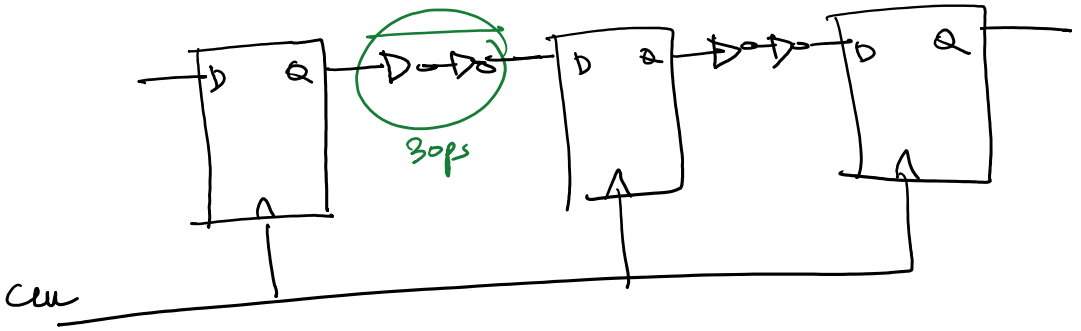
$t_{ccq} = t_{pcq} = 25ps$ $\quad t_{setup} \geq 100ps$, $t_{hold} = 50ps$, $T_{CLK} = 500ps$

$t_{pd} \leq 375ps$ ✓

$t_{cd} \geq 25ps$ ← → Will fail hold check

* No issues for setup time

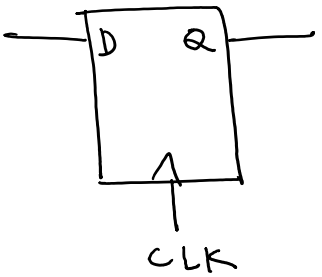
But need to fix hold time issue

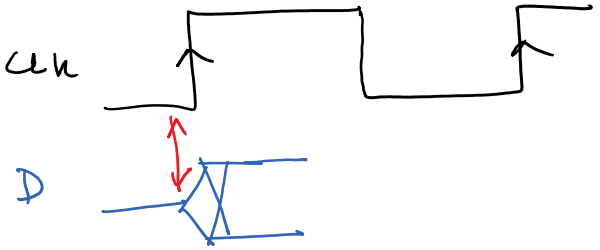


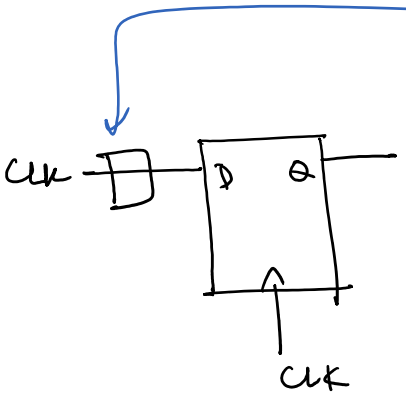
$t_{INV} = 15ps$

$t_{pd} = 30ps \leq 375ps$ ✓

$t_{cd} = 30ps \gtrsim 25ps$ ✓







⇒ Synchronizers to avoid metastability due to setup time violation

↓

Weste → Harris