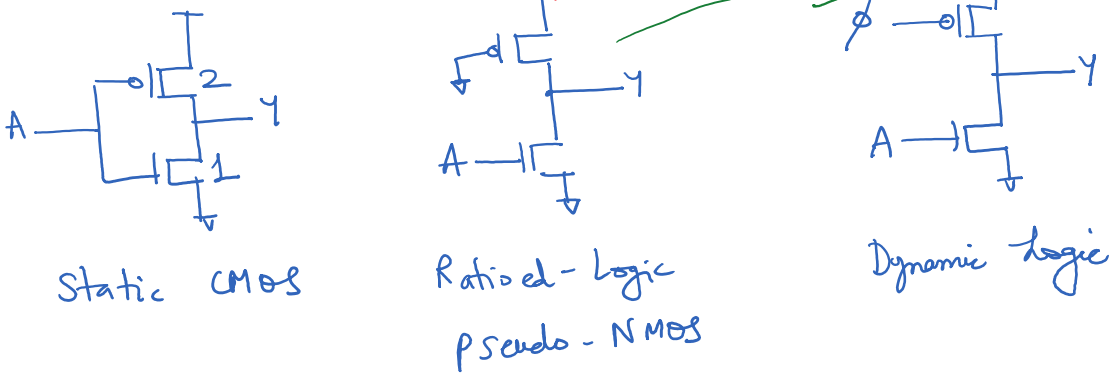
ECE 445 - Lecture 24.

Wednesday, April 24, 2019 7:59 AM

Dynamic Circuits:



Static CMOS | Ratioed-Logic (Pseudo-NMOS) | Dynamic logic

* Dynamic circuits use a clocked pull-up instead of a PMOS.
  - ↳ the pull-up is only active during the clock phase (ϕ)

Operation has two modes:

1) precharge ⇒ $\phi = 0$ ⇒ PMOS is ON and initializes the output
   $Y \Rightarrow$ "1" $\Rightarrow V_{DD}$

2) Evaluate ⇒ $\phi = 1$ ⇒ clocked PMOS turns off
   - ↳ the NMOS network evaluates the logic
   - ↳ Y remains high or may be pulled down to ground

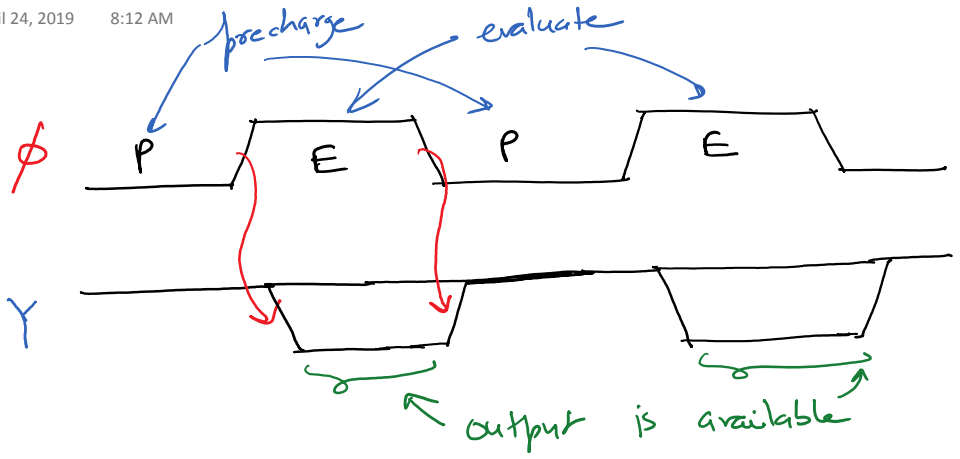
(+) fastest logic type
- ↳ lower input cap (only one PMOS precharge device)
- ↳ no contention during switching

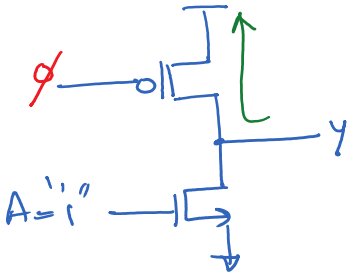
↳ zero static power dissipation

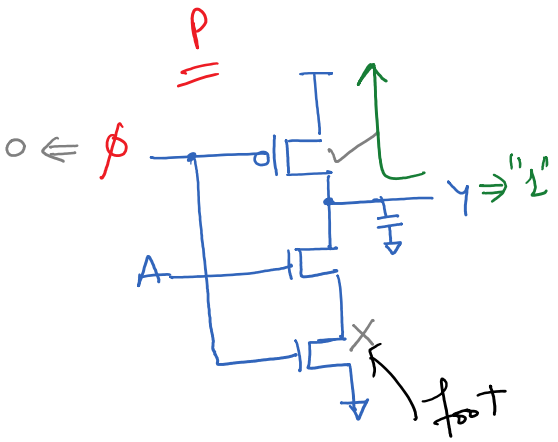
(–) ↳ require careful clocking

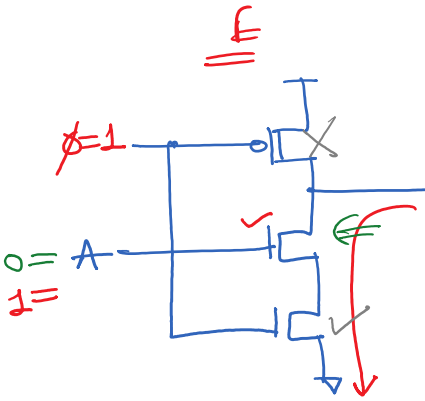
↳ can consume significant dynamic power (CV^2f)

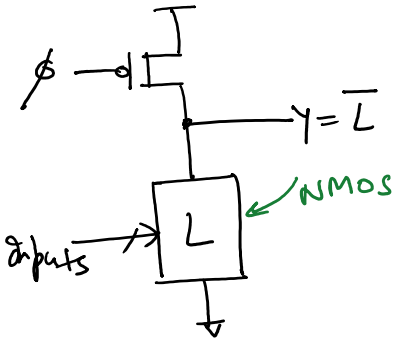
↳ sensitive to noise/coupling during evaluation

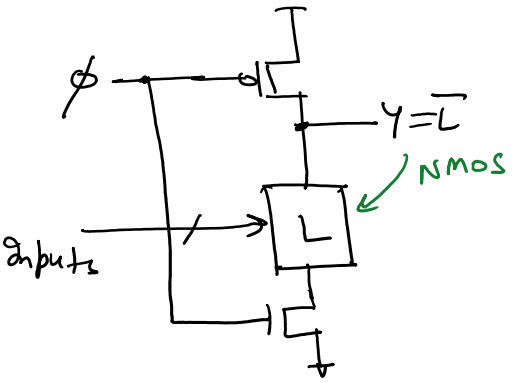

precharge
evaluate
ϕ
P
E
P
E
Y
output is available


ϕ
Y
A="1"


P
0 ⇐ ϕ
Y ⇒ "1"
A
foot


E
ϕ=1
Y = "1" ⇒ output stays at VDD
0 = A
1 =
Y = "0" ⇒ output is discharged to ground

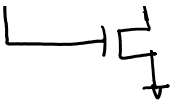

ϕ
Y = L̄
NMOS
inputs
L


ϕ
Y = L̄
NMOS
inputs
L

inputs

Unfooted Dynamic logic

Domino



~~footed~~ Dynamic logic

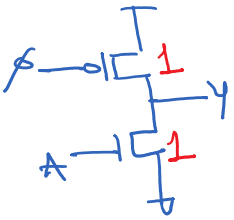
footed-Domino

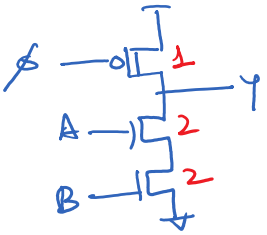
Inverter

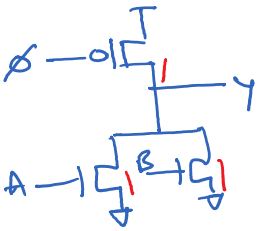
NAND2

NOR2

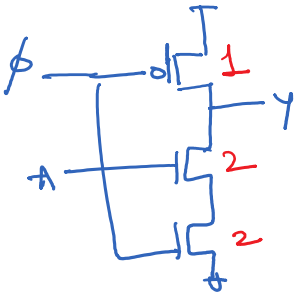
Unfooted

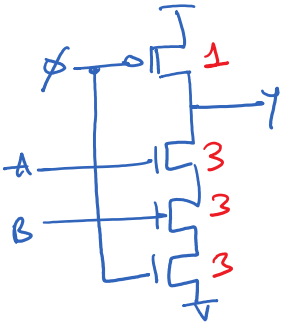


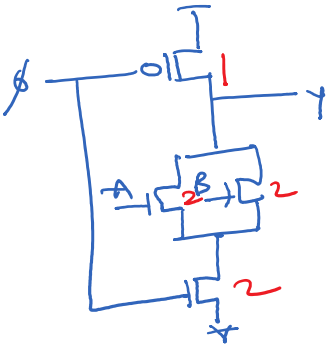




Footed







→ Pt-logic ⇒ DRAM design

(Address decoders)

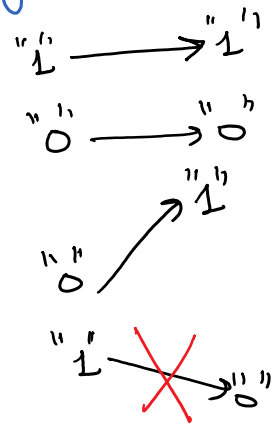
* Can be 2-3× faster than static logic
* Dynamic power consumption adds up ⇒ almost same as Static logic

* fundamental difficulty with dynamic circuits

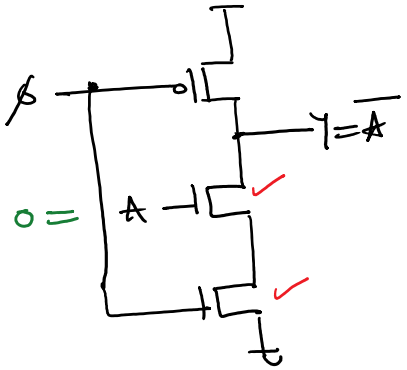
↳ monotonicity requirement

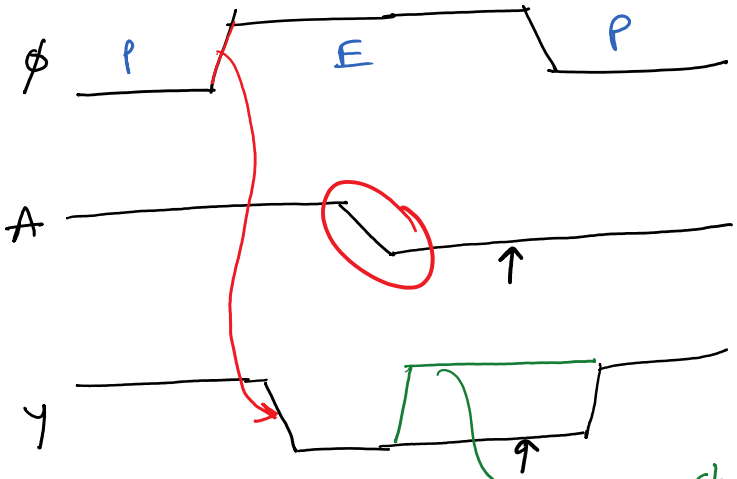
* while a dynamic gate is in evaluation, inputs must be monotonically rising.

⇒ inputs

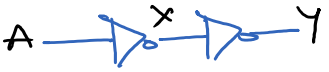


⇒ falling input transitions during evaluation are not allowed

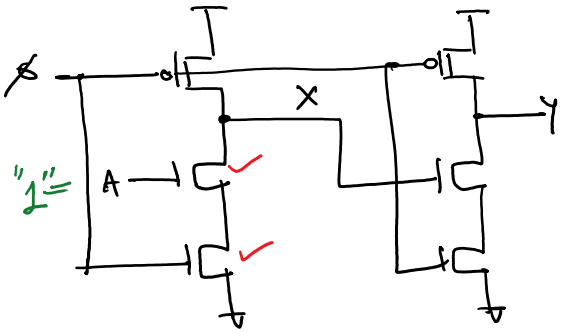


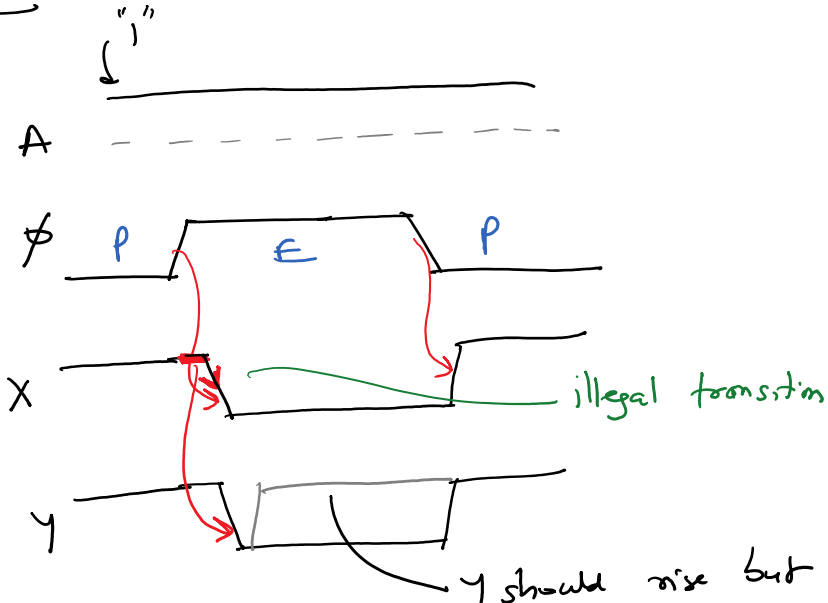


* Logic works fine if the falling input transition occurs during the precharge phase



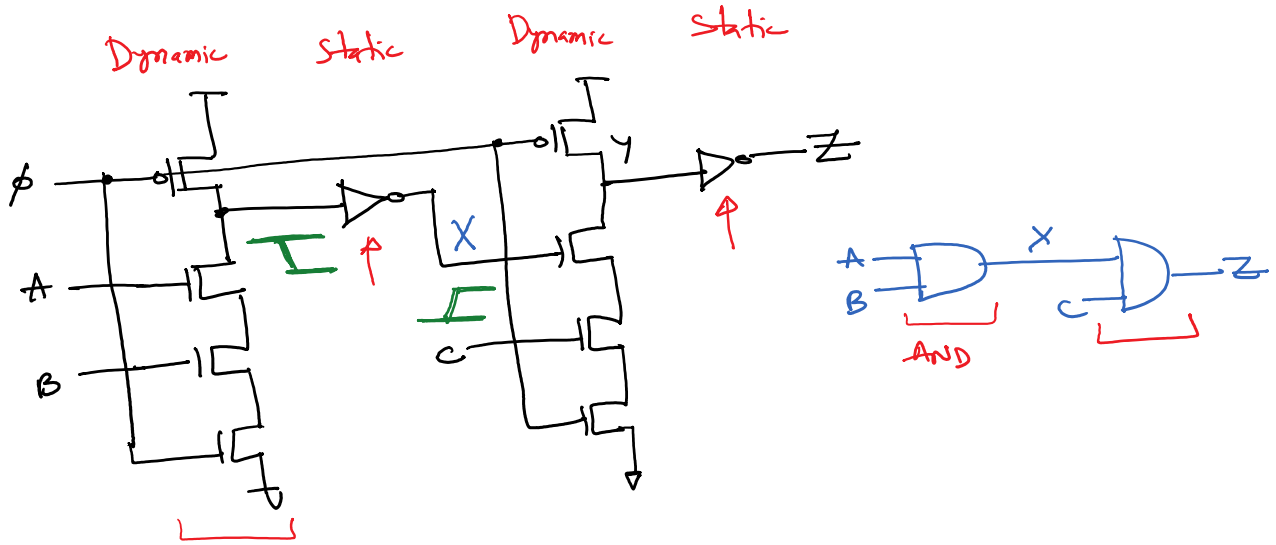
Cascade two Dynamic Gates :





⇒ Cannot cascade two dynamic gate with same clock ϕ

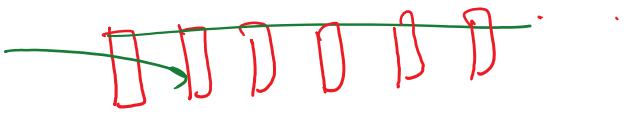
* Place a static CMOS logic (or simply a static inverter) between dynamic gates



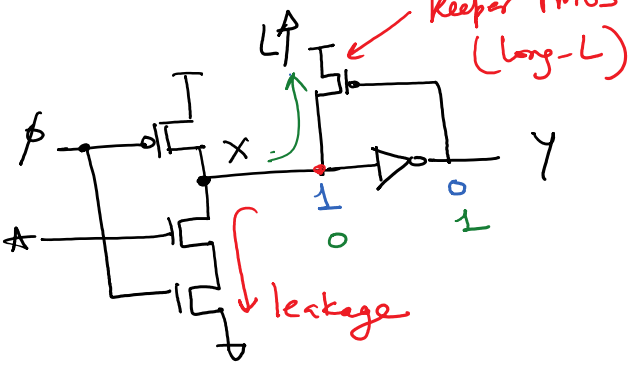
⇒ Static stage converts falling output into a monotonically rising signal suitable for the next dynamic gate.

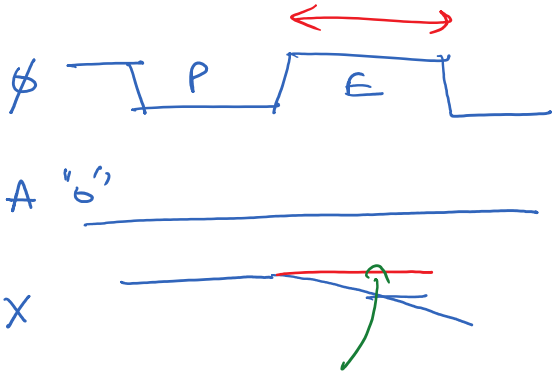
* Dynamic and static logic put together is called Domino Logic

↳ precharge resembles setting up a chain of dominoes and evaluation causes the gates to fire like dominoes tipping over, triggering the next.



Leakage problem :

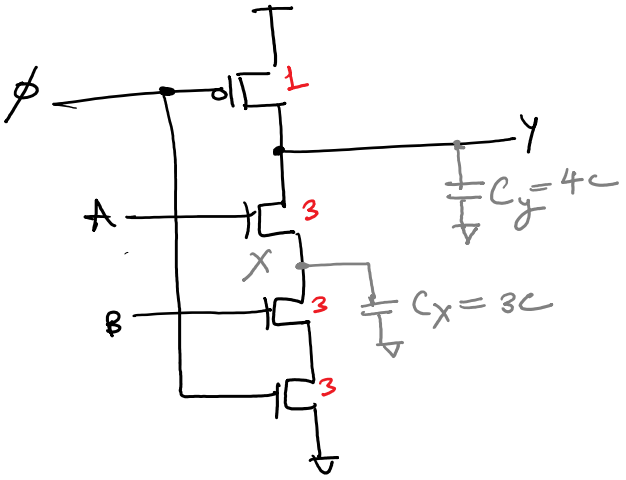


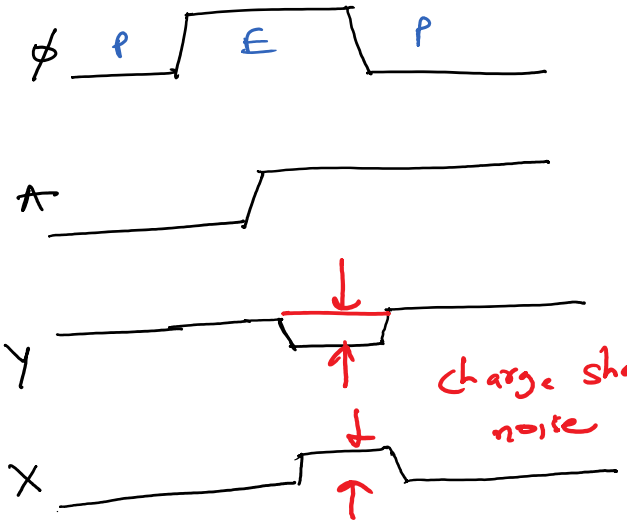


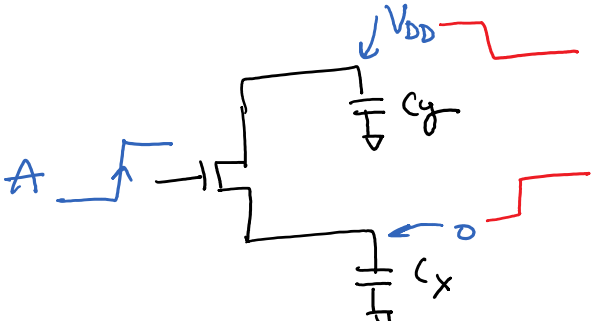
keeper PMOS holds node from discharging due to leakage

Charge - sharing problems :

B = "0"







C_X

Charge sharing between C_Y & C_X

* If charge sharing noise is large
  ↳ output may flip and cause logic errors