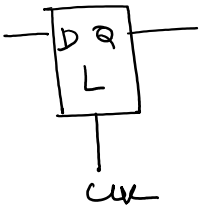
ECE 445 – Lecture 23

Monday, April 22, 2019 8:04 AM

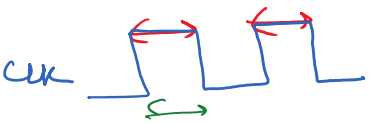
CMOS Latch

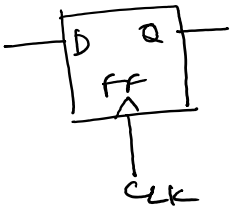
Flip-flop.



Latches

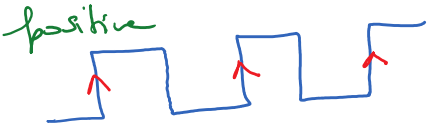
level sensitive

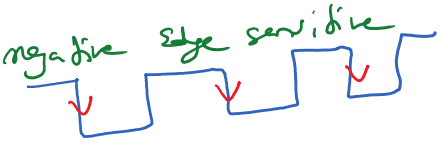




flip-flop

Edge-sensitive





Setup Time:

minimum time before which data (D) should be ready before the clock edge

Hold Time:

minimum time for which data should be held before the clock edge.

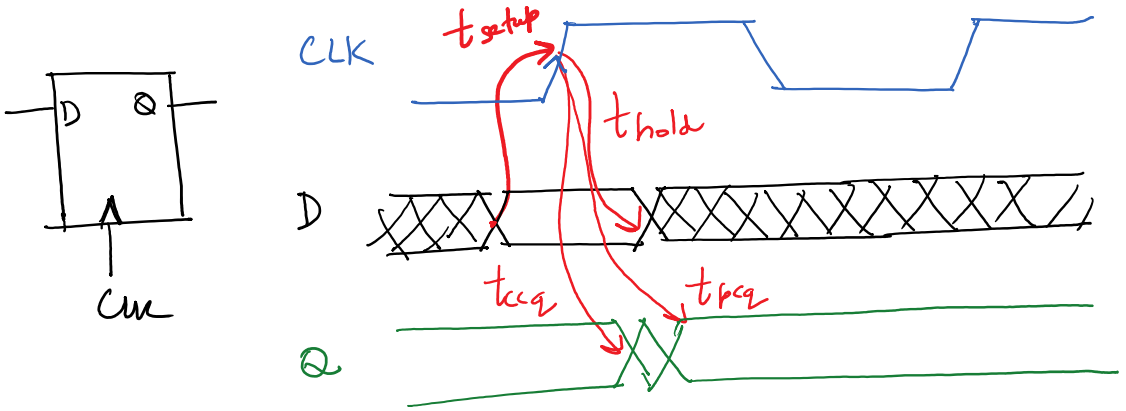
Clk-to-Q Delay:

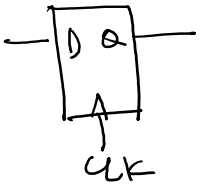
delay from the clock edge to when the output (Q) is available.

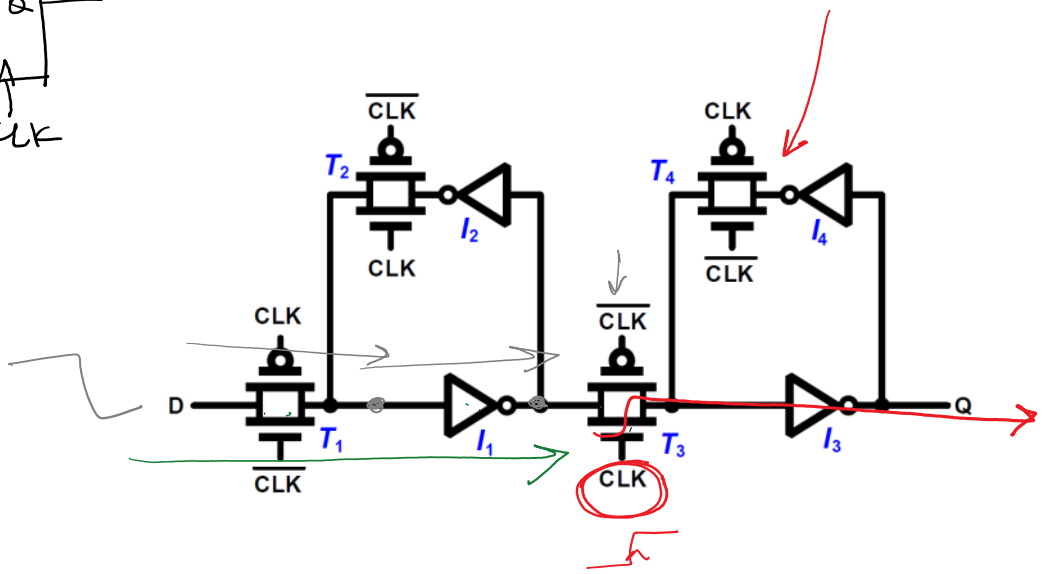
t_{pcq} ← propagation clk-q delay

t_{ccq} ← contamination clk-Q delay

positive edge-triggered FF







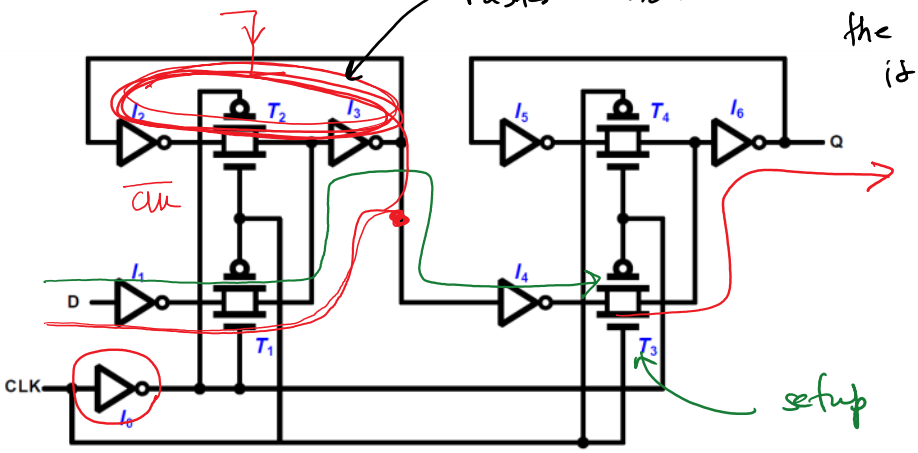
$$t_{setup} = t_{T_1} + t_{I_1}$$

$$t_{pcq} = t_{ccq} = t_{T_3} + t_{I_3}$$

t_{hold} = negative ← because even if we change the input at D after the clock-edge, the FF is able to capture the data.

$$= -(t_{T_1} + t_{I_1})$$

Master Latch should be able to hold the data so that it doesn't change if D is removed.



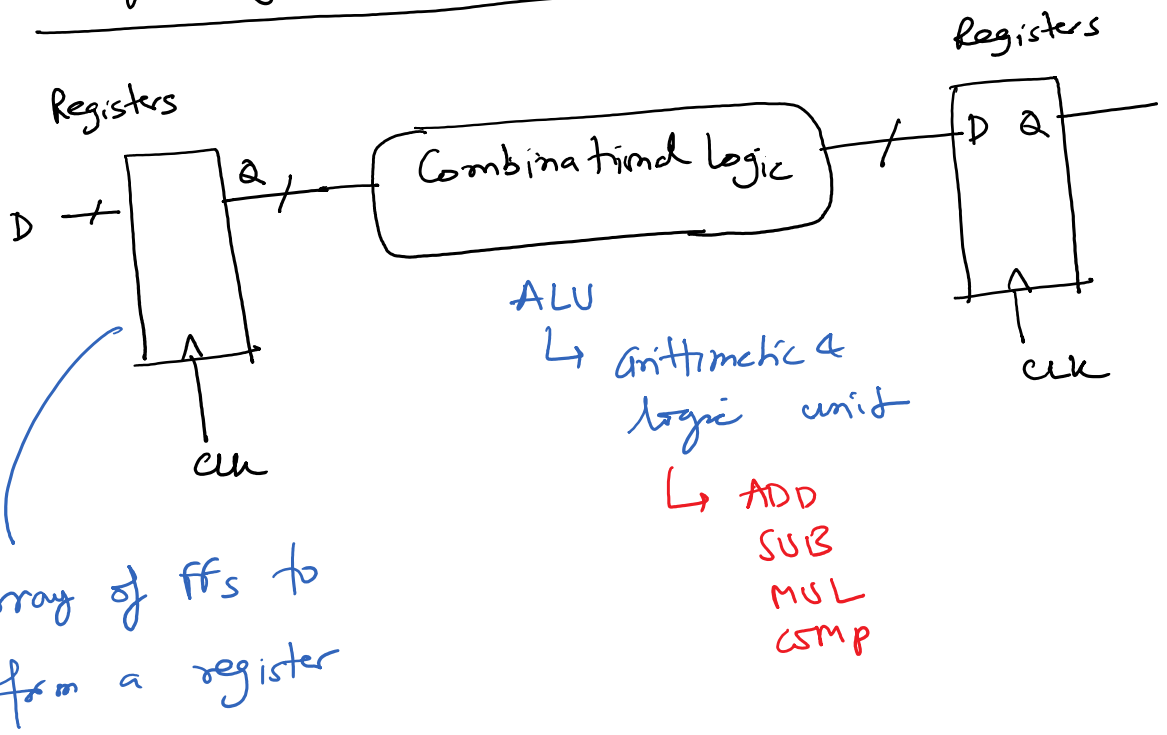
$$t_{setup} = t_{I_1} + t_{T_1} + t_{I_3} + t_{I_4}$$

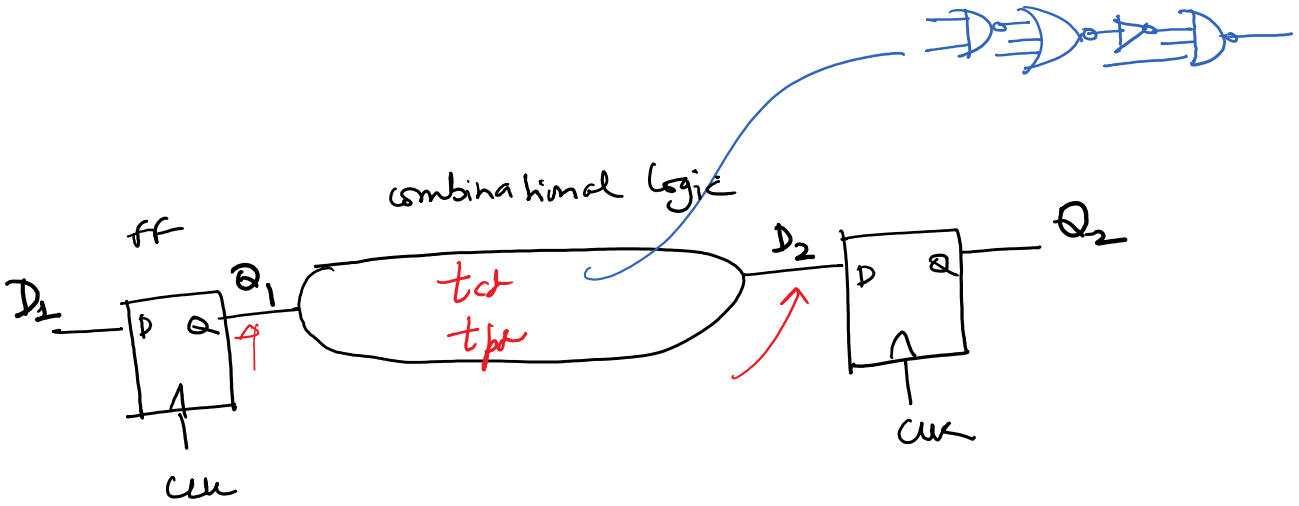
$$t_{pcq} = t_{ccq} = t_{T_3} + t_{I_6}$$

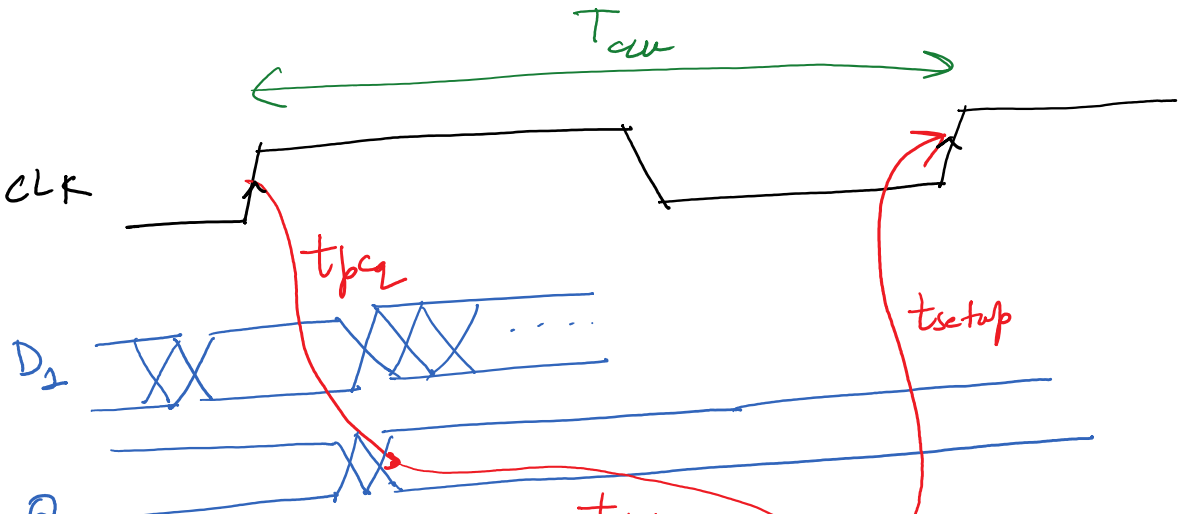
$$t_{hold} = t_{I_0} - (t_{I_1} + t_{T_1} + t_{I_3}) \leftarrow$$

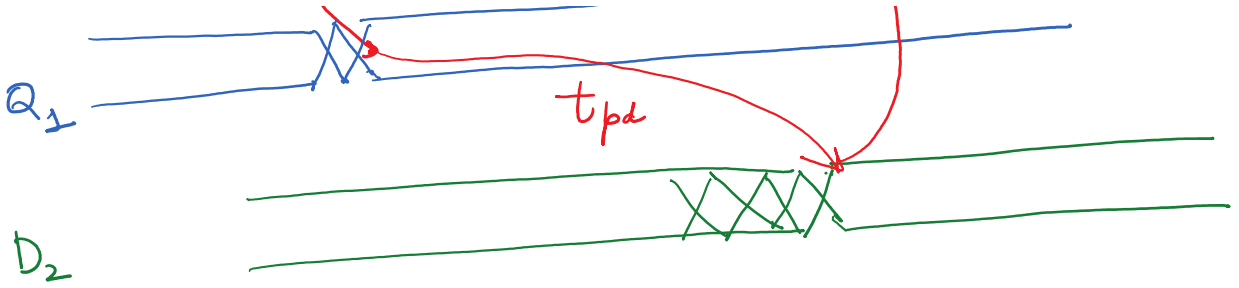
$$< 0$$

Sequencing of Static Circuits









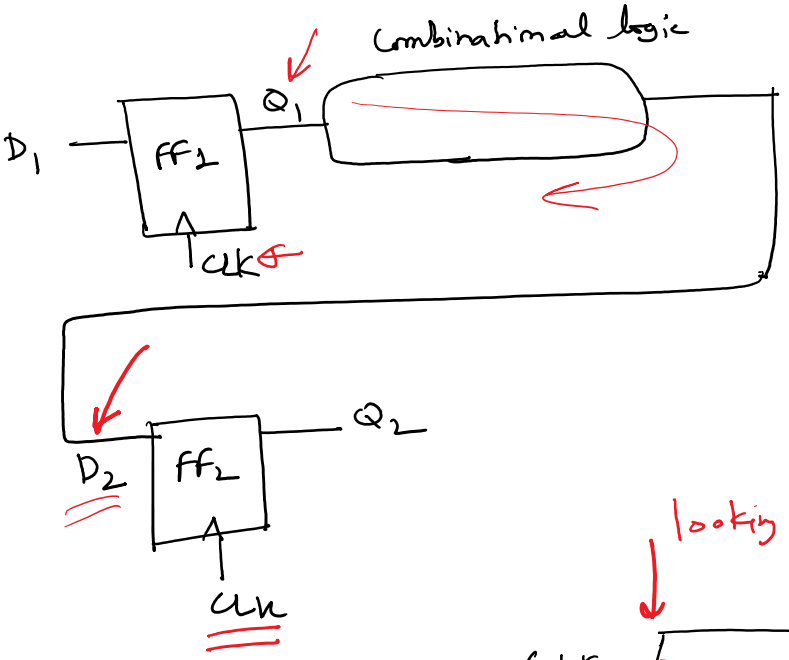
$$t_{pcq} + t_{pd} + t_{setup} \leq T_{CLK}$$

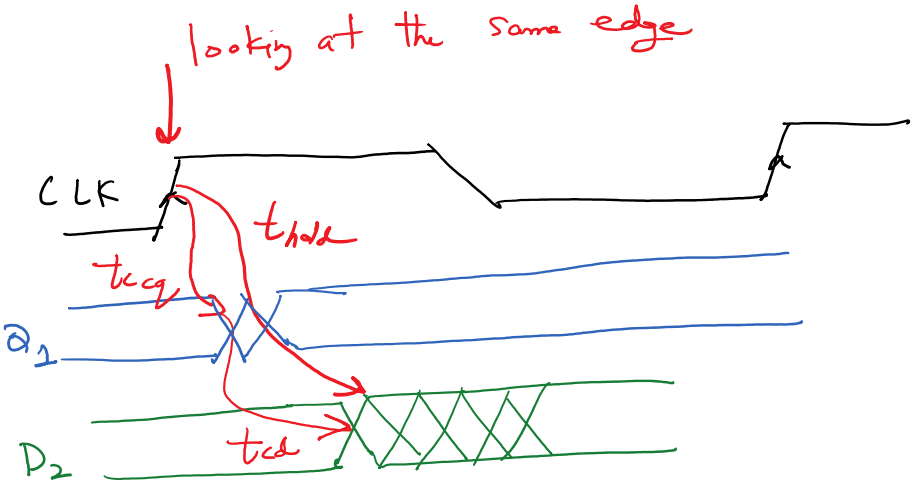
$$\Rightarrow \boxed{t_{pd} \leq T_{CLK} - (t_{pcq} + t_{setup})}$$

Max-delay

↳ setup check

* Can slow down the clock to make the circuit work.





* D_2 must be held at FF_2's input (hold time requirement)

* But in the meantime this data (D_2) could be contaminated by change in Q_1

* D_1 change could contaminate D_2 before the hold time needed for FF_2.

↳ Hold time failure at FF_2 (hold check).

$$t_{ccq} + t_{cd} \geq t_{hold}$$

$$t_{ccq} + t_{cd} \geq t_{hold}$$

$t_{ccq} + t_{cd}$ → Contamination delay due to change in D_1

t_{hold} → hold time at D_2

$$t_{cd} \geq t_{hold} - t_{ccq}$$

→ Min-delay hold-check

Min-delay: $t_{hold} - t_{ccq} \leq t_{cd}$

Max-Delay: $t_{pd} \leq T_{CLK} - (t_{pcq} + t_{setup})$

$$t_{hold} - t_{ccq} \leq t_{cd}, \quad t_{pd} \leq T_{CLK} - (t_{pcq} + t_{setup})$$

delay constraints on the combinational logic

* Can't fix hold time failures
  ↳ throw the chip away.