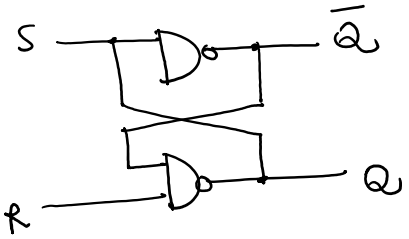
ECE 445 - Lecture 22

Wednesday, April 17, 2019 8:04 AM

Latches:

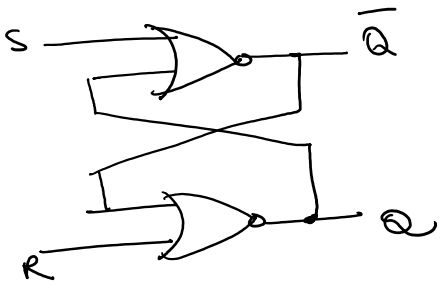
SR Latches (NAND)



Set
Reset

S	R	Q	$\bar{Q}$	
0	0	1	1	reset
0	1	0	1	set
1	0	1	0	set
1	1	Q	$\bar{Q}$	previous state

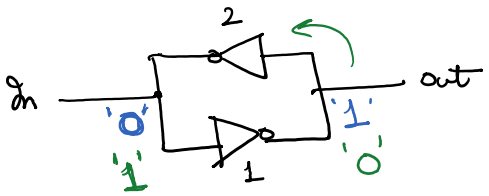
SR Latch (NOR)

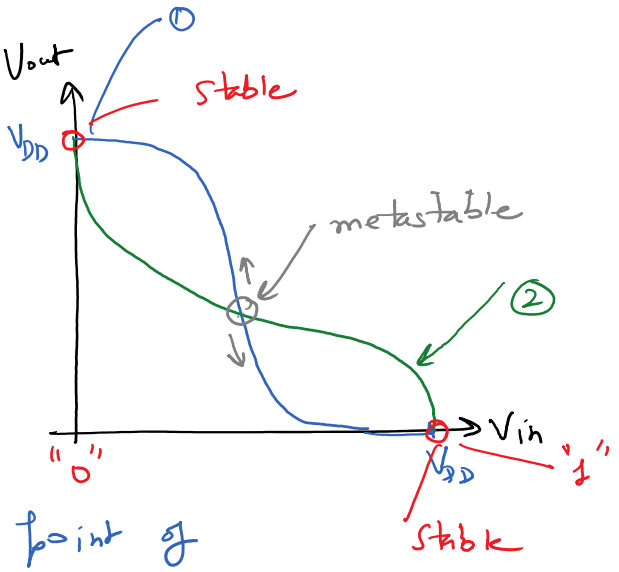


S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	← previous state
0	1	0	1	set
1	0	1	0	set
1	1	0	0	← reset

* Can design these using CMOS static logic
* Asynchronous latch (no clock input)

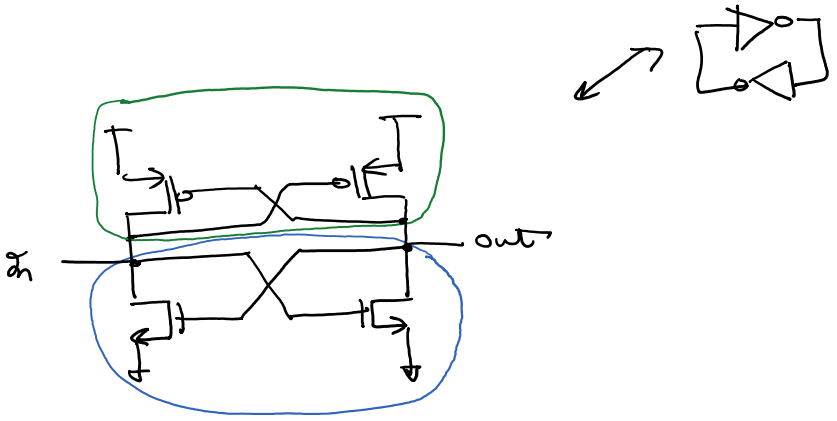
Synchronous Latch → CMOS

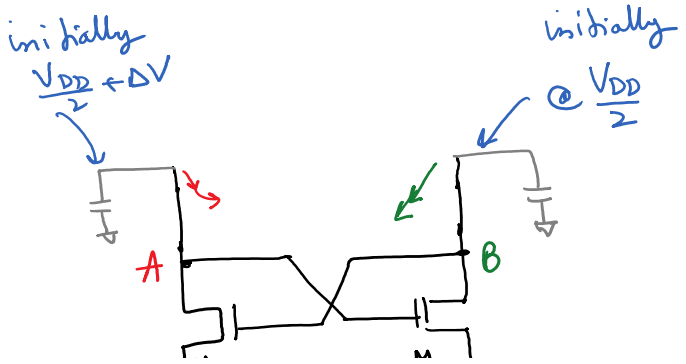


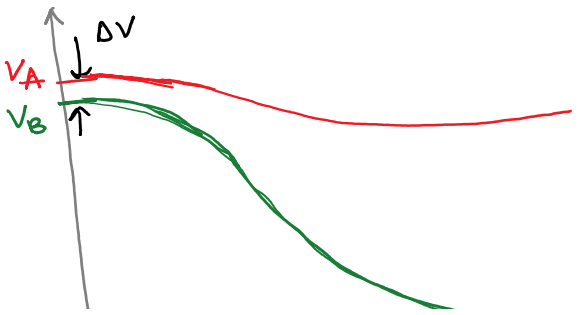


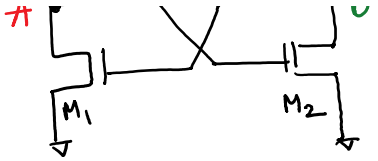
* metastable state ⇒ switching point of the inverters

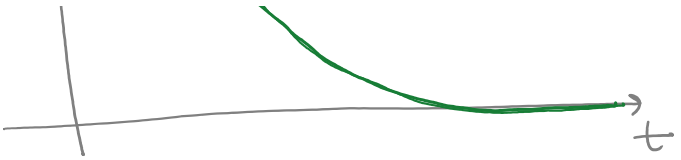
* Cross coupled inverters











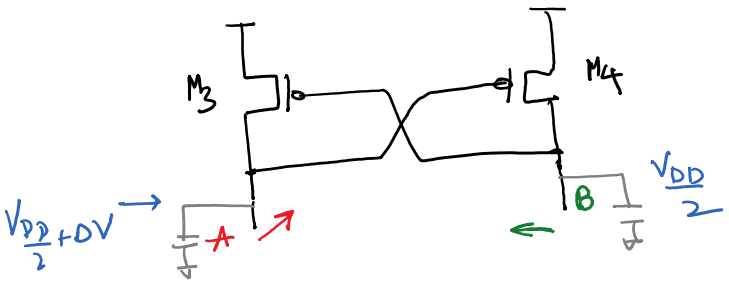
$\because V_A > V_B$

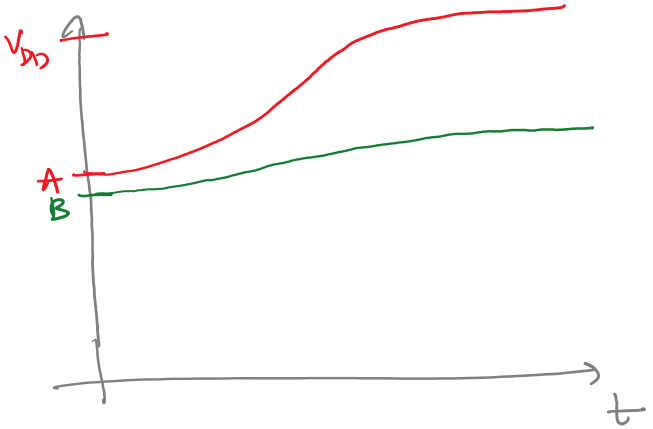
$V_{GS_2} > V_{GS_1}$

as time progresses

$V_{GS_2} >> V_{GS_1}$

* positive feedback

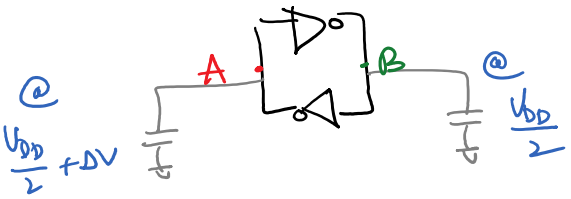


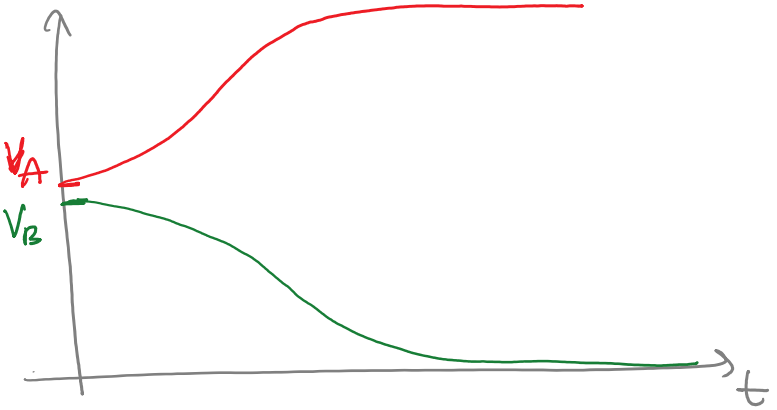


$V_{SG_3} > V_{SG_4}$

M_3 is stronger

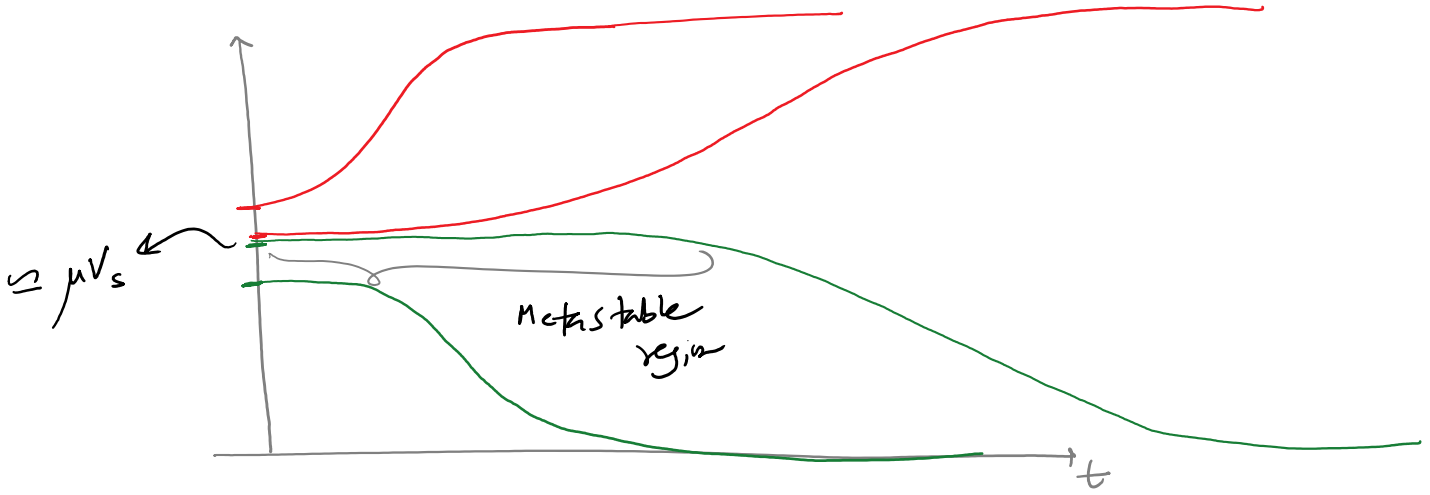
* Combining the cross coupled NMOS & PMOS together





Known as Sense amplifiers in the context of memory ICs

* Core component of analog comparators



* Regenerative Latch
  - ↳ regenerate the levels back
  - ↳ positive feedback
    - ↳ very fast circuit
  - ↳ a key component of comparators

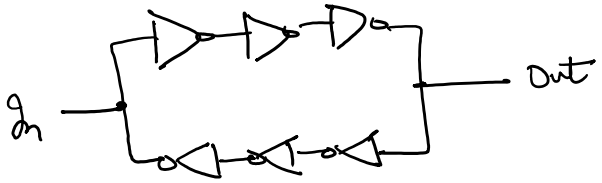
* minimum value of ΔV which can be resolved
  - ↳ resolution of the latch

Too small a value of ΔV → metastability
- ↳ takes long time of resolve

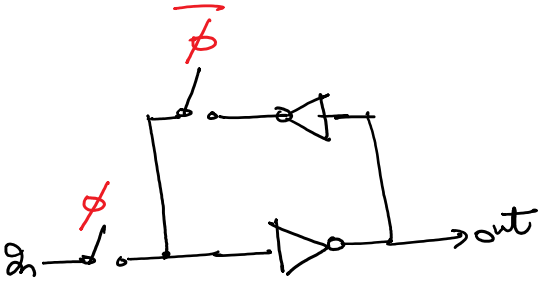
* To avoid metastability.

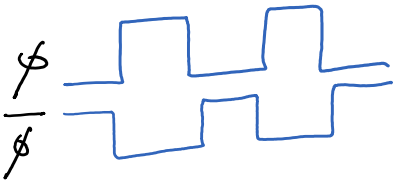
① Use clean logic levels

② increase gain of the inverters ⇒ use longer lengths
⇒ more stages



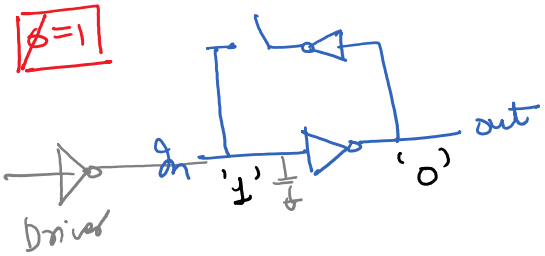
③ Add a switch





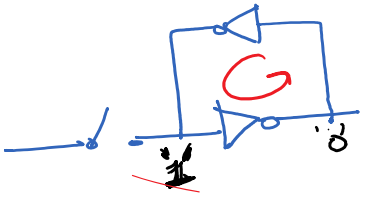
ϕ & $\bar{\phi}$ are non-overlapping clocks.

$\phi=1$

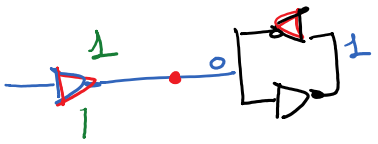


apply the input

$\phi=0$

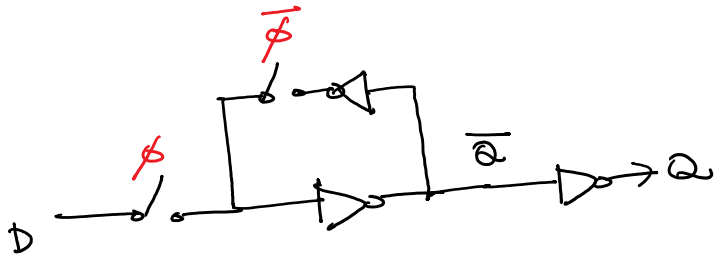


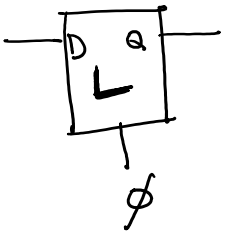
regeneration

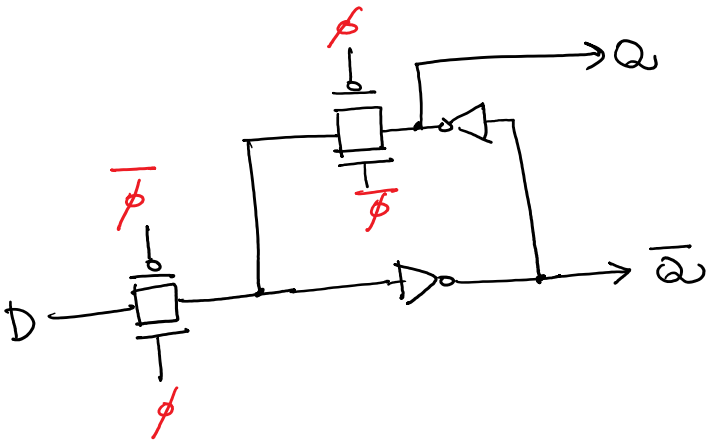


* The feedback inverter is not fighting the input driver
  ↳ avoids metastability

Level-sensitive Latch







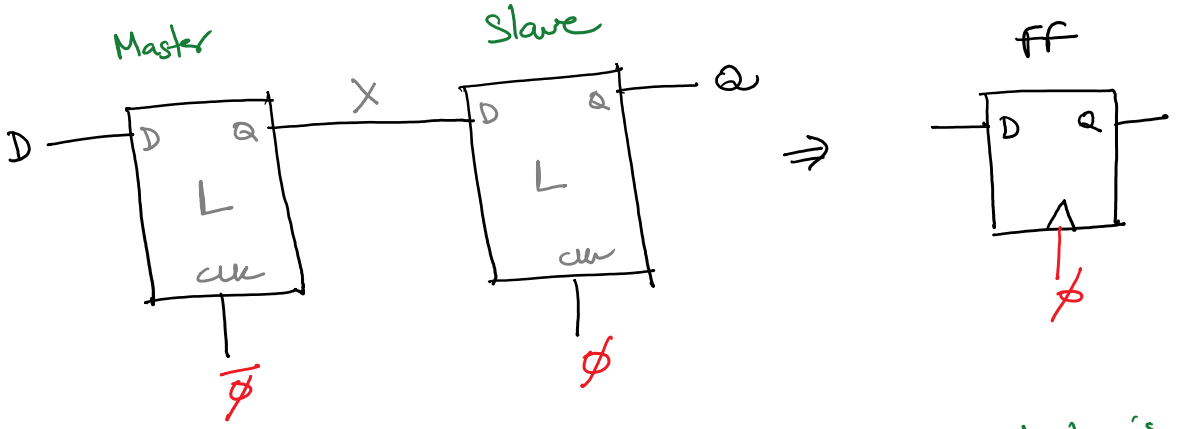
when $\phi = 1 \Rightarrow$ D is stored on $\overline{Q}$

when $\phi = 0 \Rightarrow \overline{\phi} = 1 \Rightarrow$ input D is "latched"
↳ regenerated in the cross-coupled latch

* Clock Edge-triggered digital circuits are more robust to glitches.

Edge-triggered Flip Flop

↳ registers input on rising (or falling) edges of the clock as opposed to the level of the clock.



When $\phi = 0 \Rightarrow$ first stage tracks the input (D) → Master is transparent
Slave is opaque

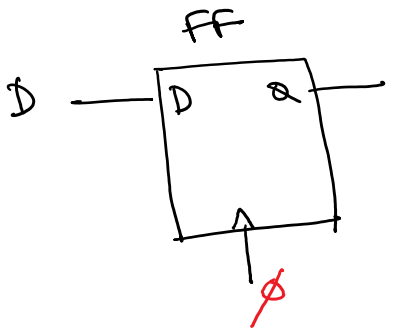
Second stage holds the previous output (Q)

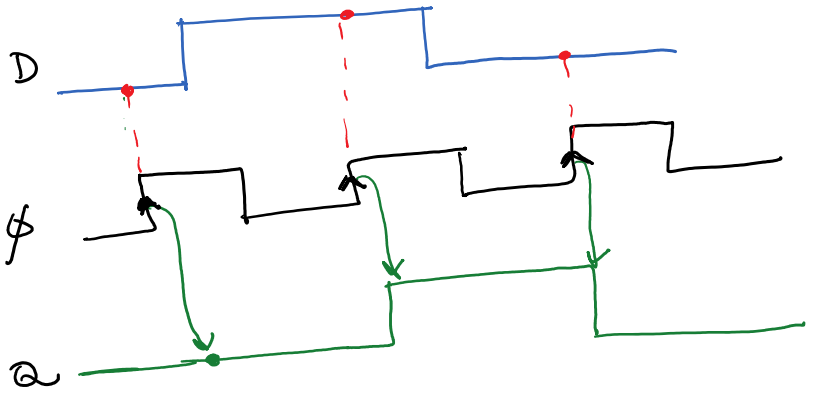
When ϕ goes from 0 to 1 $\Rightarrow$ first stage captures the input and transfers to the second stage

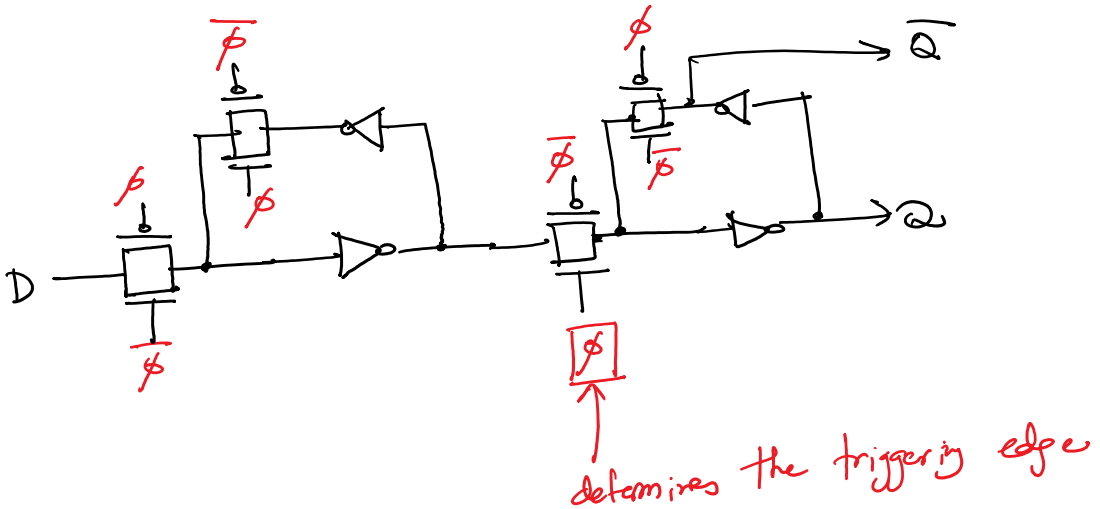
* The value of D at the instance when ϕ has a [illegible] is captured [illegible] other instances in

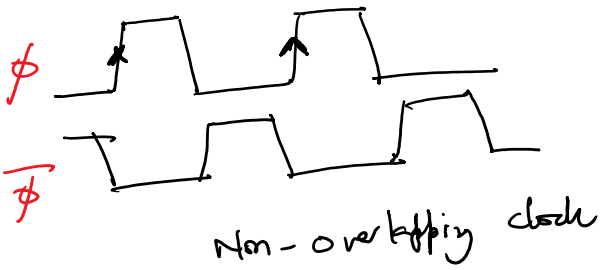
↳ value of D at the time when $\phi = 1$ is immaterial

⇒ Positive Edge-triggered flip-flop









Non-overlapping clock