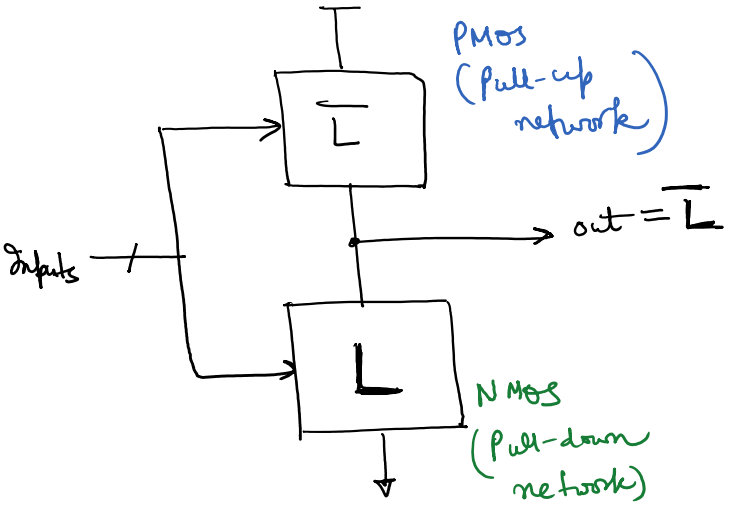
ECE 445 Lecture 21

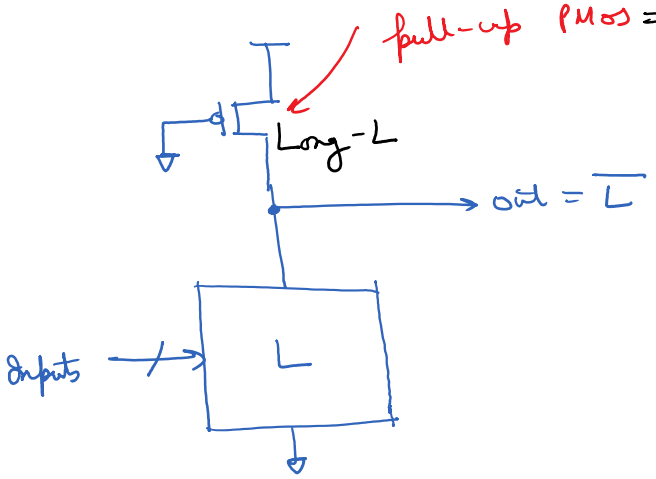
Monday, April 15, 2019 8:05 AM

Static cMos Logic:



* Input capacitance includes the NMOS & PMOS Cin
  - ↳ large input capacitance and area

Ratioed logic:

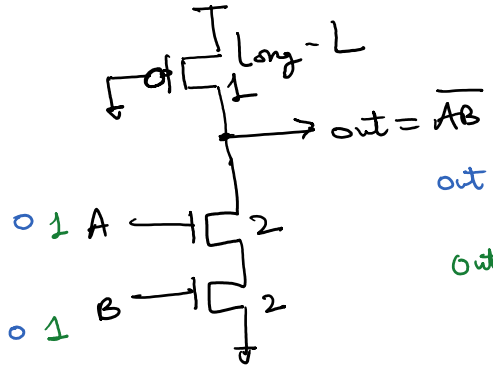


* reduces net input capacitance
* avoids large PMOS transistors

Called ratioed logic as the voltage transfer curve depends upon $\frac{R_{pull\text{-}up}}{R_{pull\text{-}down}}$

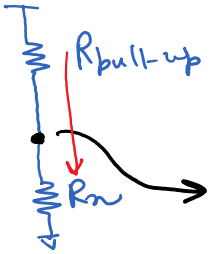
(←) Consumes static power ($V_{out,low} > 0$)

not full-swing



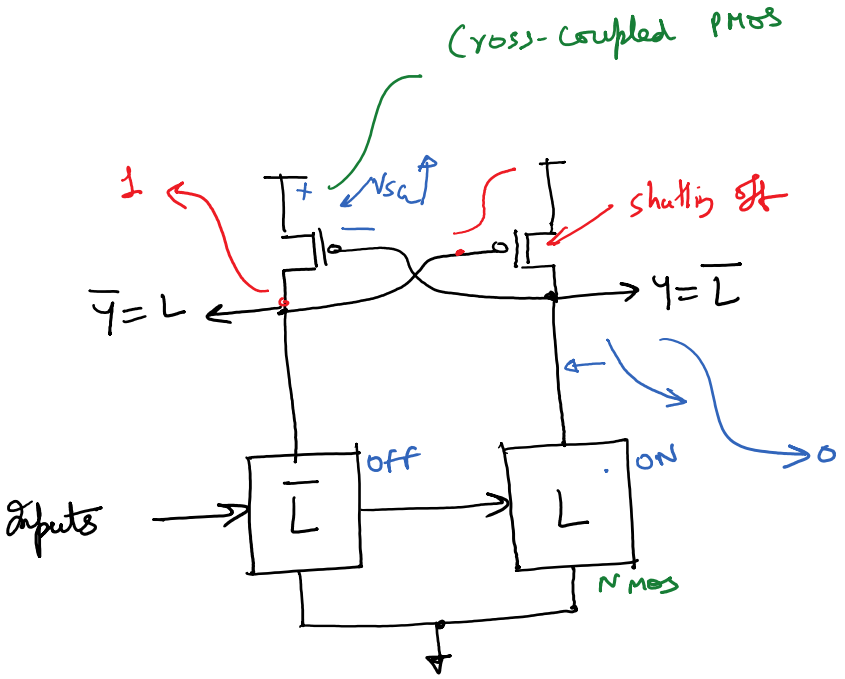
out = "1" ⇒ V_{DD}

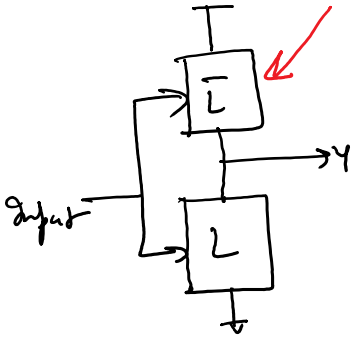
out = "0" ⇒ ≤ 50mV



Cascode Voltage Switch logic (CVSL)

↳ performance of ratioed logic without static power consumption.



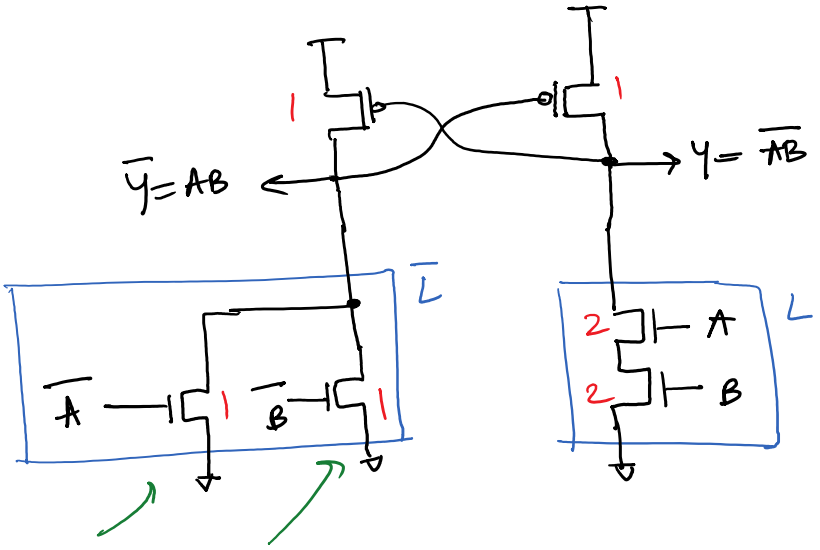


* uses true and complimentary inputs (A, Ā ...)
* Computes both true and complimentary outputs using a pair of NMOS pull-down networks
* faster than the ratioed logic but not faster than static logic

↳ what do we gain?

NAND.

$\overline{AB} = \bar{A} + \bar{B}$



XOR / XNOR Gate

$$Y = \overline{A \oplus B} = \bar{L}$$

$$\Rightarrow \quad L = \bar{A}B + A\bar{B} \leftarrow L$$

$$\bar{L} = AB + \bar{A}\bar{B}$$

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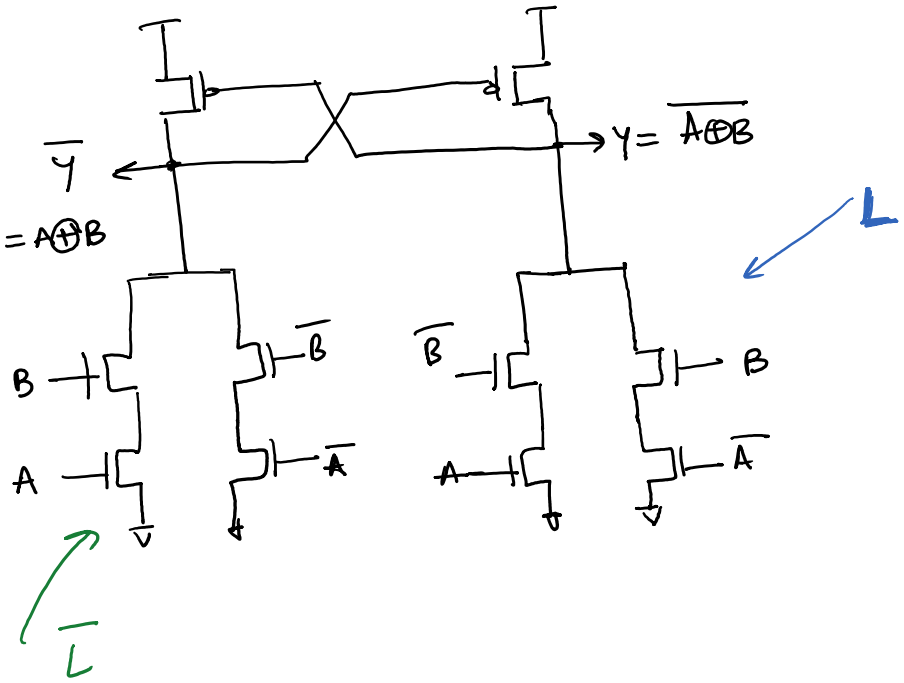
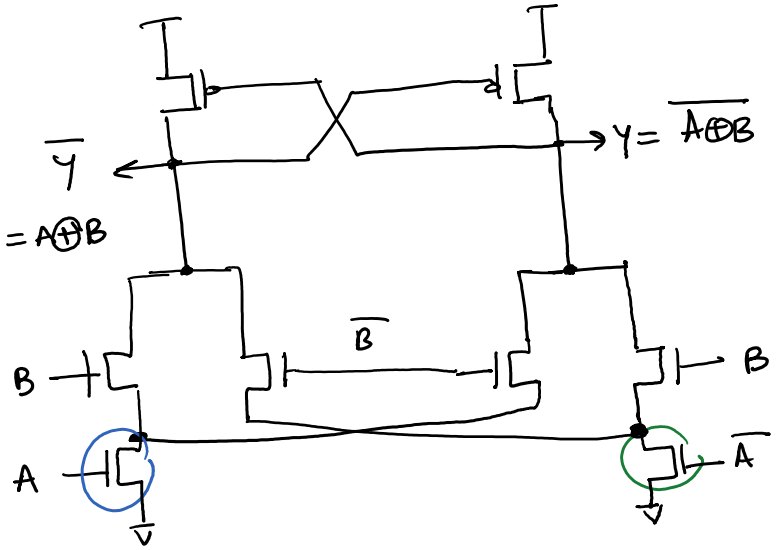


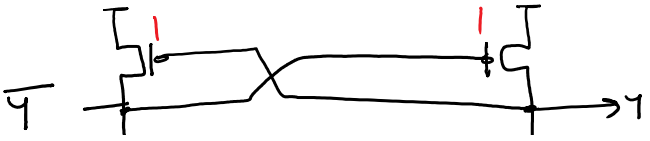
2-input XOR

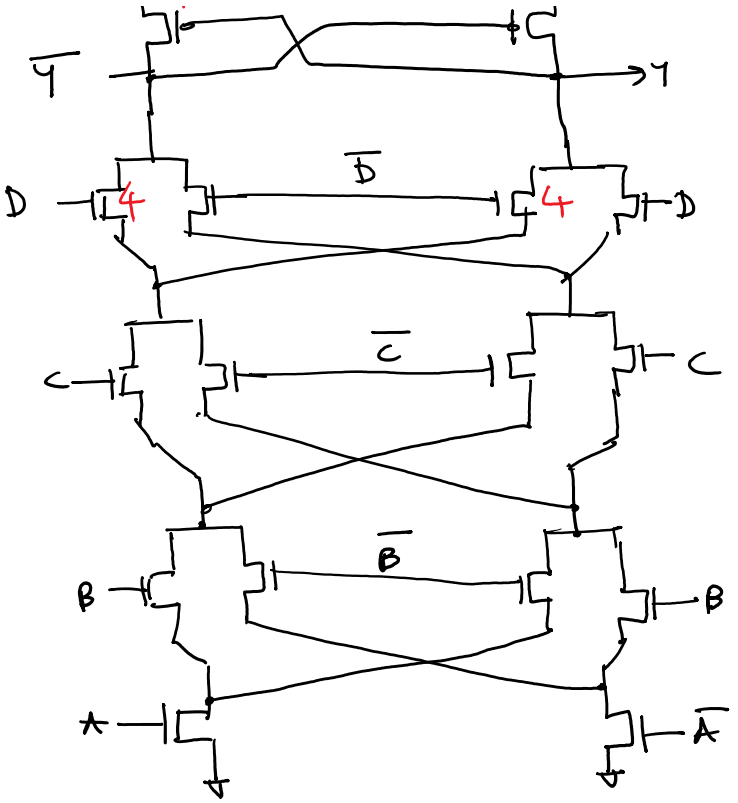


Eliminated duplication of $A \& \overline{A}$

* CVSL realizes compact XOR/XNOR logic

4-input XOR gate

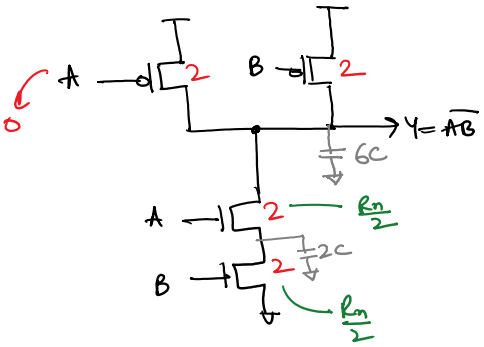




$$Y = \overline{A \oplus B \oplus C \oplus D}$$

Contamination & propagation Delays:

$t_{pHL}, t_{pLH} \leftarrow t_{pd}$



$R_p = R_n = R$

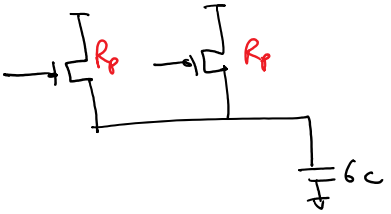
AB ⇒ 01 → 11

delay ⇒ $\left(\frac{R_n}{2} + \frac{R_n}{2}\right) 6C = 6R_nC = 6RC$

AB ⇒ 11 → 01

delay ⇒ $R_p \cdot 6C = 6R_pC = 6RC$

AB ⇒ 11 → 00 both PMOS pull-up.



delay = $\frac{R_p}{2} \cdot 6C = 3RC$

→ Not all input combinations lead to the same delay.

→ Min. Delay (t_{cd}) = minimum time from input ... crossing 50%.

Contamination delay -) the output
crossing 50%. to

propagation delay (t_{pd}) = maximum time from input crossing
50% to the output crossing 50%.