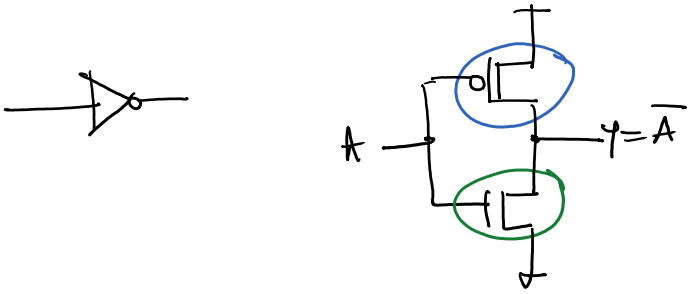
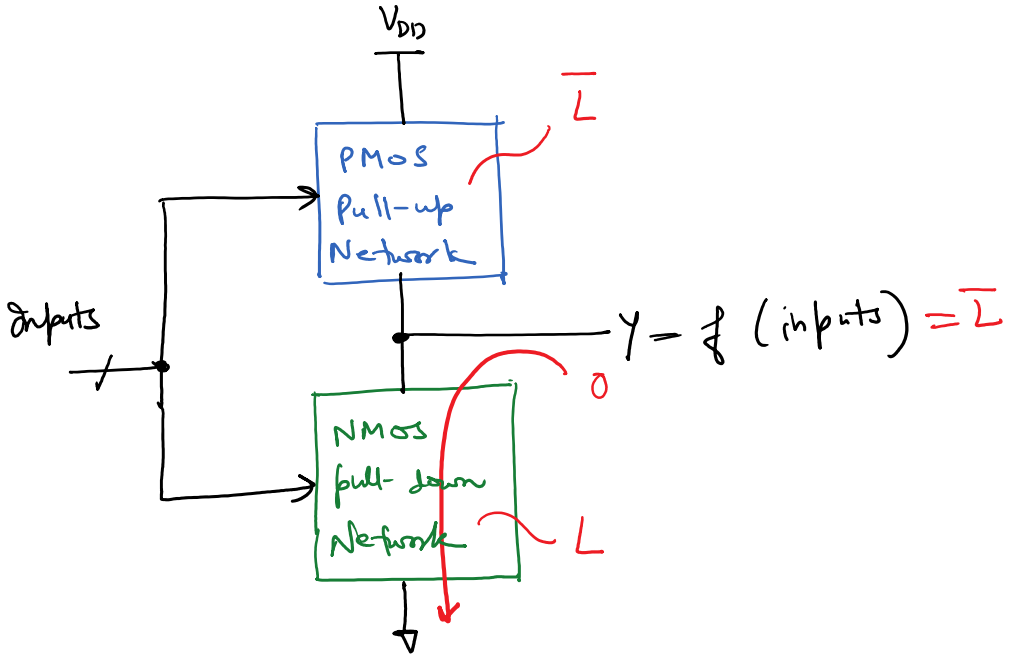
ECE 445 - Lecture 20

Wednesday, April 10, 2019 8:06 AM

Logic

- Combinational: gates, MUXES
- Sequential logic: Latch, ffs → State Machine





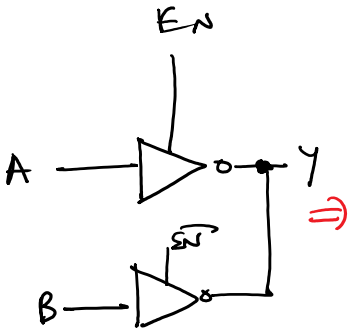
* PMOS and NMOS networks are complimentary to each other.
  - ↳ exclusive
  - ↳ both are on → large current from VDD to ground. ✗

↳ both are on

↳ large current from V_{DD} to ground. ✗

↳ both of off at the same time

↳ output is Hi-Z (high impedance) or floating. ←

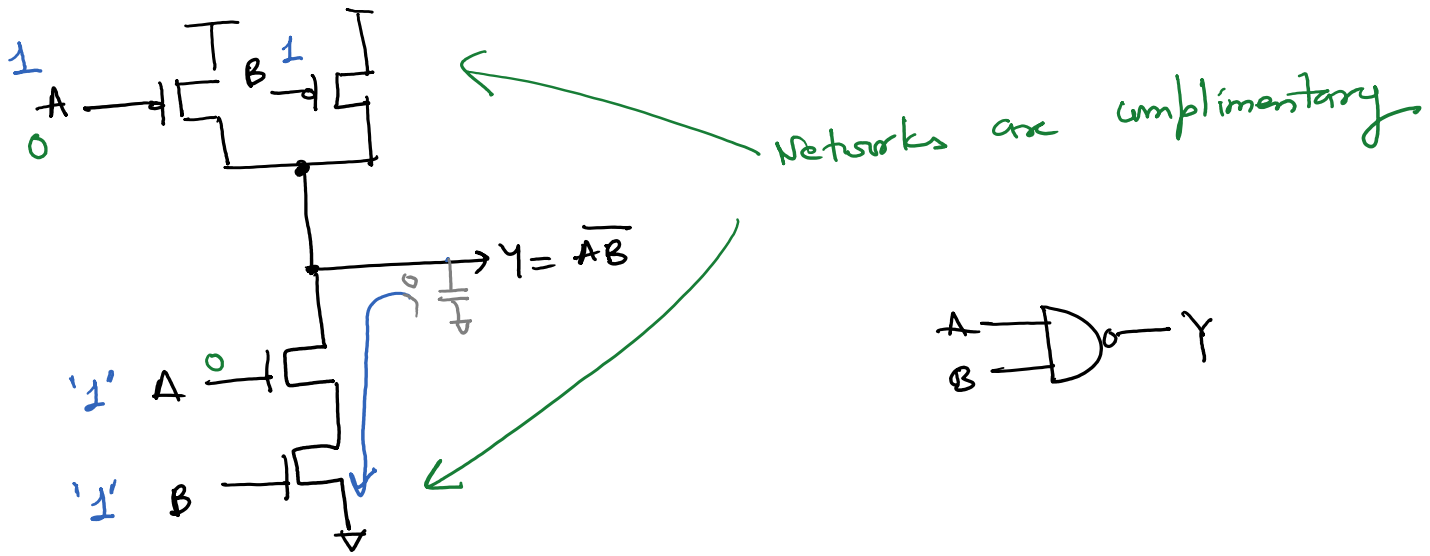


⇒ Buses

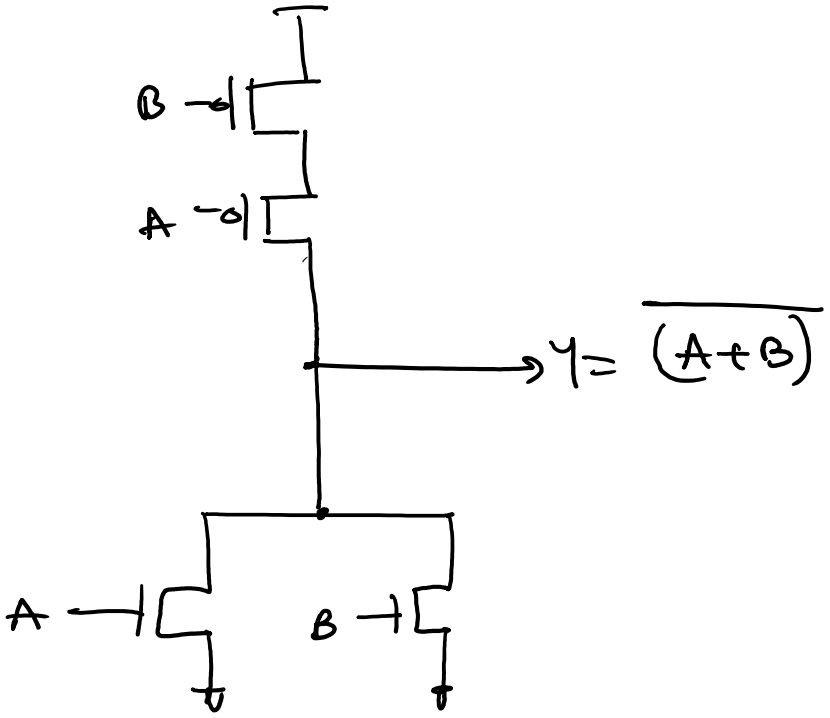
* CMOS Static Logic is inverting by nature.

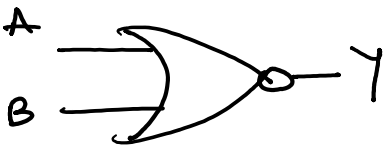
NAND-2

$Y = \overline{AB}$



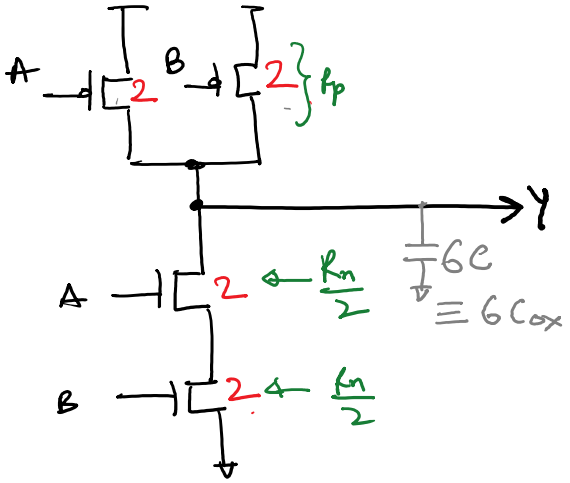
NOR-2



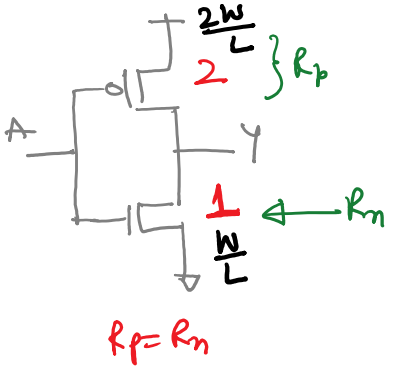


Short-channel CMOS (Sign in the CMOS book)

NAND2

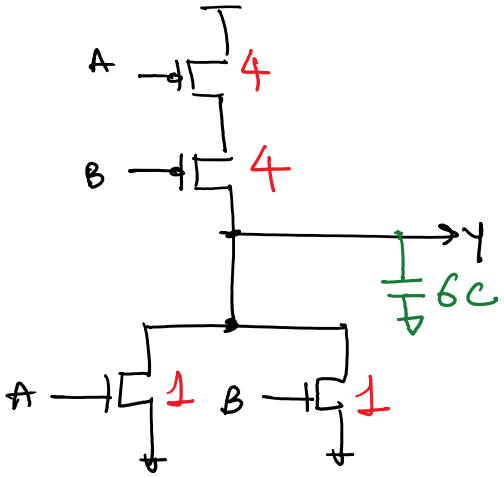


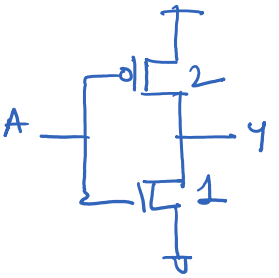
$R_n = R_n' \frac{L}{W}$



$R_p = R_n$

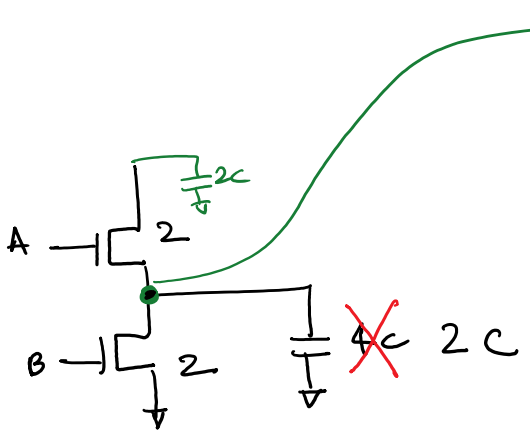
NOR2

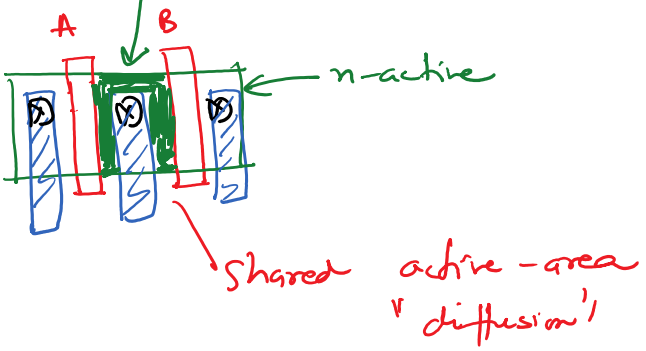




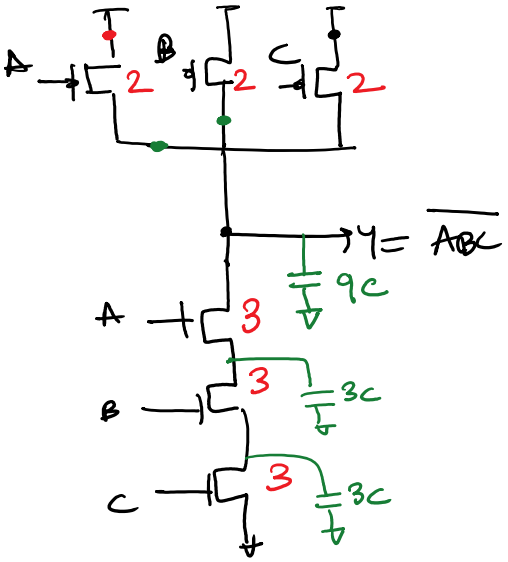
+ Preferable to have NMOS in series than PMOS
  ↳ NAND-based logic is preferable over NOR.

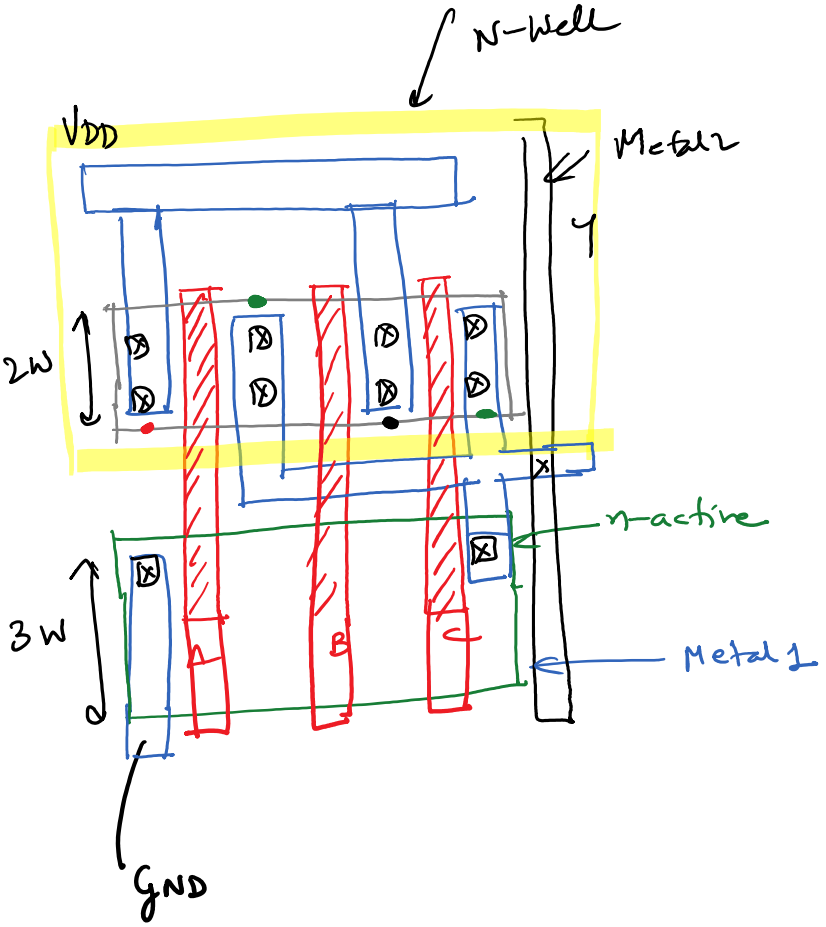
Shared diffusion



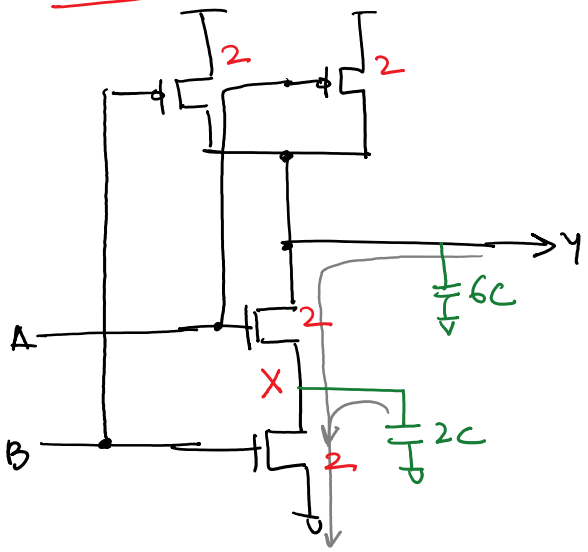


NAND 3


A
B
C
2
2
2
Y = $\overline{ABC}$
9c
A
3
B
3
3c
C
3
3c

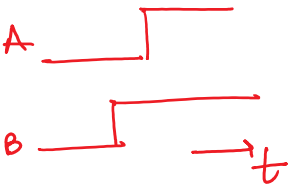

N-Well
VDD
Metal2
Y
2W
n-active
3W
A
B
C
Metal 1
GND

Input Order



Calculate t_{pHL} (Y falling edge)

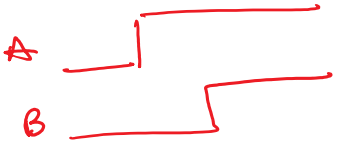
* when A arrives latest

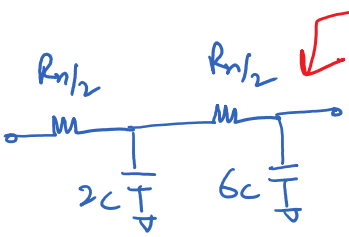


node-X has been discharged earlier

$t_{pHL} = 0.7 R_n 6C = 0.7 \times 2\tau$

* when B arrives latest





both output capacitance as well as the cap at node-X need to be discharged

extra delay

$$t_{pHL} = 0.7\left[R_n \times 6C + \frac{R_n}{2} \times 2C\right]$$

$$= 0.7 \times 2.33\tau$$

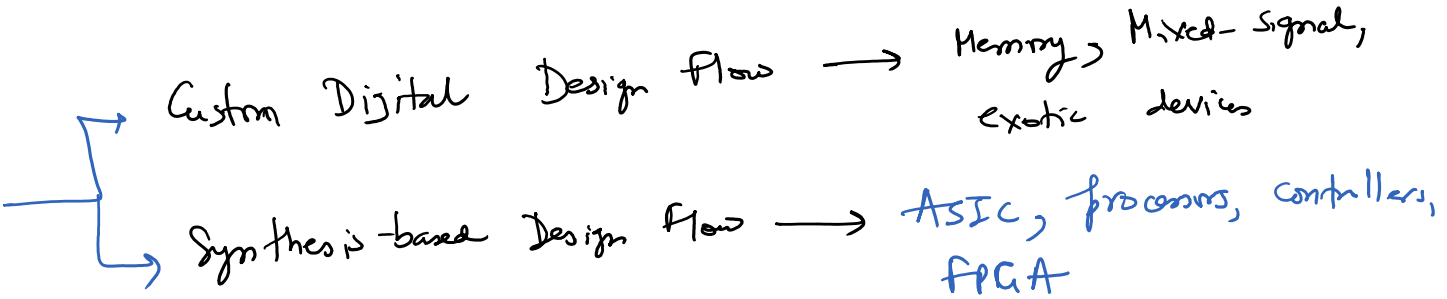
Define Rule of Thumb:

Inner input is closest to the output (i.e. A)

Outer input is closest to the supply rails (i.e B)

1. If input arrival time is known, ... the inner

"Connect latest inputs to "
terminal."

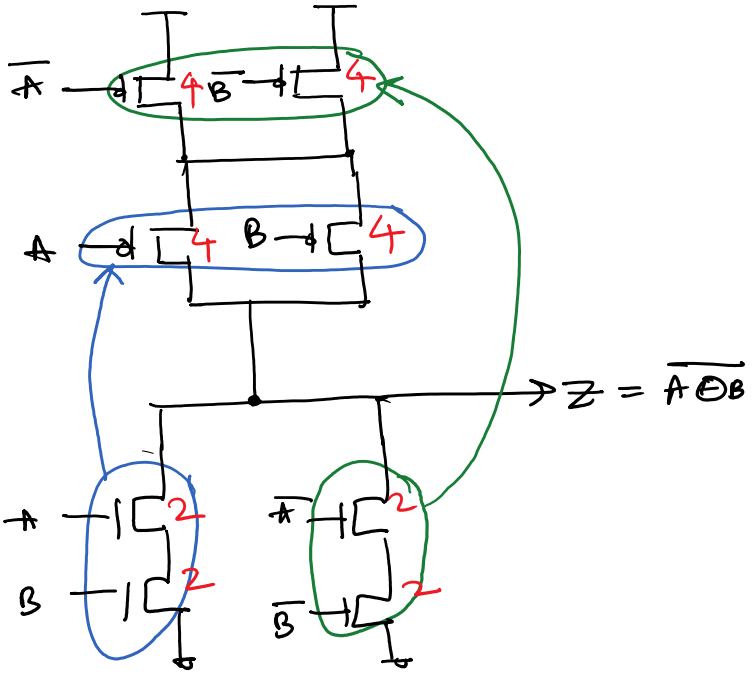


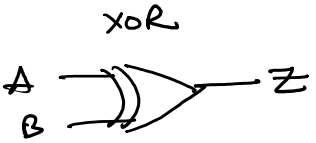
XOR Gate :

$Z = A \oplus B = \overline{(A \oplus B)} = \overline{(AB + \bar{A}\bar{B})}$

XOR: $A \oplus B = A\bar{B} + \bar{A}B$

XNOR: $\overline{A \oplus B} = AB + \bar{A}\bar{B}$

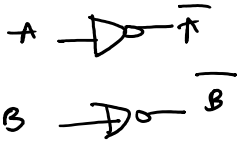




* Implement.

$Z = \overline{A \oplus B}$

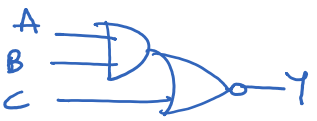
XNOR gate

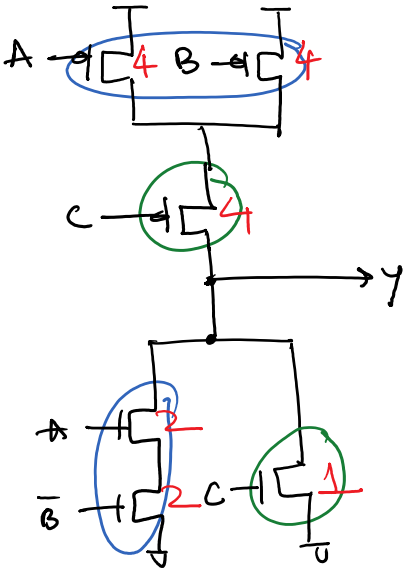


And or invert

AOI21 ⇒

$Y = \overline{AB+C}$





* PMOS A & B closer to the V_{DD} rail to minimize parasitic capacitance that needs to be charged

AOI22 ⇒ $Y = \overline{AB+CD}$