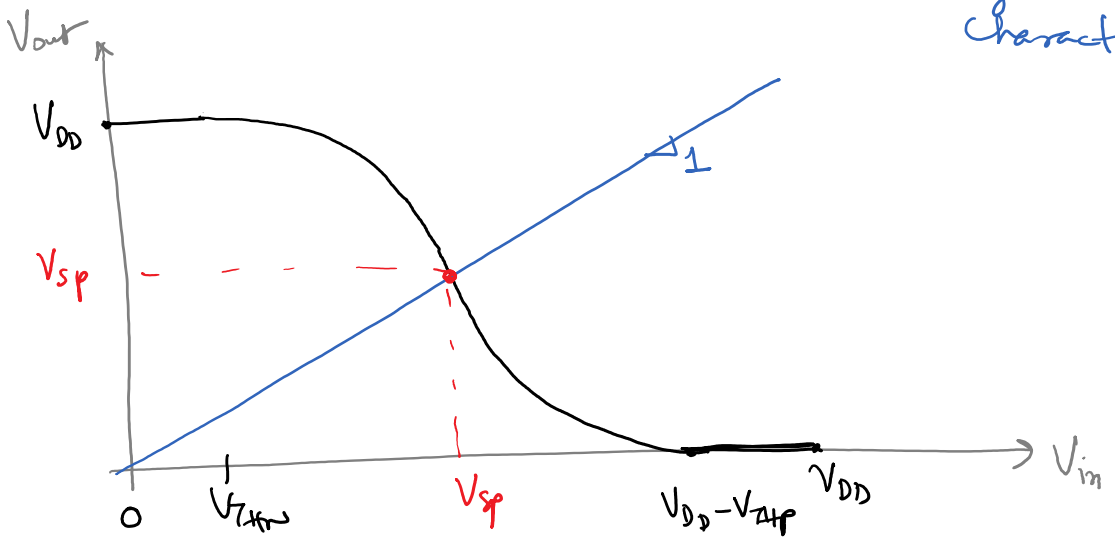
ECE 445 – Lecture 17

Monday, March 25, 2019 8:05 AM

Voltage Transfer Characteristics



$$V_{sp} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THn} + (V_{DD} - V_{THp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Beta ratio: $\frac{\beta_n}{\beta_p}$

$\frac{\beta_n}{\beta_p} = 1 \Rightarrow V_{sp} = \frac{V_{DD}}{2}$

Assume $L = L_{min}$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \cdot W_n}{k'_p \cdot W_p} = 1$$

Long-channel

$$\Rightarrow \frac{W_p}{W_n} = \frac{k'_n}{k'_p} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{\mu_n}{\mu_p}$$

for $\beta = 1 \Rightarrow \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = 3$

Assume Length

For $\beta = 1 \Rightarrow$ $\frac{}{W_n}$ μ_p

$\Rightarrow \boxed{W_p = 3 W_n}$ for same Length

* In short-channel cMOS

$$\frac{W_p}{W_n} \simeq \frac{v_{satn}}{v_{satp}} \simeq 2$$ ← find this ratio by technology characterization

* $\beta_n = \beta_p$

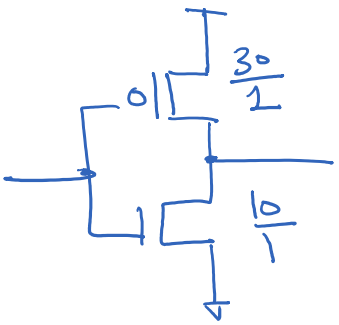
$\Rightarrow R_n = R_p$

$R_p' \left(\frac{L}{W}\right)_p$

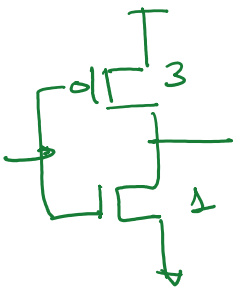
$R_n \left(\frac{L}{W}\right)_n$

Drive strength $\propto R_n, R_p$

Schematic conventions

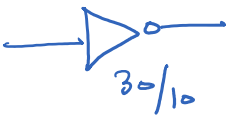


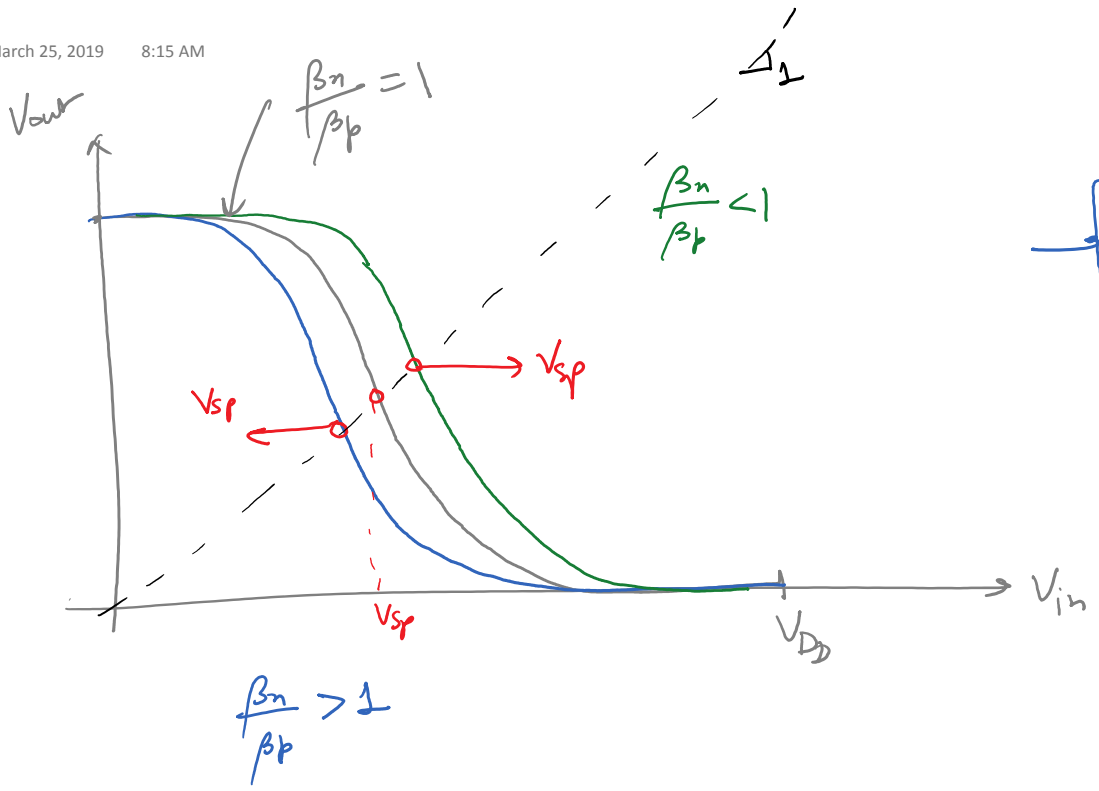
$\Rightarrow$



relative sizing

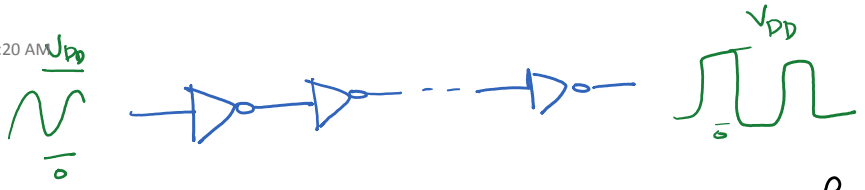
3/1





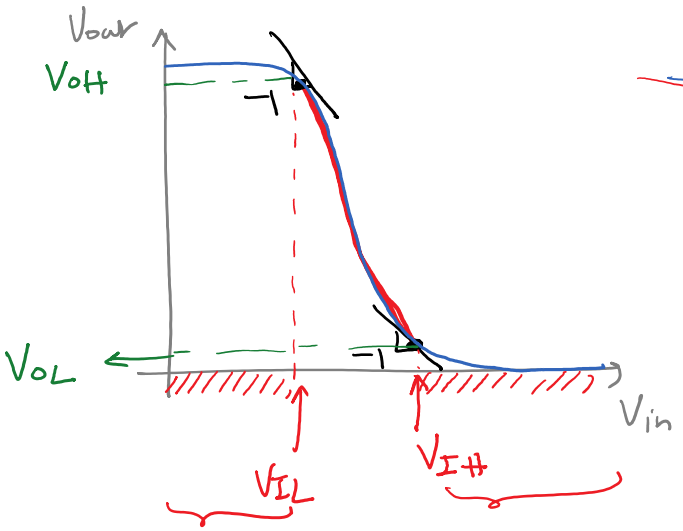
$\beta_n > \beta_p \Rightarrow$ NMOS is stronger $\Rightarrow$ pulls down VTC more

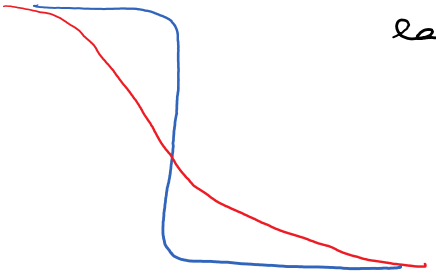
$\beta_p > \beta_n \Rightarrow$ PMOS " " $\Rightarrow$ pulls up the VTC more



Regenerative property

⇒ need gain from each stage





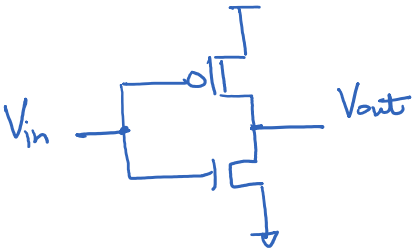
Noise Margin ⇒ $NM_L = V_{IL} - V_{OL}$

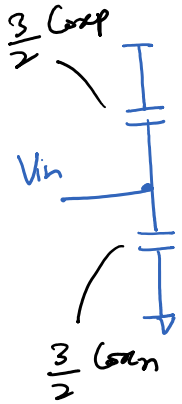
$NM_H = V_{IH} - V_{OH}$

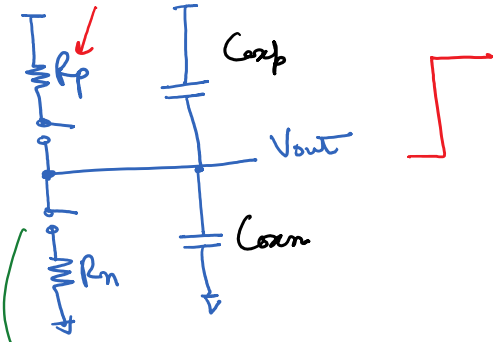
As high NM as possible

See Slides

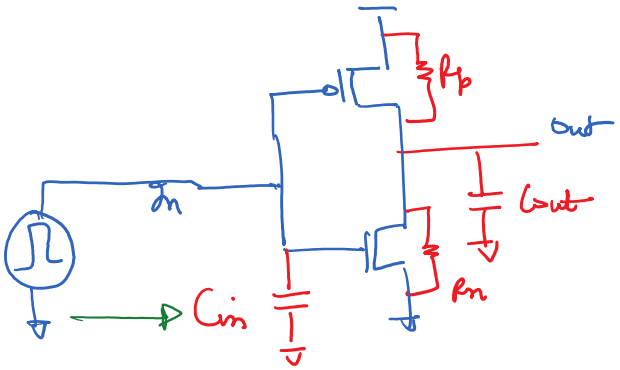
Inverter Delay







only one switch is closed at a time

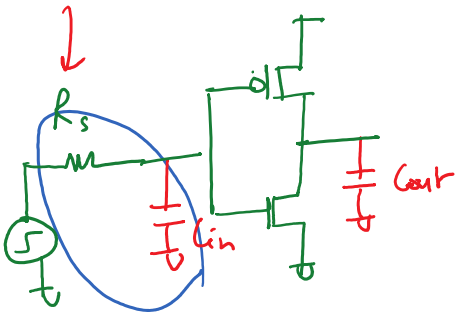


$$C_{in} = \frac{3}{2}\left(C_{gdn} + C_{gdp}\right)$$

$$C_{out} = C_{gdn} + C_{gdp}$$

$$t_{pLH} = 0.7\, R_p \left(C_{gdn} + C_{gdp}\right) = 0.7\, R_p\, C_{out}$$

$$t_{pHL} = 0.7\, R_n\, C_{out}$$

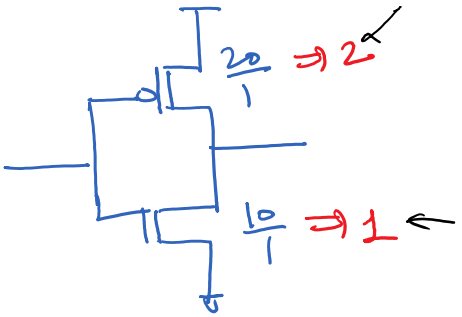


$$\tau = R_s\, C_{in}$$

↳ Assumed infinite input drive strength $\Rightarrow R_s = 0$

$\Rightarrow$ No delay in charging C_{in}

Nano-CMOS $L = 28nm$



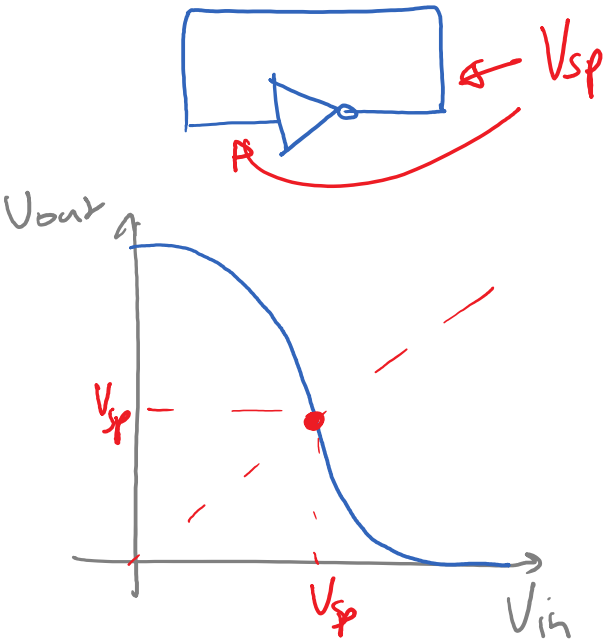
$R_p = R_n = R$

$C_{out} = 3C$

Time constant $= 3RC = 3\tau$

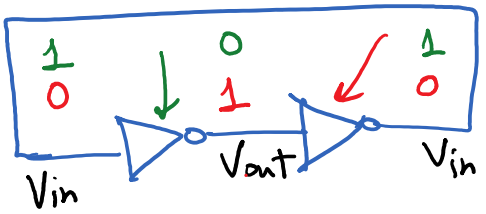
process time constant

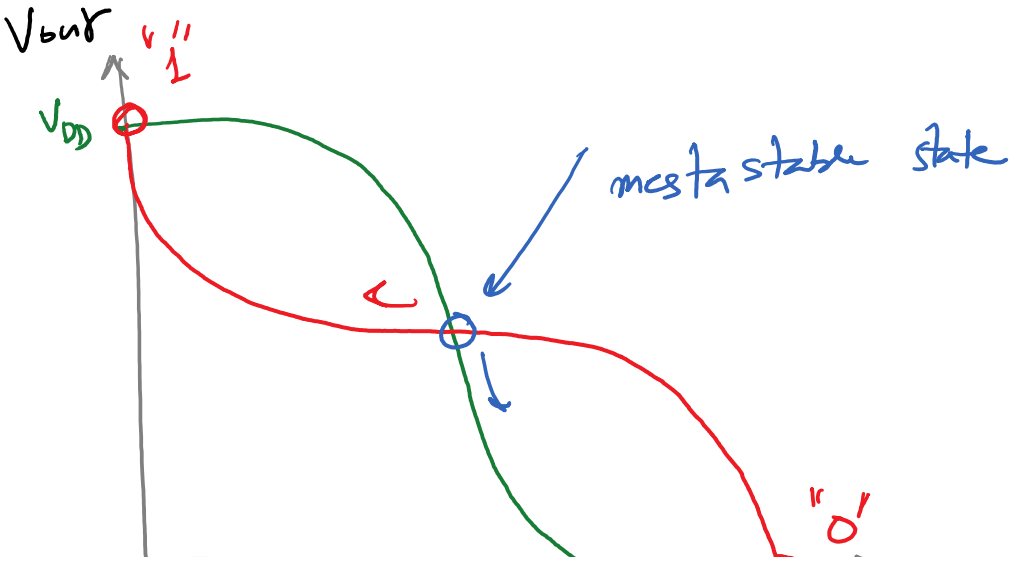
$\tau = RC$

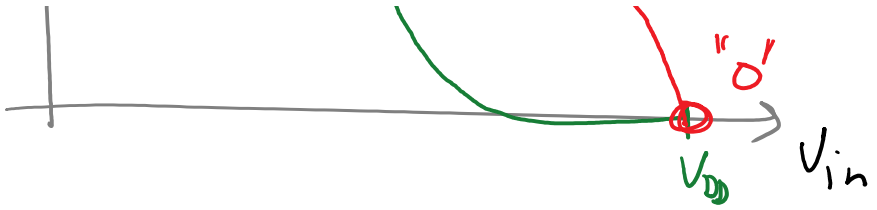


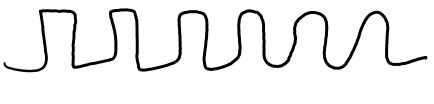
"Latch"

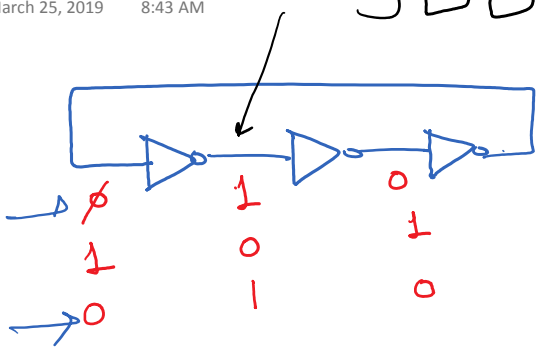
Storage Element






"0"
V_{DD}
V_{in}





Ring Oscillator

one cycle ⇒ 6 delays
or 2n delays
& n ⇒ odd

* Signal feedback is 180° out of phase with odd stages
  - ↳ oscillation
  - ↳ self-starting oscillation

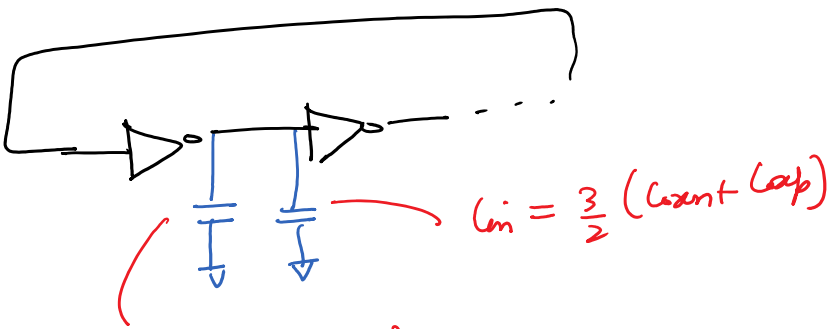
Time period of oscillation

$$T_s = n(t_{pHL} + t_{pLH}) = 2n \cdot t_d$$

if $t_d = t_{pHL} = t_{pLH}$

$$f_{osc} = \frac{1}{T_s} = \frac{1}{n(t_{pHL} + t_{pLH})}$$

* When identical inverters are used for each stage



$C_{tot} = (C_{wire} + C_{cap})$

at any node $C_{tot} = \sum (C_{wire} + C_{cap})$

$\Rightarrow t_{pHL} + t_{pLH} = 0.7 (R_n + R_p) \cdot C_{tot}$

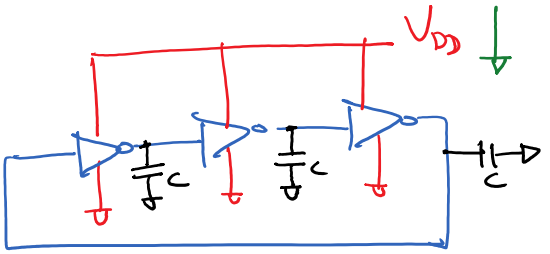
$$f_{osc} = \frac{1}{n \times 0.7 (R_n + R_p) C_{tot}}$$

$C_{tot} \rightarrow \sum (C_{wire} + C_{cap})$

$$f_{osc} = \frac{1}{n(t_{pHL} + t_{pLH})} = \frac{1}{6n\tau}$$

$t_{pHL} + t_{pLH} \rightarrow 3\tau$

* Can estimate process τ from f_{osc}



f_{osc} ↓

V_{DD} ↓ $\Rightarrow$ R_n, R_p ↑ $\rightarrow$ τ ↑ $\rightarrow$ f_{osc} ↓

↳ Voltage controlled oscillator (PLL)

↳ clocking circuitry $\Rightarrow$ PLL

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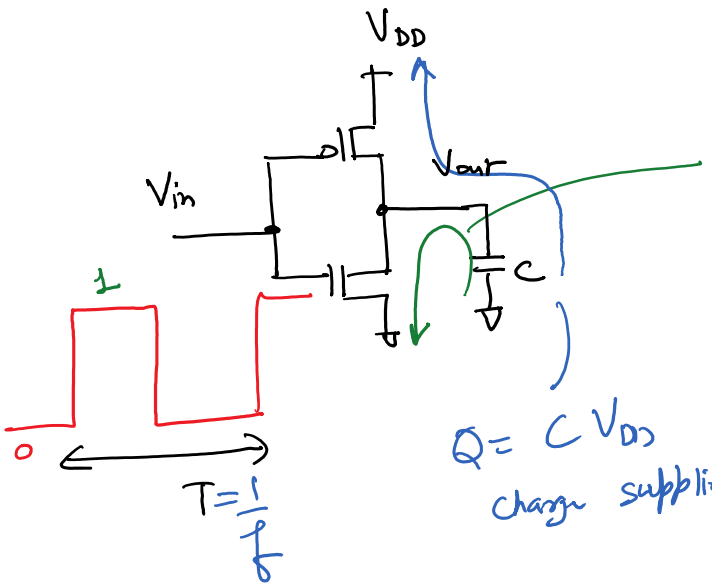
Dynamic Power Consumption:



charge supplied by $V_{DD} = 0$

$Q = CV_{DD}$

charge supplied by V_{DD}

charge supplied in every cycle $= CV_{DD}$

average current pulled from $V_{DD} = \frac{Q}{T} = \frac{CV_{DD}}{T}$

$\Rightarrow$ average power consumption from $V_{DD} = V_{DD} \cdot I_{avg}$

$= \frac{CV_{DD}^2}{T}$

$= CV_{DD}^2 f.$

Dynamic Power

$$P_d = CV^2 f$$

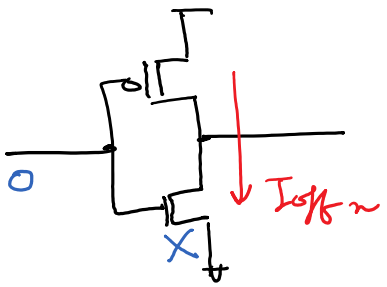
αf

αV_{DD}^2

$P_d = \alpha CV^2 f$

L activity factor $0 < a < 1$

Static Power Consumption:



average $P_s = V_{DD} \times I_{leakage} = V_{DD} \cdot \frac{(I_{off_n} + I_{off_p})}{2}$

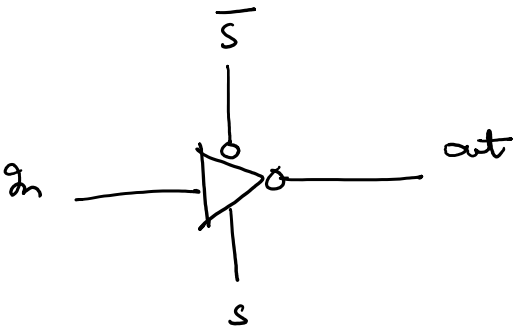
Subthreshold leakage

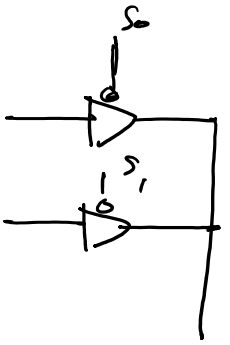
Dynamic & static power consumption

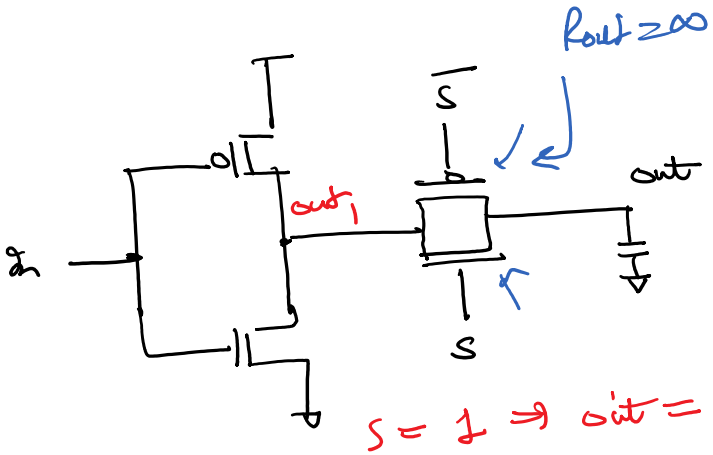
Dynamic Power Consumption $\Rightarrow$ $CV_{DD}^2 f$

Inverter $\Rightarrow$ $n C V_{DD}^2 f_{osc}$

Inverter with a Tristate







$S = 1 \Rightarrow out = out_1 = \overline{in}$

$S = 0 \Rightarrow$ out is in Hi-Z

high-impedance state