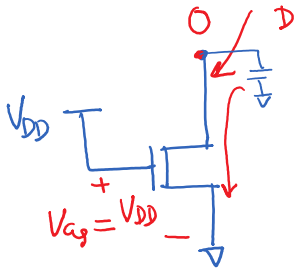
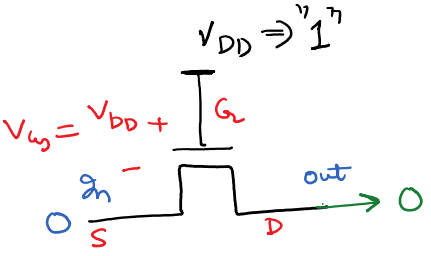
ECE 445 – Lecture 16.

Monday, March 18, 2019 12:29 PM

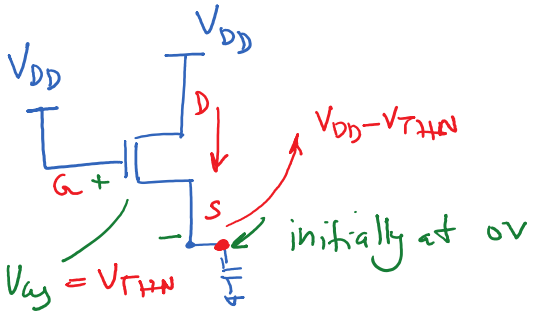
MOSFET Pass gates:



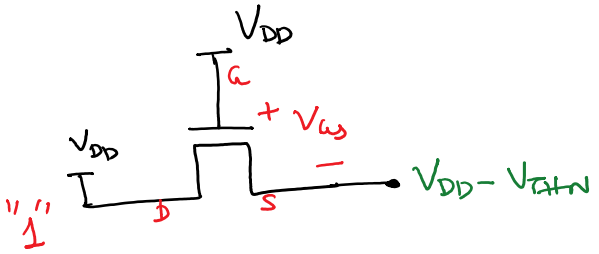
⇒



NMOS is good at "passing" a "0".

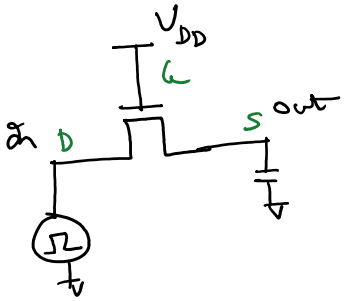


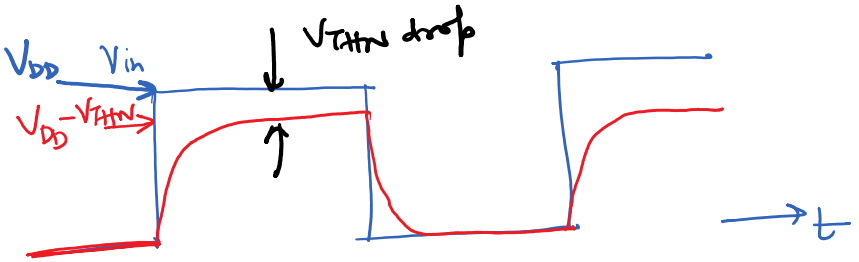
⇒



NMOS is bad at passing a "1".

fig 10.14



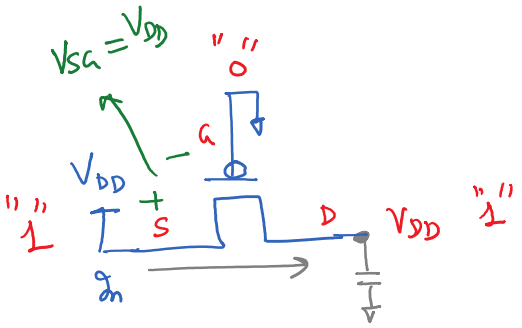


V_{THN} drop include the body effect

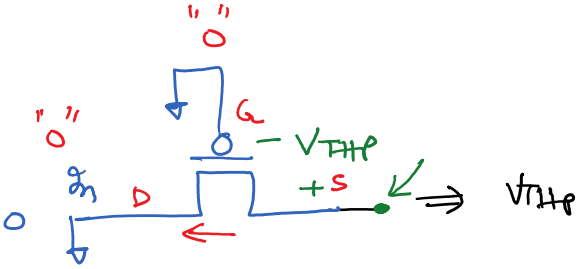
$$V_{THN} = V_{THN0} + \gamma\left(\sqrt{V_{SB} + |2V_{fp}|} - \sqrt{|2V_{fp}|}\right)$$

$V_{SB} = V_{DD} - V_{THN}$

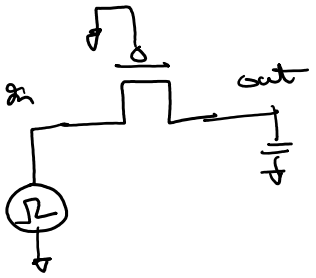
PMOS pass gate

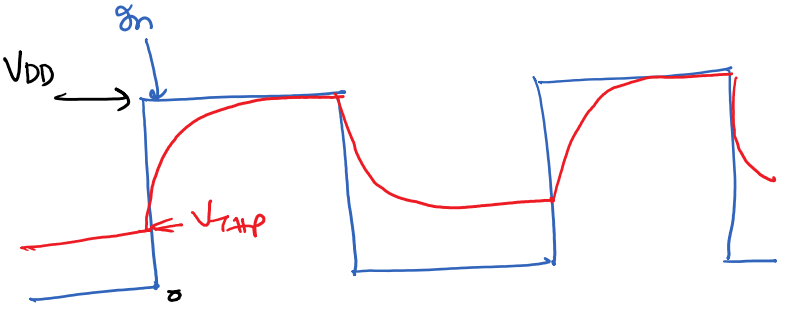


* PMOS is good at passing a "1".

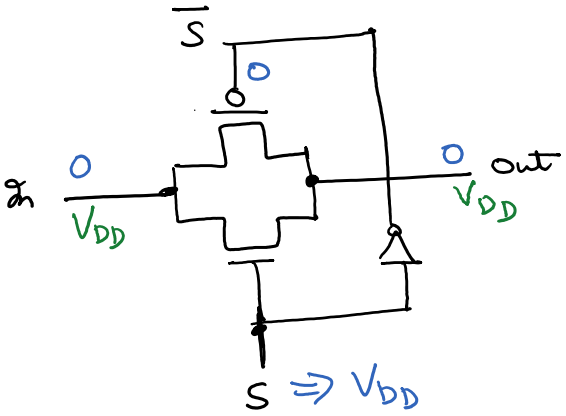


* PMOS is bad at passing a "0" $\Rightarrow V_{THP}$.





Transmission Gate (TG)



(+) rail-to-rail output swing
0 to V_{DD}

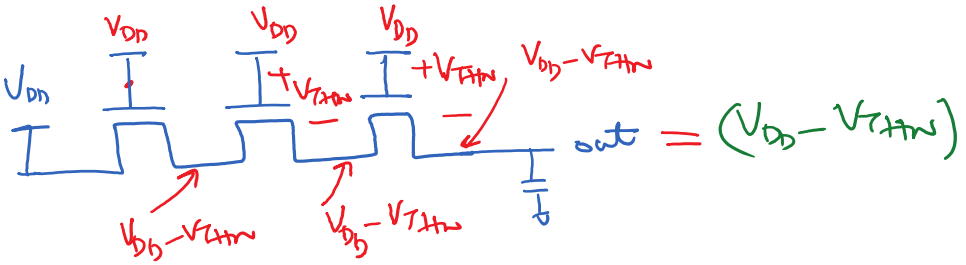
(−) Larger layout Area (4T's)

OR

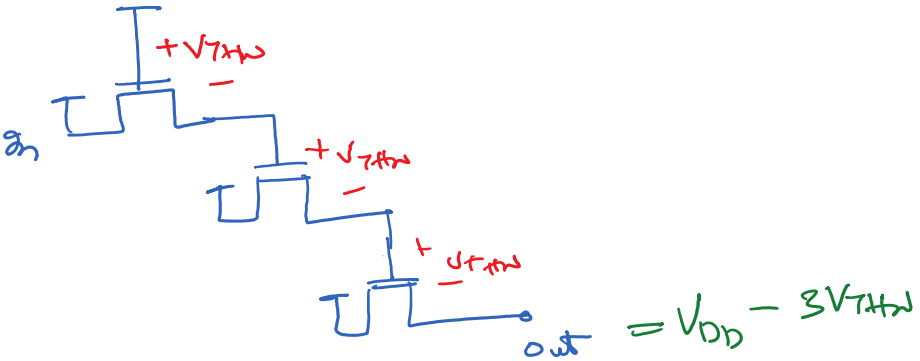
(−) two select lines S & $\overline{S}$

Ex 10.3

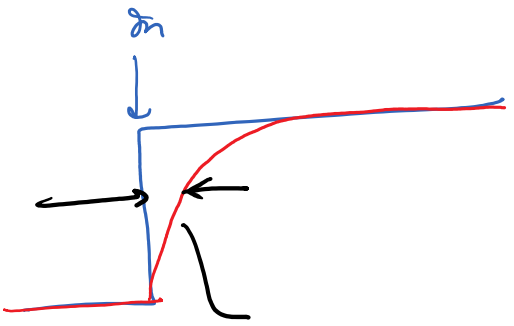
a)



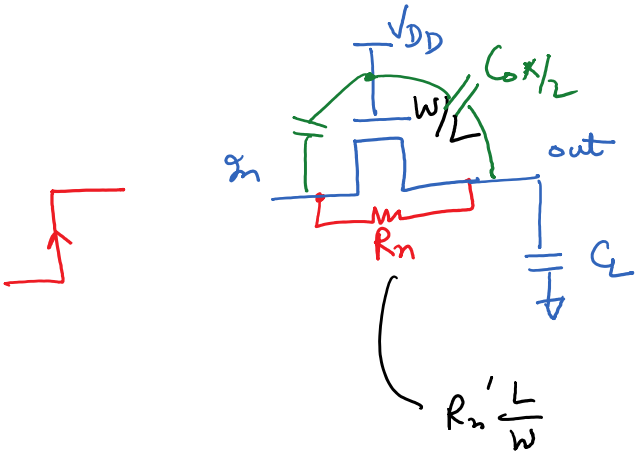
b)



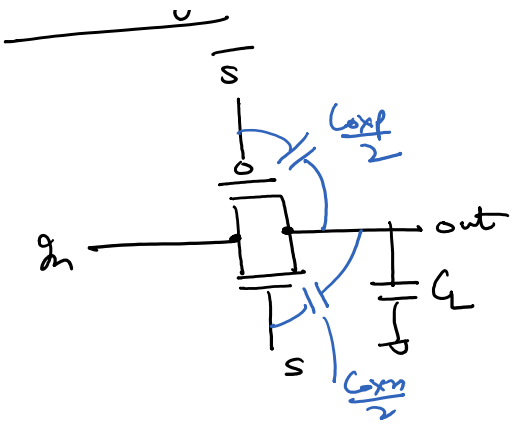
Delay through a pass gate:



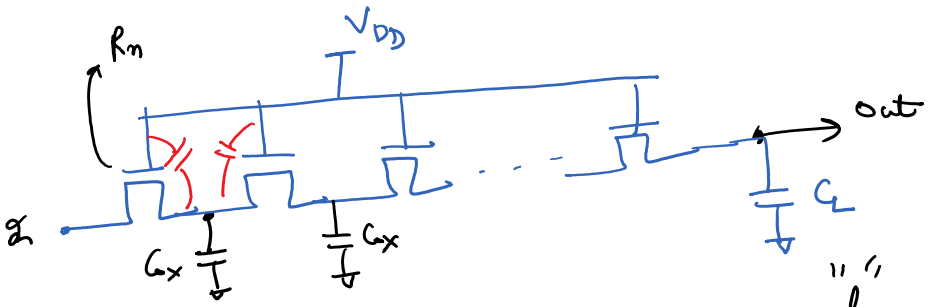
$$t_d = 0.7 R_n \left(C_L + \frac{C_{ox}}{2}\right)$$



TG Delay



$$t_d = 0.7 (R_p || R_n) \left(C_L + \frac{C_{oxn}}{2} + \frac{C_{oxp}}{2} \right)$$

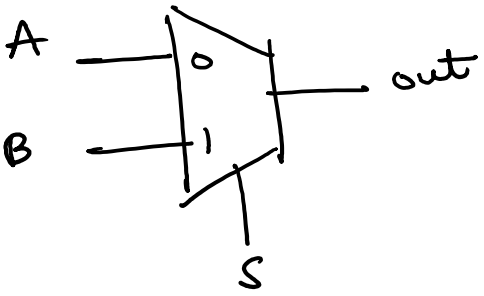


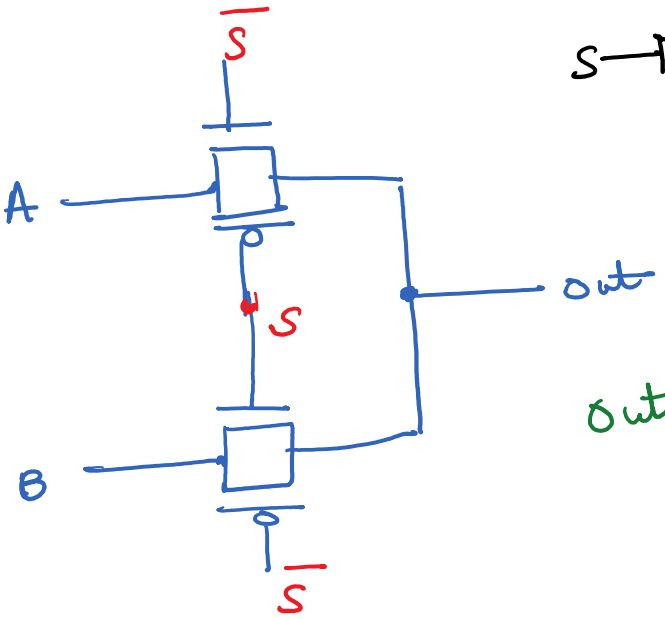
"RC Transmission Line"

"l" gates in series

$$t_d = 0.35 R_n C_x l^2 + 0.7 (l R_n) C_L$$

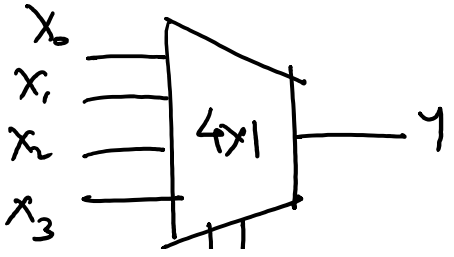
2x1 MUX

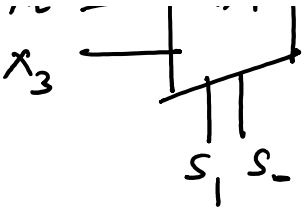


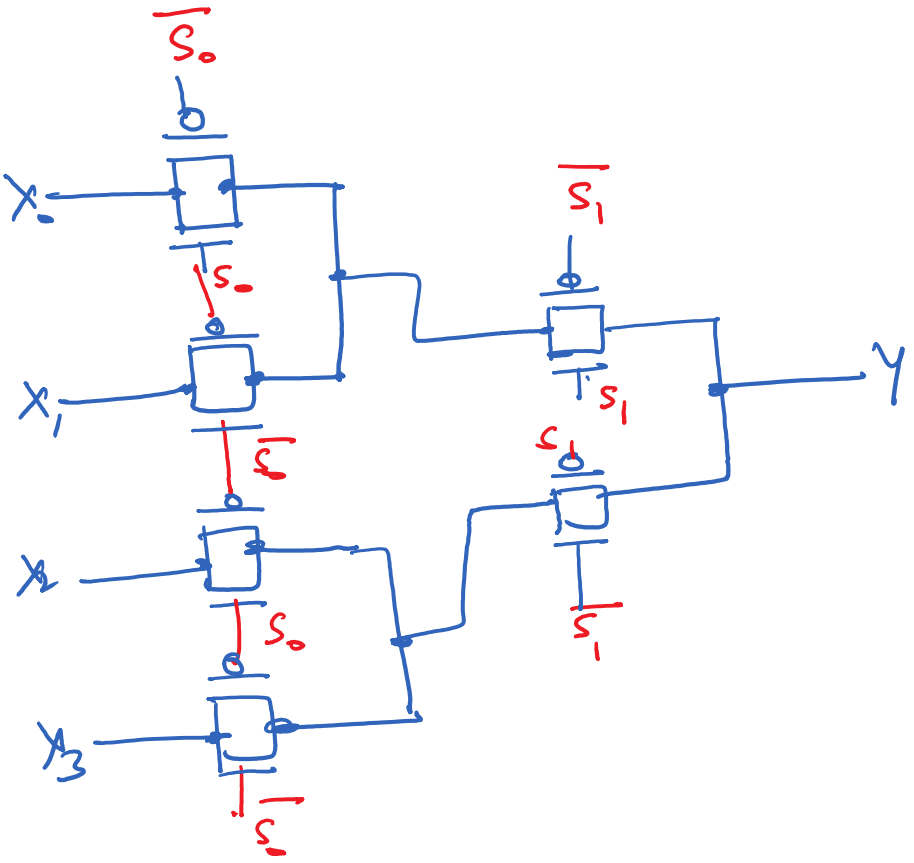


$$out = \bar{S} \cdot A + S \cdot B$$

4x1 MUX




X_3
S_1
S_0


$\overline{S_0}$
X_0
S_0
X_1
$\overline{S_0}$
X_2
S_0
X_3
$\overline{S_0}$
$\overline{S_1}$
S_1
S_1
$\overline{S_1}$
$\overline{S_1}$
Y

S_0 S_1

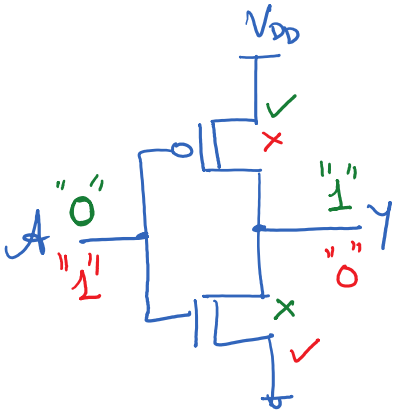
CMOS Inverters:

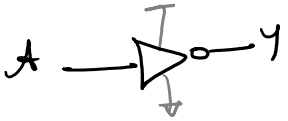
(+) full logic swing $(0 \leftrightarrow V_{DD})$

(+) static power dissipation

$\simeq V_{DD} I_{off} \simeq 0$

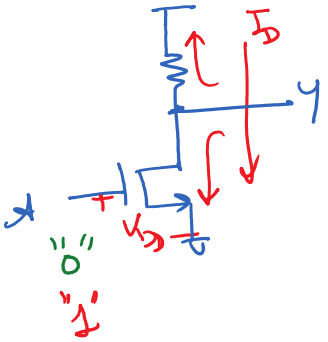
↑ only leakage power





$y = \overline{A}$

NMOS-only logic



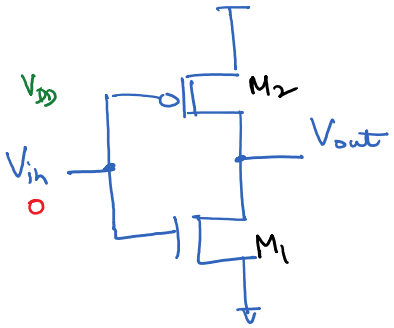
"1" $\in V_{DD}$

out > 0

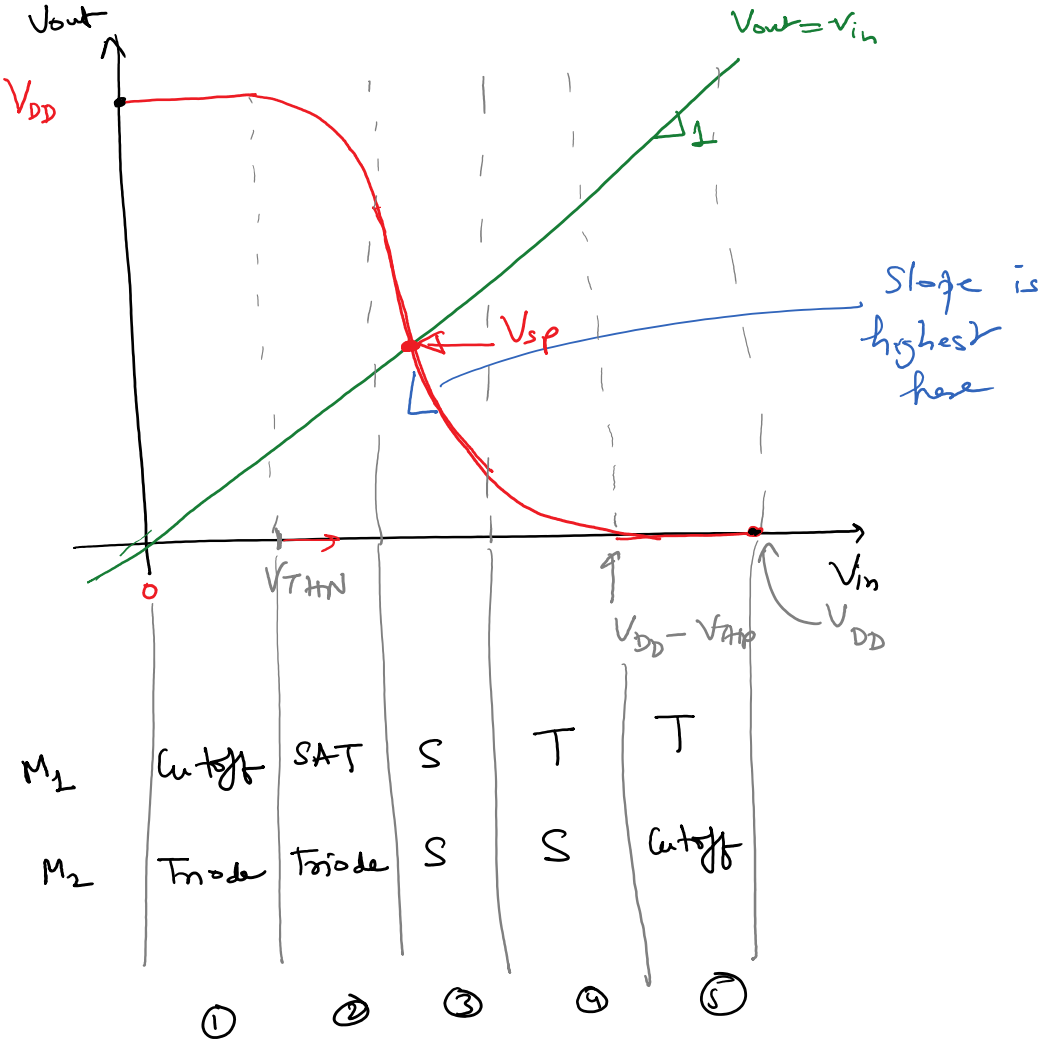
"Static power consumption"

Inverter Voltage Transfer Curve (VTC)

(input–output characteristics)



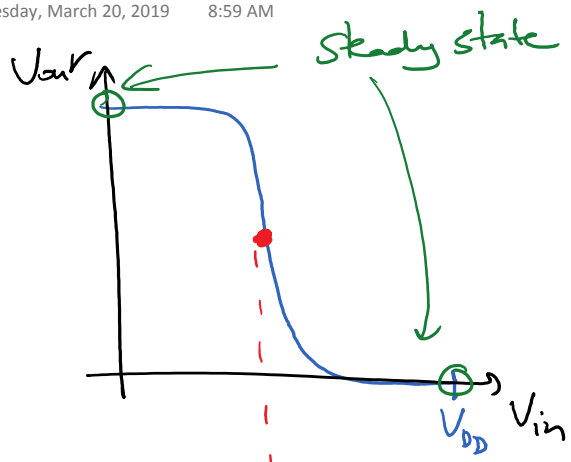
V_{sp} ⇒ switching point

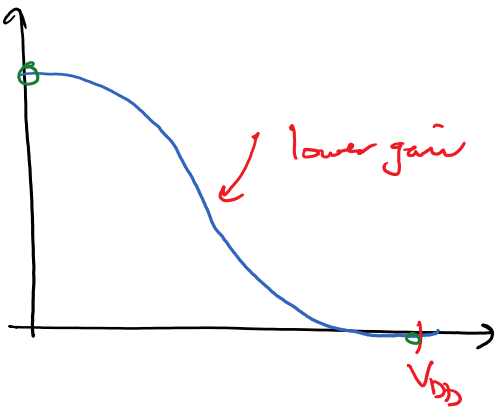


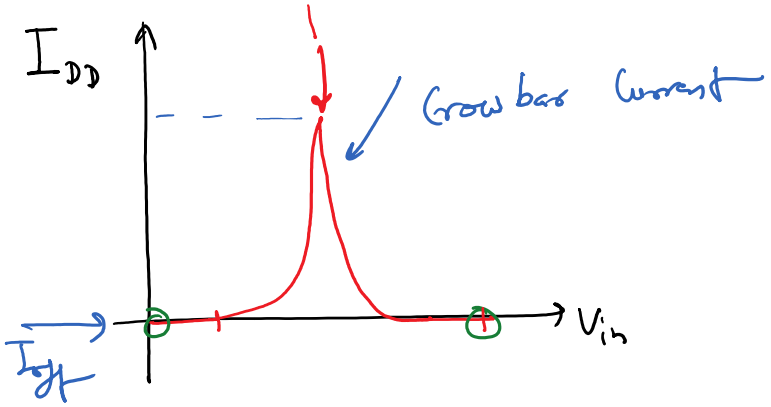
		①	②	③	④	⑤
(NMOS)	M_1	Cutoff	SAT	S	T	T
(PMOS)	M_2	Triode	Triode	S	S	Cutoff

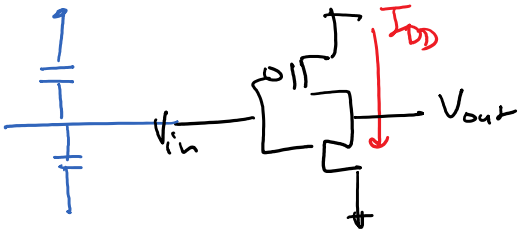
Short channel cmos

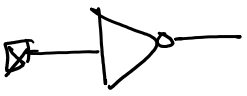
Wednesday, March 20, 2019 8:59 AM



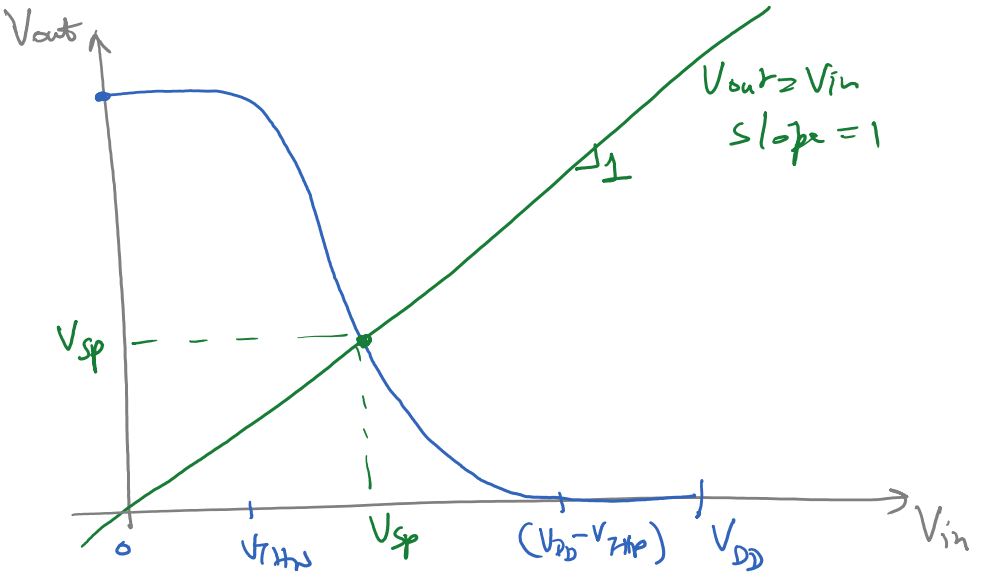


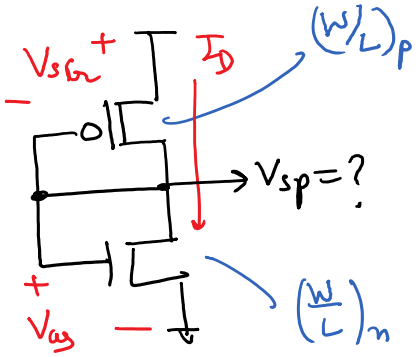






Switching point :





Diode Connected

gate & Drain are connected

Both transistors are in Saturation

$V_{DS} > V_{DS,sat} = V_{GS} - V_{THN}$

$$I_D = \frac{\beta_n}{2}\left(\overbrace{V_{sp} - V_{THN}}^{V_{GS}}\right)^2 = \frac{\beta_p}{2}\left(\overbrace{V_{DD} - V_{sp} - V_{THP}}^{V_{SG}}\right)^2$$

Solve for V_{sp}

$$V_{sp} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THN} + (V_{DD} - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

$$V_{sp} = \frac{\quad}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

V_p depends upon Beta ratio $= \frac{\beta_n}{\beta_p}$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \cdot \left(\frac{W}{L}\right)_n}{(k'_p) \cdot \left(\frac{W}{L}\right)_p} \Rightarrow$$

If $\frac{\beta_n}{\beta_p} = 1 \Rightarrow V_p = \frac{V_{THN} + V_{DD} - V_{THP}}{2} \simeq \frac{V_{DD}}{2}$

desired case

No- skew in the inverter

VTC is symmetric

Both PMOS and NMOS have the same "Drive strength"

Long channel CMOS:

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = 1$$

$$\Rightarrow \frac{(W/L)_p}{(W/L)_n} = \frac{\mu_n}{\mu_p} \simeq 3$$

$L_p = L_n = L_{min}$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \simeq 3$$