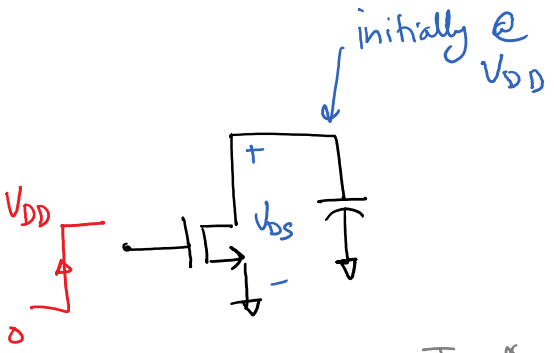
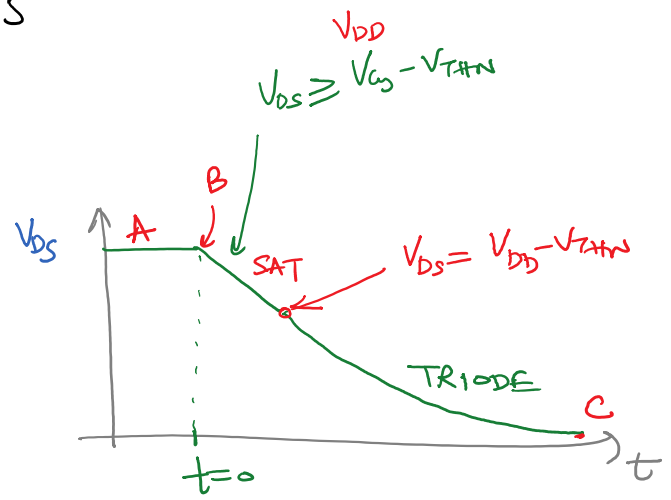
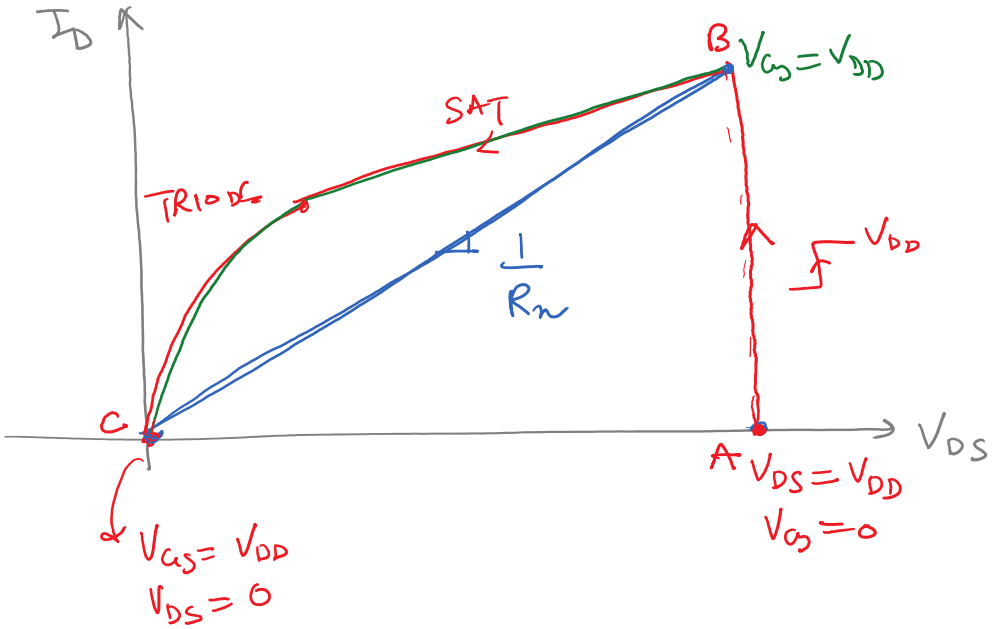
ECE 495 - Lecture 15

Monday, March 18, 2019 10:01 AM

Digital MOSFET Model:







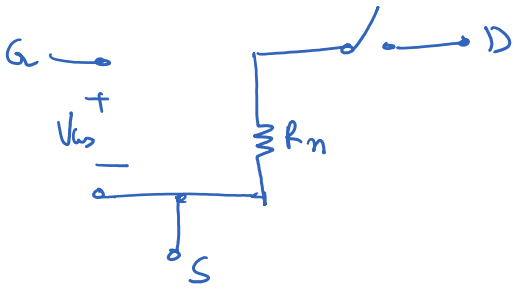
$$R_n = \frac{\Delta V}{\Delta I} = \frac{V_{DD}}{\frac{\beta}{2}(V_{DD} - V_{THN})^2}$$

$$= \frac{V_{DD}}{k_n' \frac{W}{L} \frac{(V_{DD} - V_{THN})^2}{2}}$$

$$= \underbrace{\left(\frac{V_{DD}}{k_n' \frac{(V_{DD} - V_{THN})^2}{2}} \right)}_{R_n'} \cdot \frac{L}{W}$$

R_n'

$$R_n = R_n' \cdot \frac{L}{W}$$



- Switch is closed when $V_{GS} > V_{THN}$
- Switch is open when $V_{GS} < V_{THN}$

On Resistance $\Rightarrow R_n$

off Resistance $\rightarrow \infty$

Table 9.1 from Cmos Book

$L = 1\,\mu m$, $\frac{W}{L} = \frac{10}{1}$

$$R_n = \frac{V_{DD}}{I_{D,sat}} = \frac{5V}{3.3\,mA} \simeq 1.5\,k\Omega$$

$$R_n = R_n' \left(\frac{L}{W}\right)$$

$$\Rightarrow R_n' = R_n \cdot \left(\frac{W}{L}\right) = 1.5\,k\Omega \times \frac{10}{1} = 15\,k\Omega$$

Similarly from I-V curves for the PMOS

$$R_p = 45\,k\Omega \cdot \frac{L}{W}$$

R_p'

PMOS → $\frac{R_p'}{R_n'} = \frac{k_{Pn}}{k_{Pp}} = \boxed{\frac{\mu_n}{\mu_p} \simeq 3}$ in silicon before velocity saturation

NMOS

electron mobility = 3x hole mobility

$\Rightarrow \quad R_p' = 3X \; R_n'$

$\Rightarrow$ Effective switching resistance of PMOS is roughly 3X than that of the NMOS in long-channel cases.

Short-channel : CMOS Book Example of 50nm CMOS

$$R_n = \frac{V_{DD}}{I_D} = \frac{V_{DD}}{I_{on} \cdot W \cdot (\text{scale})} = \frac{1V}{600\frac{\mu A}{\mu m} \times W \times \text{scale}} \longrightarrow 50nm$$

$$= \frac{34k\Omega}{W}$$

$$R_p = \frac{68k\Omega}{W}$$

ratio of saturation velocities in short channel CMOS.

$$\frac{R_p}{R_n} = \frac{v_{satn}}{v_{satp}} \simeq 2$$

PMOS switch resistance is 2x of NMOS.

↳ $\frac{R_p}{R_n}$ ratio depends upon the exact process and needs to be characterized using the I-V curves.

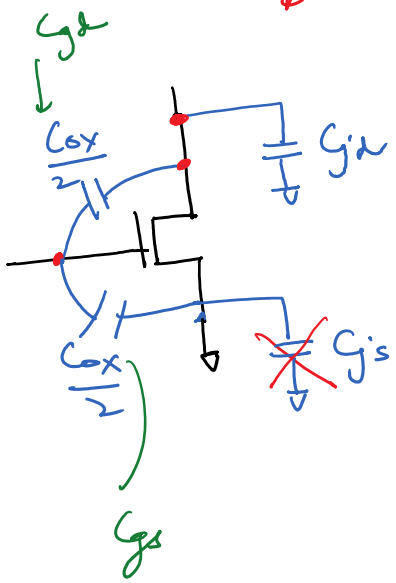
Capacitance Models:

CMOS Textbook:

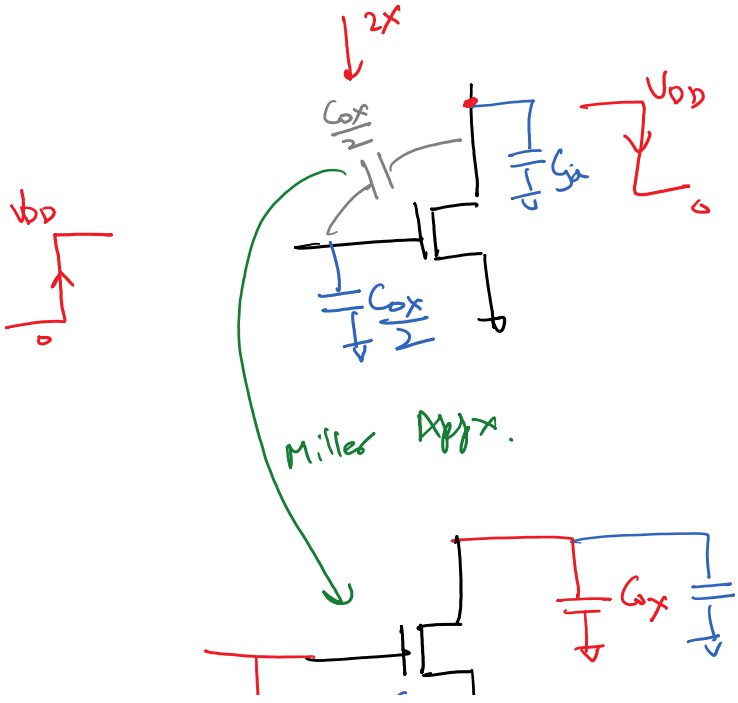
NMOSFET spends most of the time in Triode region while switching

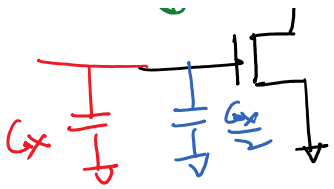
→ Using Triode capacitance

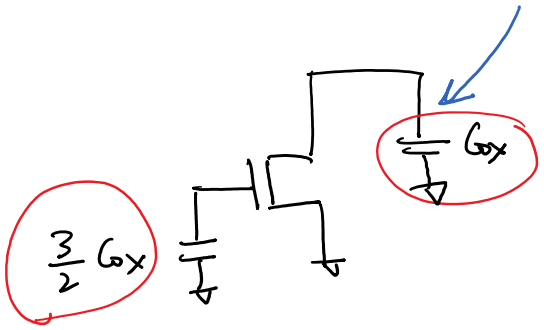
↳ overestimate in Saturation

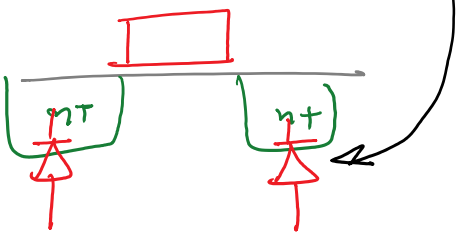


Apply Miller Approximation to Cgd

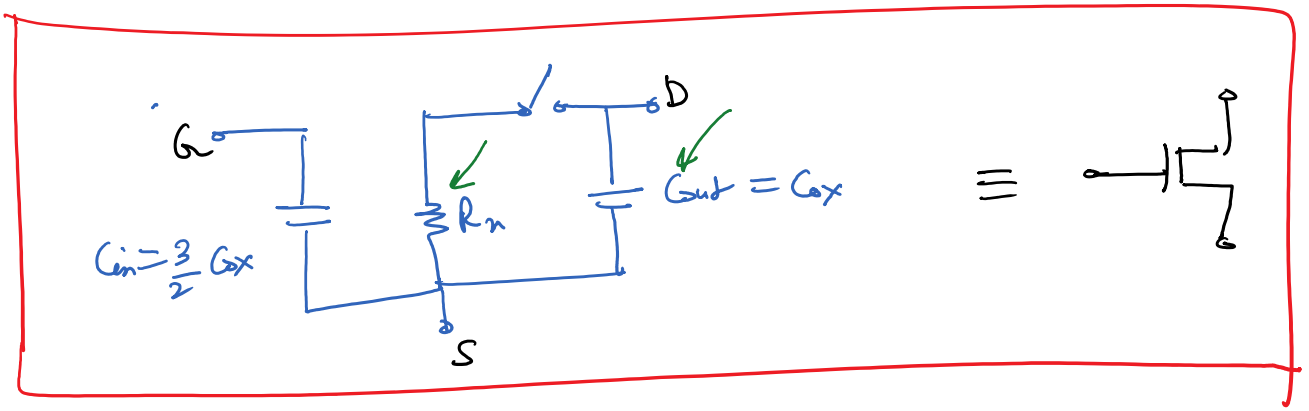






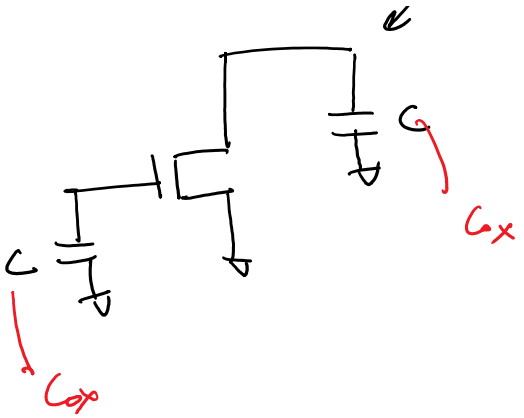


Complete Model for the NMOS switch



Other Models

Synthesis tools using Logical Effort


G
Cox
C
Cox

Process Characteristic Time Constant :

↳ intrinsic switching speed of MOSFET.

Long-channel CMOS:

$$\tau_n = R_n C_{ox} = \frac{2L \cdot V_{DD}}{k' \mu_n \frac{W}{L} (V_{DD} - V_{Tn})^2} \cdot C_{ox}' \frac{W}{L} L^2 (\text{scale})^2$$

$$= \frac{2 C_{ox}' V_{DD} \cdot L^2 \cdot (\text{scale})^2}{k' \mu_n (V_{DD} - V_{Tn})} \quad \propto L^2$$

Speed increases as $\frac{\alpha 1}{L^2}$

↳ Speed doubles for every decrease in length by $\sqrt{2}$.

for Short-channel CMOS process :

$$\tau_n = R_n C_{ox} = \frac{V_{DD}}{I_{on} \cdot W \cdot (\text{scale})} \cdot C_{ox}' W L (\text{scale})^2$$

$$= \frac{V_{DD} \cdot C_{ox}' \cdot L \cdot \text{scale}}{I_{on,n}} \quad \propto L$$

Speed $\propto \frac{1}{L}$

$\Rightarrow$ Use minimum channel length for maximum speed in a technology.

From CMOS book:

Long-L (1μm)

C_{ox}'

$$\tau_n = \underbrace{15k \cdot \frac{L}{W}}_{R_n'} \times 1.75 \frac{fF}{\mu m^2} \cdot L \cdot W \cdot (scale)^2 \simeq 25 ps$$

$$\tau_p = R_p C_{ox} \simeq 75 ps$$ 3x slower than NMOS

Book short channel (50nm)

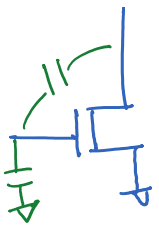
$$\tau_n = \frac{17 k\Omega \, \mu m}{W \cdot scale} \times 25 \frac{fF}{\mu m^2} WL(scale)^2 = 2.1 ps$$

$$\tau_p = 4.2 ps$$ PMOS is 2x slower than NMOS

Intrinsic delay

$\tau_n = R_n C_{ox}$ $\propto L^2$ or L

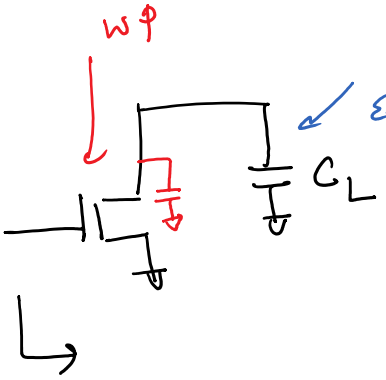
independent of W?

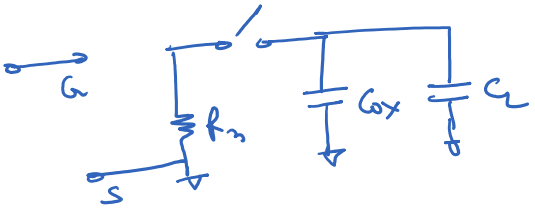


$\left(\frac{W}{L}\right)\uparrow \Rightarrow R_n \downarrow$

$C_{ox} = C_{ox}' WL \uparrow$

↑ Delay when the N/PMOS switch is driving its own parasitic capacitance





$$\tau = R_n (C_{ox} + C_L)$$

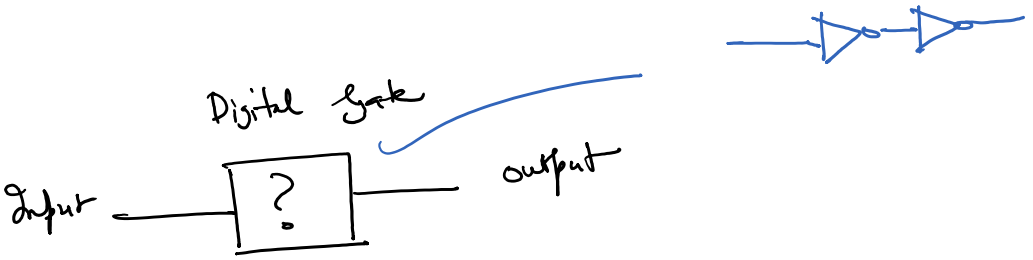
$$\frac{\tau}{\tau_n} = \frac{R_n(C_{ox} + C_L)}{R_n C_{ox}} = \left(1 + \frac{C_L}{C_{ox}}\right) \downarrow$$

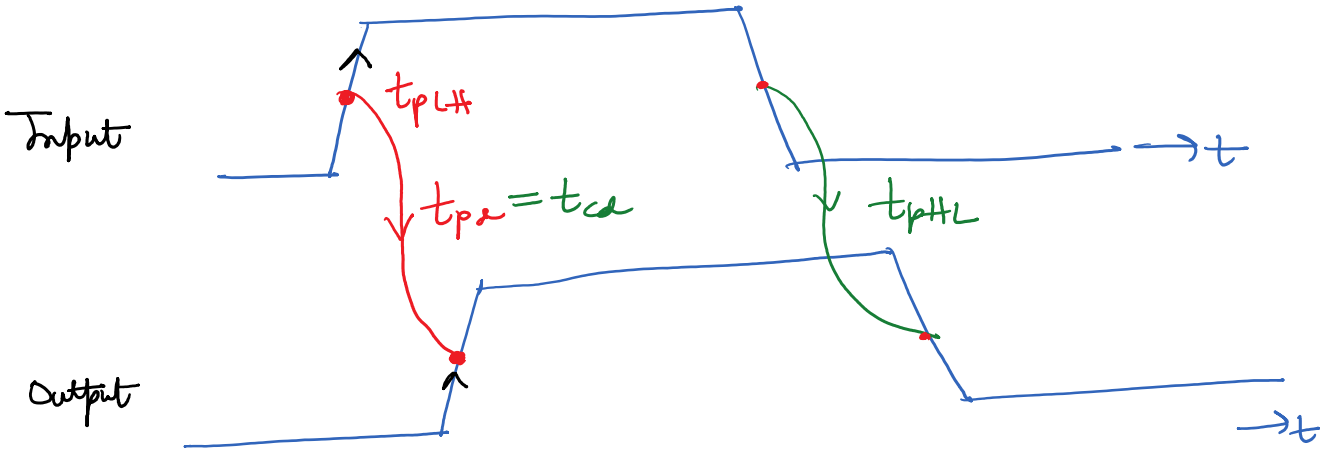
fixed

$W\uparrow \Rightarrow C_{ox}\uparrow$

∴ Naturally the switching delay will decrease with $\left(\frac{W}{L}\right)\uparrow$ when driving a fixed load.

Delay Definitions in a Digital Circuit:



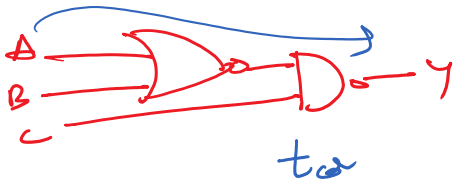


Propagation Delay:

t_{pd} ⇒ maximum time from the input crossing 50% to the output crossing 50% value.

Contamination Delay

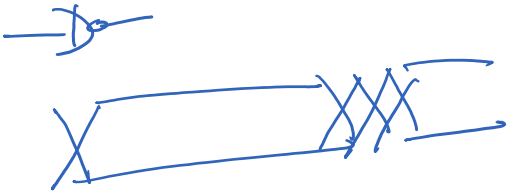
t_{cd} ⇒ minimum time from input crossing 50% to the output crossing 50%.



t_d

t_{pHL} ⇒ propagation delay time for output going high to low

t_{pLH} ⇒ " " " output going from low to high

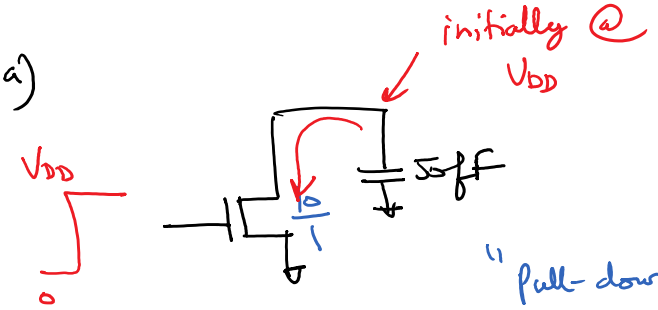


$t_d = 0.7RC$ ← propagation delay

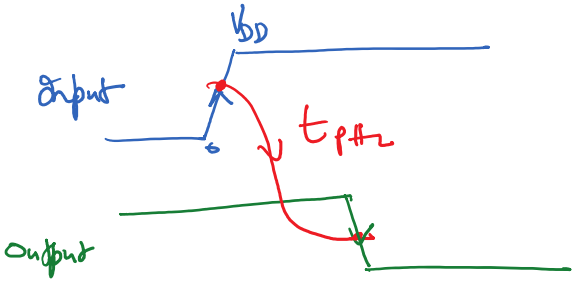
⇒ $t_{rise} = 2.2RC$ ← 10% to 90% rise time

Book Example 10.2 :

a)



find t_{pHL}



$$t_{pHL} = 0.7\, R_n C_{tot}$$

Cont + load capacitance

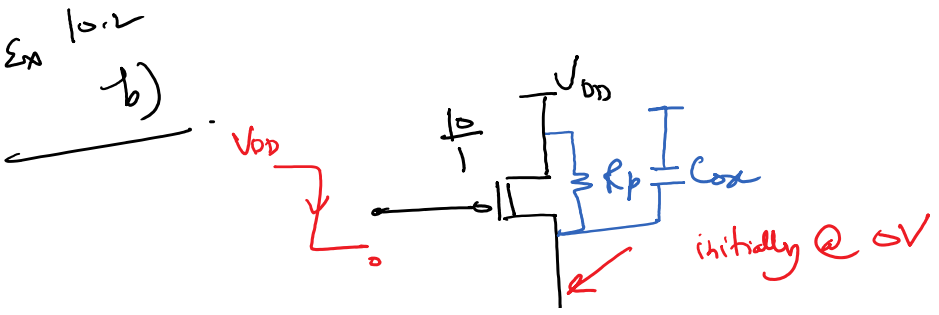
$$= 0.7 \times R_n \times (C_{ox} + C_L)$$

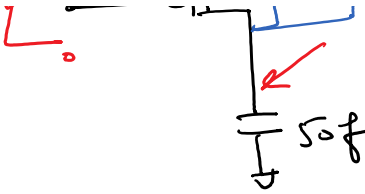
$$= 0.7 \times 15k\Omega \cdot \frac{1}{10} \times \left(1.75\frac{ff}{\mu m^2} \times 10 \times 1 + 50ff\right)$$

R_n ! $\frac{L}{W}$

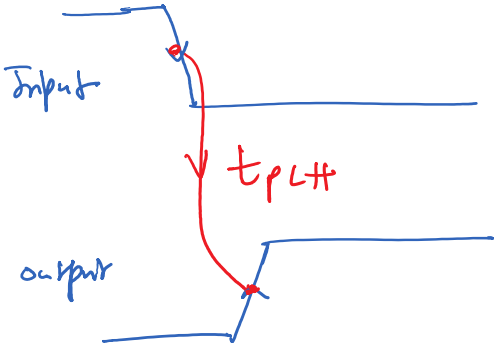
$$\approx 7ps$$

Ex 10.2 b)





"pull-up switch"

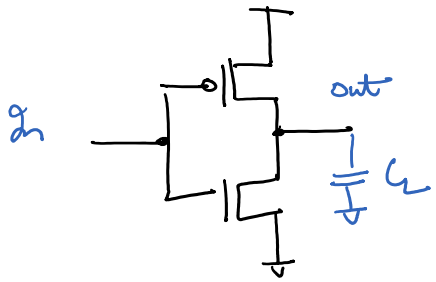


$t_{pLH} = 0.7 R_p C_{out}$

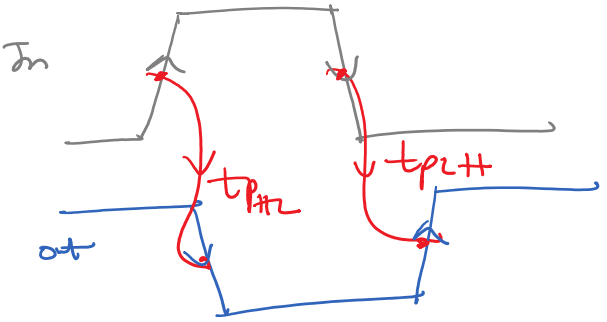
$= 0.7 \times 45k\Omega \left(\frac{L}{W}\right) \left[1.95\frac{fF}{\mu m^2} \times WL + 50pF\right]$

$\approx 210ps$

3X worse delay due to the PMOS



CMOS Inverter.



CMOS Book chapter 10