

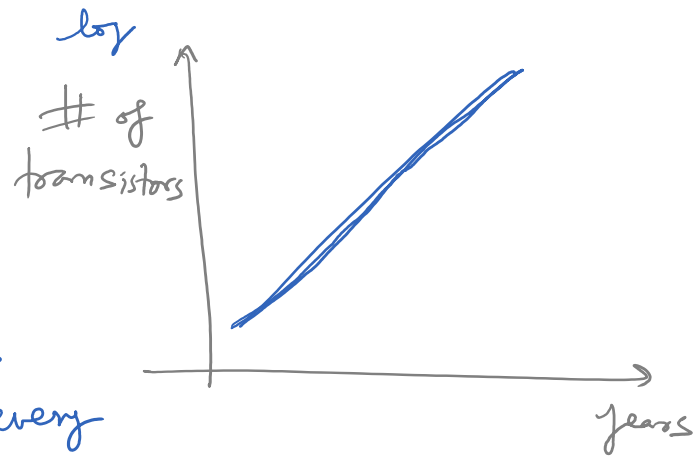
ECE 445- Lecture 14

Wednesday, March 6, 2019 8:05 AM

CMOS Scaling:

Moore's Law

2x the number of transistors
in the same chip area every
2 years



* In every generation the length of the MOSFET
was shrunk by a factor of $S = \sqrt{2} = 0.7$

$$L' = L \cdot S$$

$$W' = W \cdot S$$

$$\text{Area} \propto WL \Rightarrow S^2 = 2$$

$$V_{DD} \rightarrow S$$

$$t_{ox} \rightarrow S$$

$$N_A \rightarrow S^{-1}$$

$$C_{ox}' \rightarrow S$$

Drive
Current

$$I_{on} \rightarrow S^{-1}$$

$$\text{gate Delay} \rightarrow S^{-2}$$

stopped now due to tunneling
 $\epsilon_{ox} \uparrow$

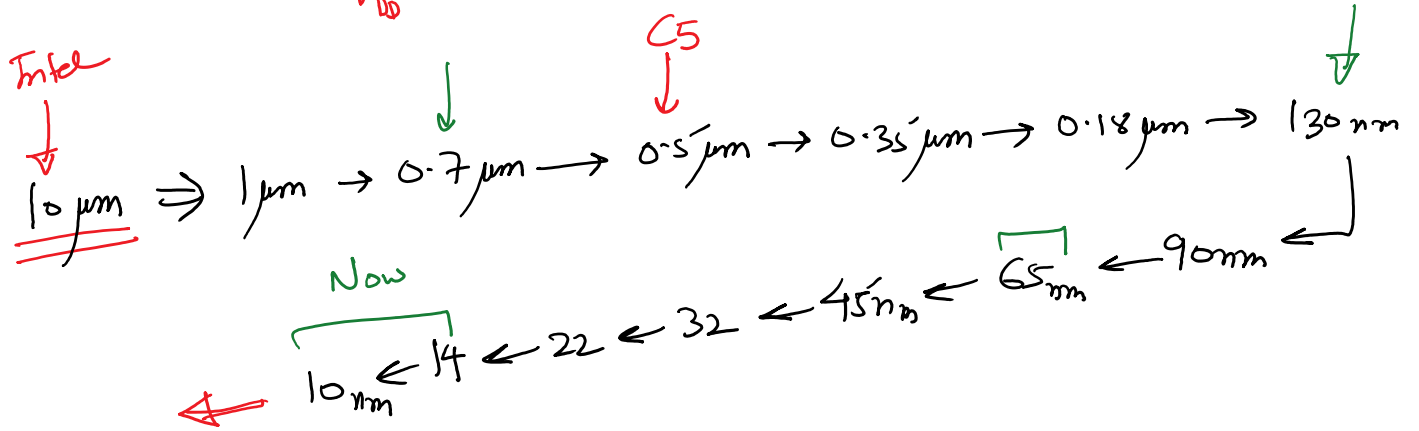
Constant-field scaling

Later

↳ combination of constant
field and constant
supply voltage

gate Delay $\rightarrow \sim$
 Area $\rightarrow s^2 \leftarrow$
 Active Power $\rightarrow s^3 \leftarrow$

per -
 supply voltage
 scaling.



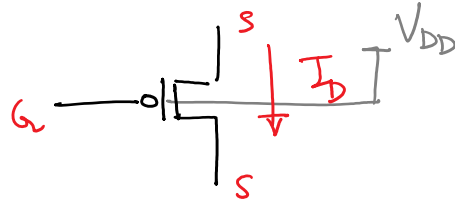
ARM

Chapter 10

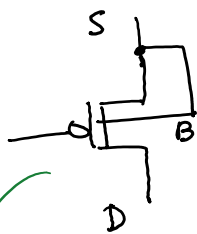
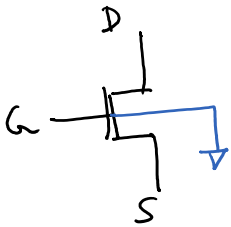
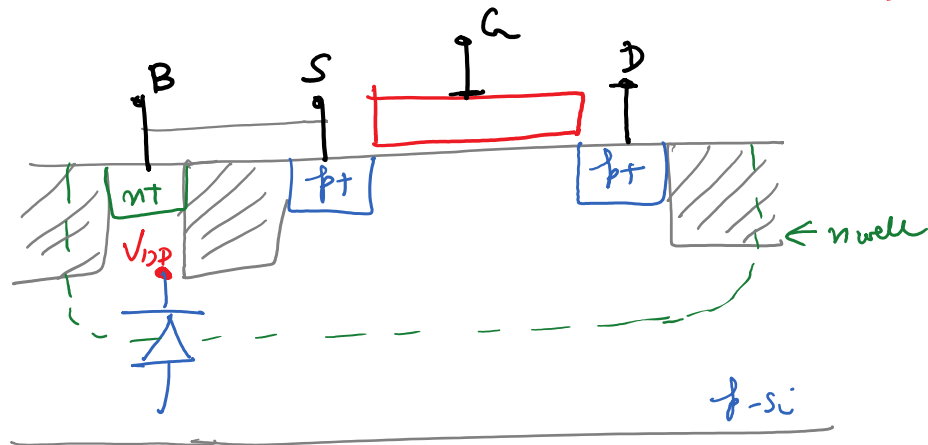
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Models for Digital Design :

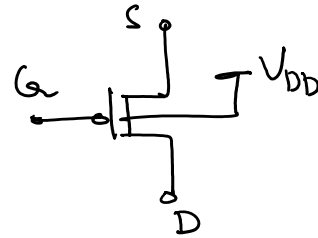
PMOS



* N-well (body) of the PMOS is tied to the highest potential (V_{DD})



OR



possible in CMOS

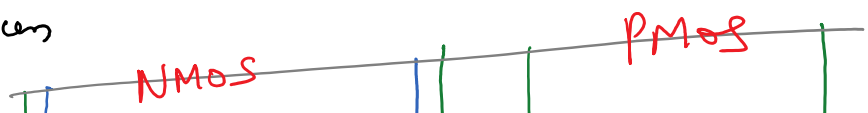
↳ each PMOS can have its own n-well (body)

Can set

$V_{SB} = 0$

↳ No body-effect

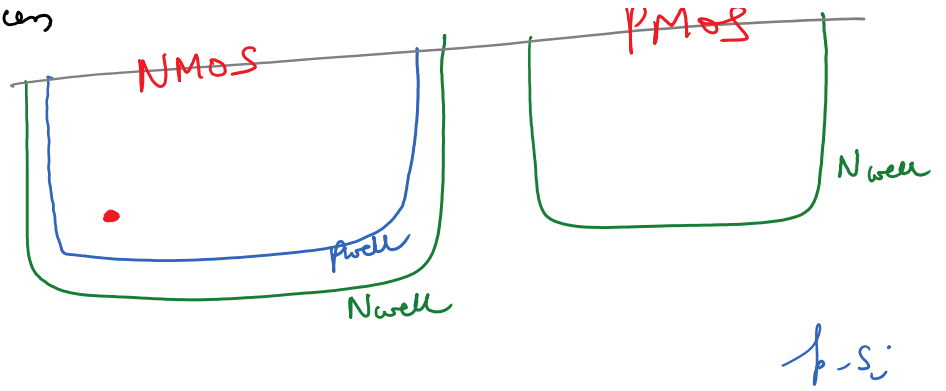
* Triple Well process



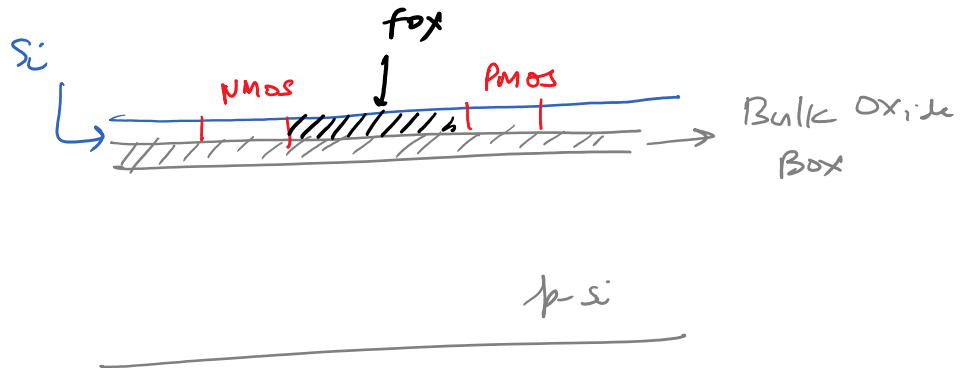
* Triple Well Process

Scattering due to
excessive doping

↳ Electron
mobility will be
lower in the NMOS.

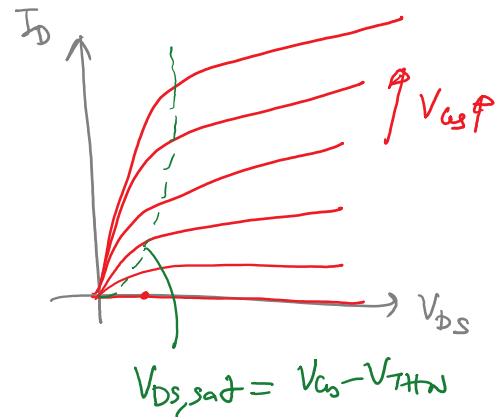
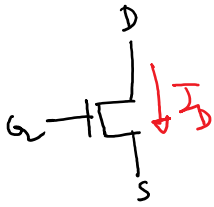


SOI

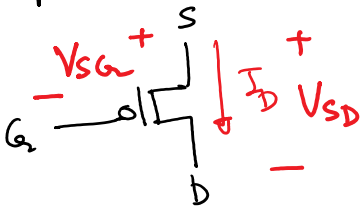


PMOS \Rightarrow All positive convention

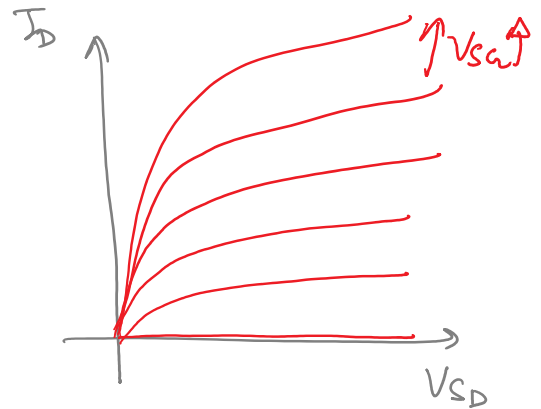
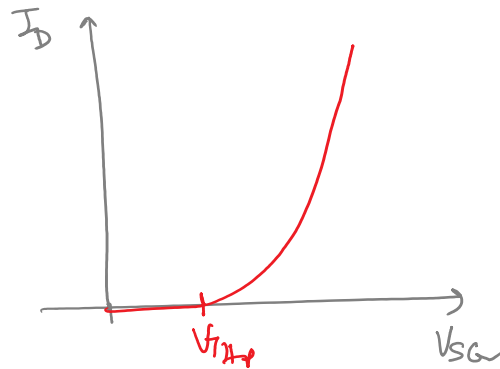
NMOS



PMOS



$V_{GS} \rightarrow V_{SG}$
 $V_{DS} \rightarrow V_{SD}$



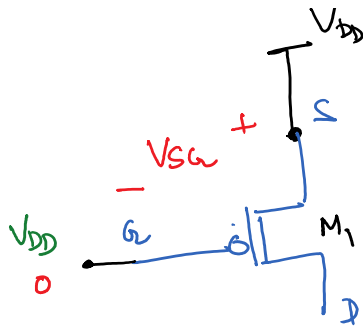
$$I_D = \begin{cases} 0 & V_{GS} < |V_{THP}| \quad \text{cutoff} \\ k_p \frac{W}{L} \left[(V_{GS} - V_{THP}) V_{SD} - \frac{V_{SD}^2}{2} \right] & V_{SD} < V_{SD,sat} = V_{GS} - V_{THP} \quad \text{Triode} \\ \frac{1}{2} k_p \frac{W}{L} (V_{GS} - V_{THP})^2 & V_{SD} > V_{SD,sat} \quad \text{Saturation} \end{cases}$$

$V_{GS} > |V_{THP}|$

in this convention V_{THP} & I_D are positive.

$T_{V_{DS}}$

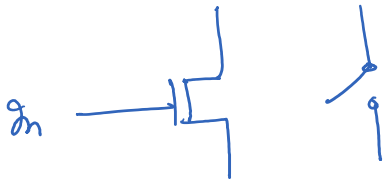
$\rightarrow V_{THP}$



$$I_D > 0 \Rightarrow V_{sw} > V_{thp}$$

"1" $\Rightarrow V_{DD} \Rightarrow M_2$ cut off

"0" $\Rightarrow 0 \Rightarrow V_{sw} = V_{DD} \Rightarrow M_2$ is ON



$g_n = "0" \Rightarrow$ switch is off

"1" \Rightarrow turns on the switch



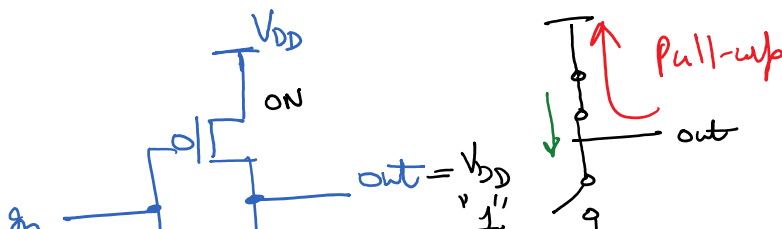
$g_n = "0" \Rightarrow$ turns ON the switch

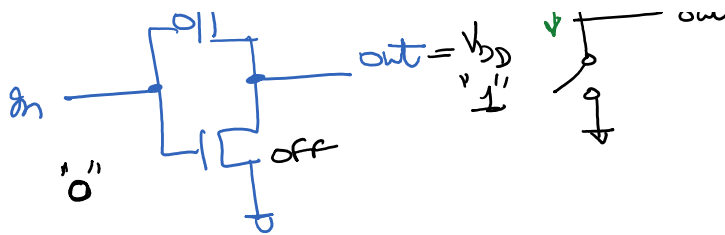
"1" \Rightarrow switch is off

NMOS + PMOS = CMOS
Complementary MOS
* Complementary logic

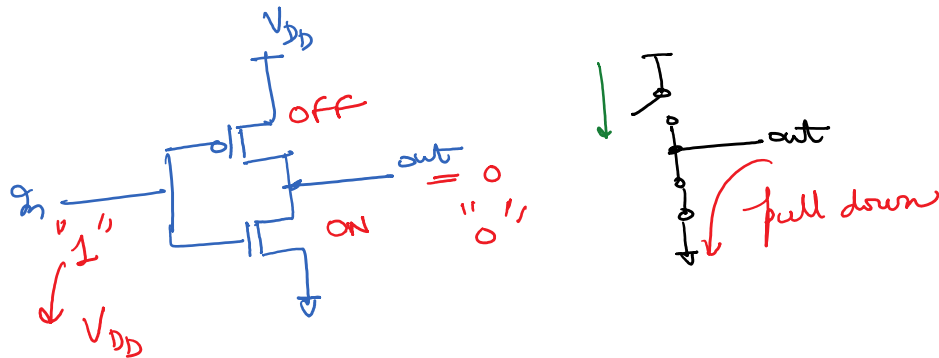
Example:

CMOS Inverter (NOT Gate)



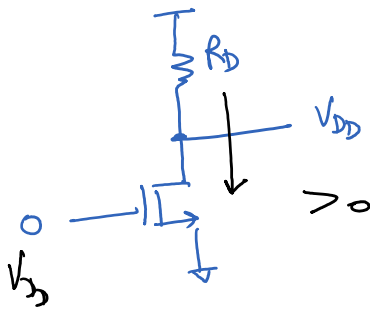


Static Current
= off current
 ≈ 0

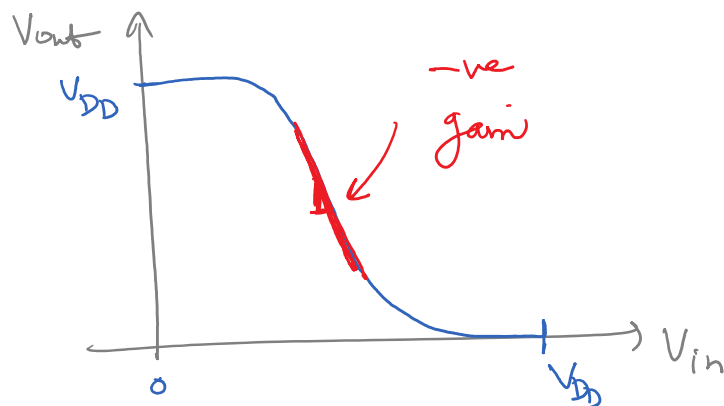


$$out = \overline{in}$$

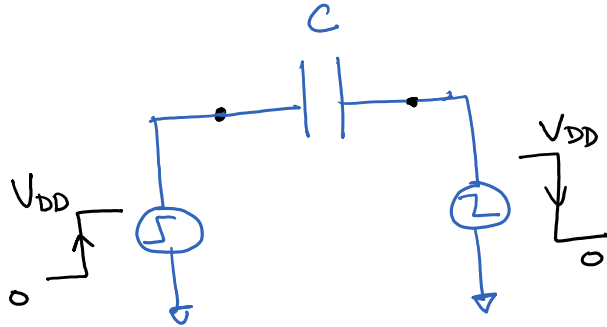
NMOS-only logic



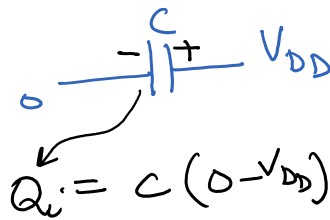
static current $\neq 0$



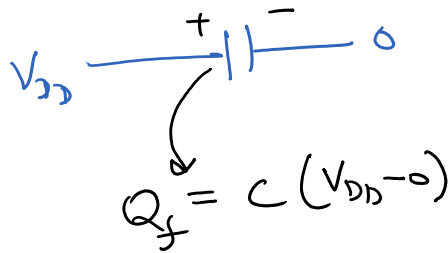
Miller Capacitance :



before switching :



After switching :



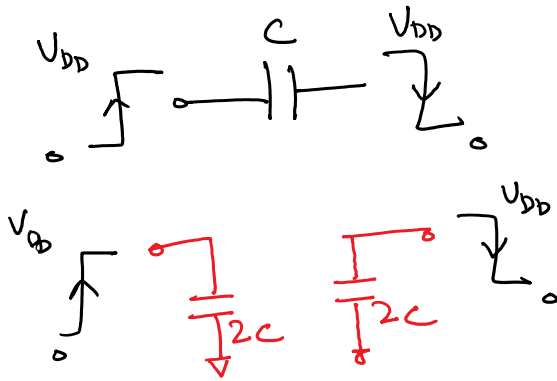
net change $\Delta Q = Q_f - Q_i = 2CV_{DD}$

* charge supplied by the source = $2CV_{DD}$

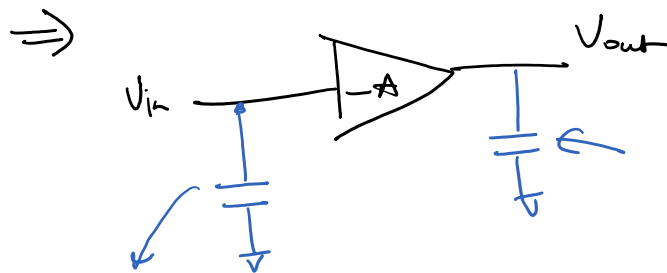
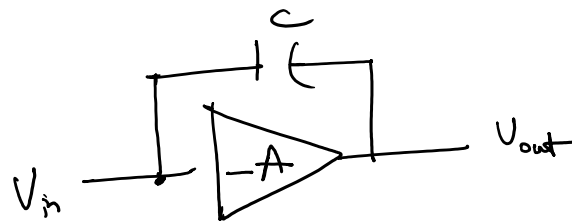
\Rightarrow Effective input capacitance = $\frac{\Delta Q}{V_{DD}} = \frac{2CV_{DD}}{V_{DD}} = 2C$

∴ net input = $\frac{\Delta Q}{V_{DD}} = \frac{2CV_{DD}}{V_{DD}} = 2C$

* Charge sink by the ...



in general



$$C_{in} = C(1 + |A|)$$

$$\approx AC \text{ for } |A| \gg 1$$

$$C_{out} = C\left(1 + \frac{1}{|A|}\right)$$

$\approx C \text{ for } |A| \gg 1$

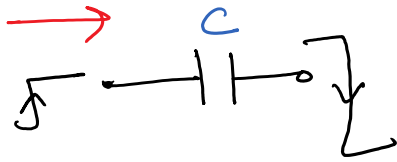
* Miller Effect \rightarrow Capacitance Multiplication Effect

for an inverter, gain = -1

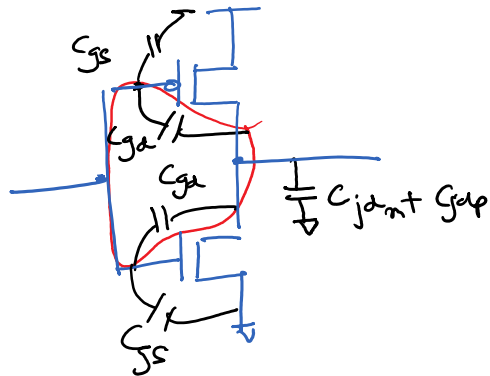
$$C_{in} = 2C$$

$$C_{out} = 2C$$

$$C_{in} = AC$$



parasitic capacitance



$C = C_{gd} + C_{ga}$ is the Miller Capacitance

