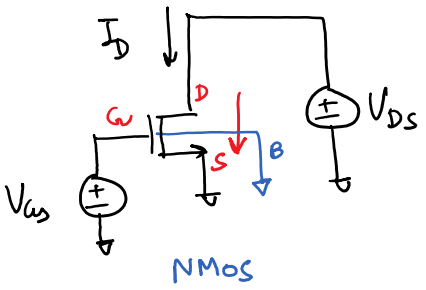
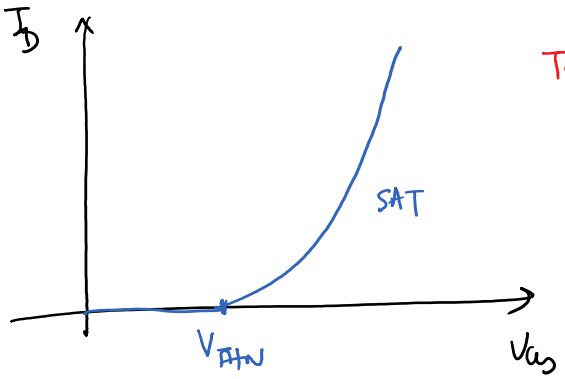
ECE 445 - Lecture 11

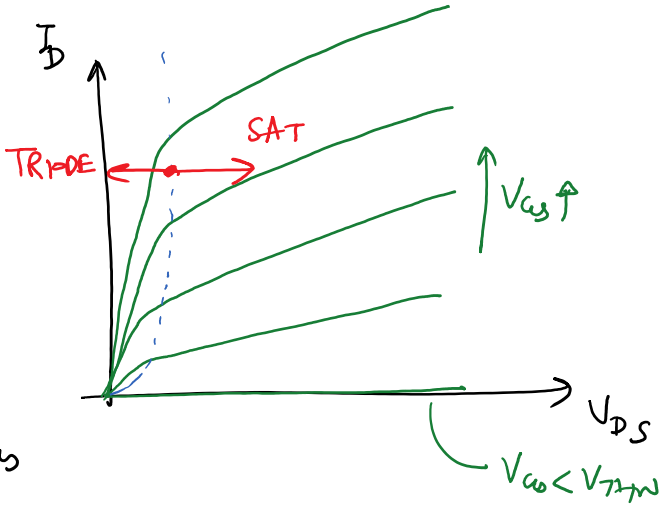
Wednesday, February 20, 2019 8:04 AM



NMOS

$$I_D = f(V_{GS}, V_{DS}, V_{SB})$$





* NMOS is in Saturation $V_{DS} > \underbrace{V_{DS,sat}}_{= V_{GS} - V_{TH,N}}$

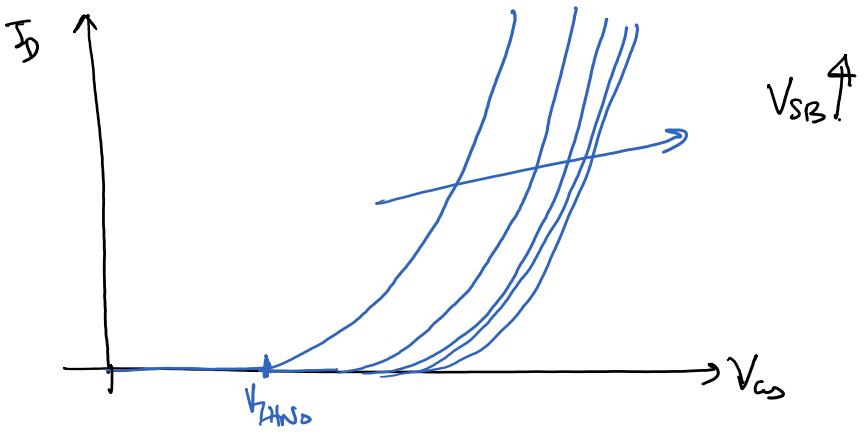
Body-effect: $V_{TH,N} = V_{TH,N0} + \gamma \cdot f(V_{SB})$

$f(V_{SB}) = \left(\sqrt{V_{SB} + |2V_{fp}|} - \sqrt{2V_{fp}}\right)$

V_{SB} ↑ $\Rightarrow$ $V_{TH,N}$ ↑

SAT: $I_{D_{SAT}} = \frac{1}{2} k_{Pn} \frac{W}{L} (V_{GS} - V_{TH,N})^2$

V_{SB} ↑ $\Rightarrow$ $V_{TH,N}$ ↑ $\Rightarrow$ $I_{D,sat}$ ↓



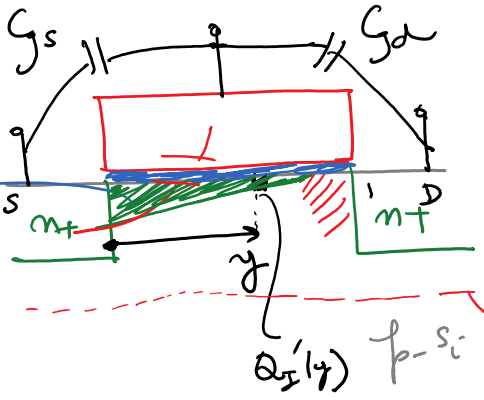
Qualitatively:

If $V_{SB} > 0 \Rightarrow$ a large voltage (V_{THN}) is needed at the gate and invert the channel

↳ V_{THN} ↑

↳ $I_{D,sat}$ ↓ ⇒ Body effect.

$V_{DS} > V_{DS,sat}$



Q_I ≡ total charge in the inversion layer

$$Q_I = W \int_0^L Q_I'(y)\,dy$$

$$= W C_{ox}' \int_0^L (V_{GS} - V(y) - V_{THN})\,dy$$

$$\vdots$$

$$Q_I = \frac{2}{3} WL C_{ox}' (V_{GS} - V_{THN})$$

$$C_{gs} = \frac{\partial Q_I}{\partial V_{GS}} = \frac{2}{3} WL C_{ox}'$$

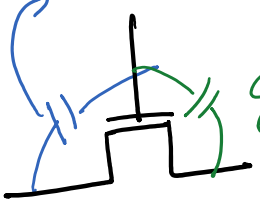
$Q = CV$

$C = \frac{\partial Q}{\partial V}$

assuming linear voltage drop of $V_{DS,sat}$ across the channel

$$\hookrightarrow C_{gs} = \frac{2}{3} C_{ox}' WL$$

$C_{gs} = \frac{2}{3} C_{ox} WL$



$C_{gd} = C_{GDO} \cdot W$

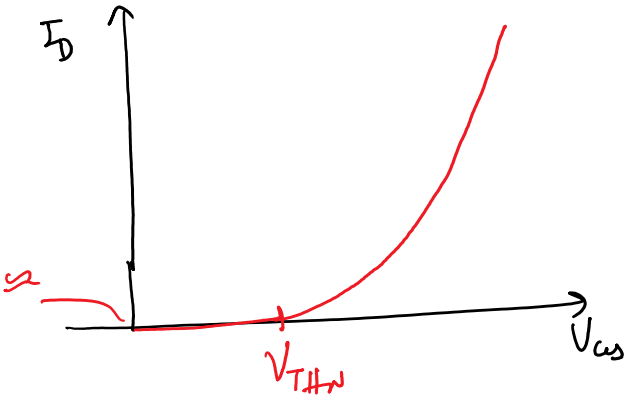
due to overlap capacitance at C_{gd}

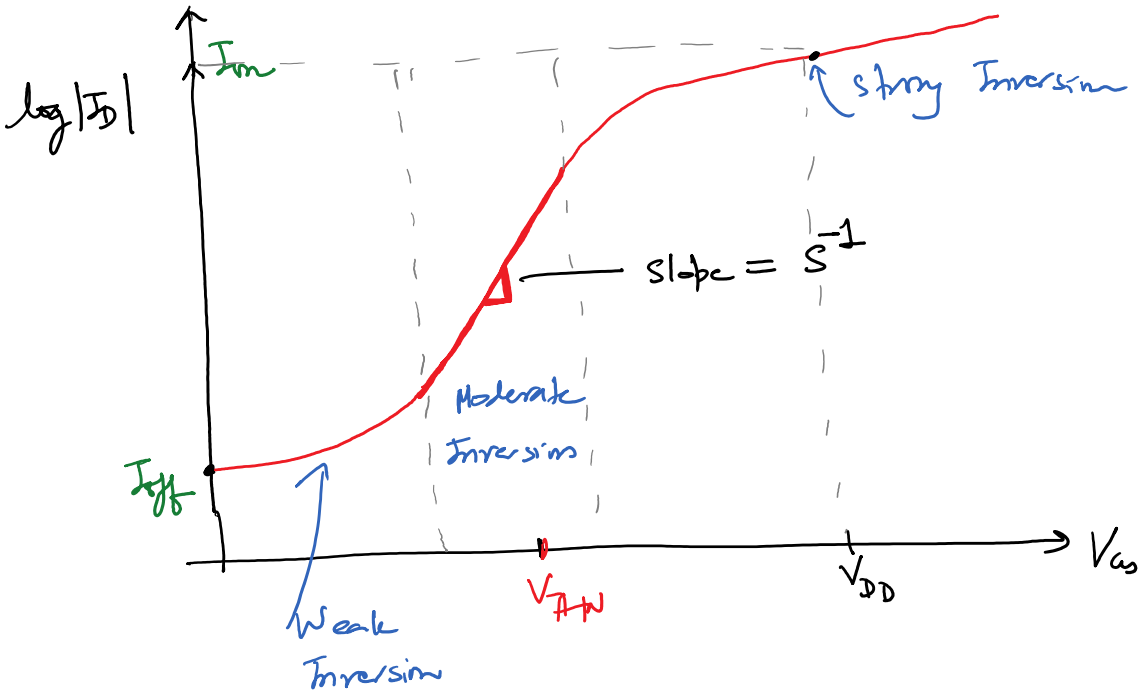
$\Rightarrow C_{gs} \gg C_{gd}$ in Saturation

Subthreshold Characteristics of MOSFETs

* So far we saw that the MOSFET starts to conduct when $V_{GS} \geq V_{THN}$

* In reality, there is a small current that flows for $V_{GS} < V_{THN}$
  - ↳ Subthreshold current. (weak inversion region of operation)





inversion

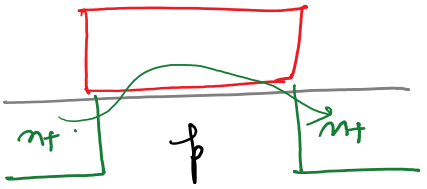
S ⇒ subthreshold slope ⇒ $\frac{mV}{\text{current change}}$

↳ inverse of the slope seen in the $\log|I_D|$ vs V_{GS} plot.

⇒ for $V_{GS} < V_{THN}$ ⇒ no channel ⇒ current is not due to drift.

↳ Subthreshold current is due to diffusion

↳ same mechanism as in the BJTs.



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* In weak inversion, electrons diffuse from source to drain through the body

↳ diffusion current in SubVT

Subthreshold.

* In subthreshold, the drain current assuming V_{DS} is small

$$I_D = I_{D0}\frac{W}{L}\cdot e^{\frac{(V_{GS}-V_{THN})}{nV_T}}\left(1-e^{-V_{DS}/V_T}\right) \qquad \left(V_T = \frac{kT}{q}\right)$$

n ⇒ slope parameter

$$\Rightarrow \log(I_D) = \log\left(\frac{W}{L}\right) + \log\left(I_{D0}\right) + \left(\frac{V_{GS}-V_{THN}}{nV_T}\right)\cdot \log_{10} e$$

$$\Rightarrow \log(I_D) = \log\left(\frac{W}{L}\right) + \log(I_{D0}) - \left(\frac{V_{THN}}{nV_T}\right) + \left(\frac{\log_{10} e}{nV_T}\right) V_{GS}$$

$$= \log\left(\frac{W}{L}\right) + \log(I_{D0}) - \frac{V_{THN}}{nV_T}\log_{10} e + \left(\frac{\log_{10} e}{nV_T}\right) V_{GS}$$

$$\frac{\partial \log(I_D)}{\partial V_{GS}} = \frac{\log_{10} e}{nV_T} \equiv S^{-1}$$

$$\Rightarrow S = \left[\frac{\partial \log(I_D)}{\partial V_{GS}}\right]^{-1} = \frac{nV_T}{\log_{10} e} = nV_T \cdot \ln(10)$$

$$\boxed{S = nV_T \ln(10)}$$

→ slope parameter depends upon the device design: doping, physical geometry, type of device

$\cdot V_T = 26mV$

Let $n = 1$

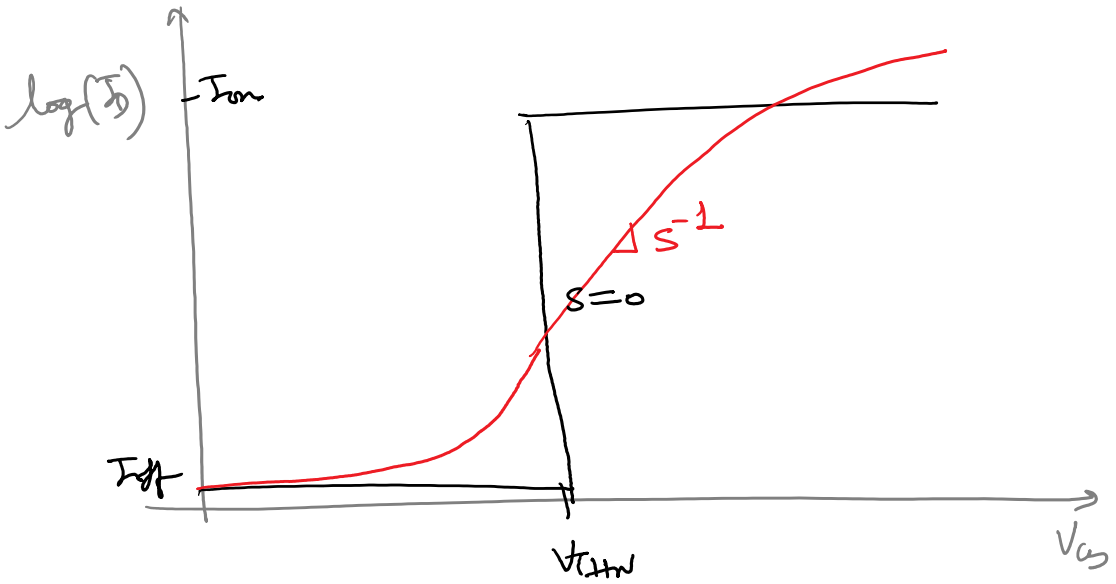
$$\Rightarrow S = 26mV \times 1 \times \ln(10) \simeq 60\frac{mV}{decade}$$

for $n = 1.6 \Rightarrow S = 100\frac{mV}{decade}$

* 'S' indicates by how much the gate voltage must drop to decrease the leakage current by an order of

magnitude (10x)

↳ we desire a smaller value for "S"



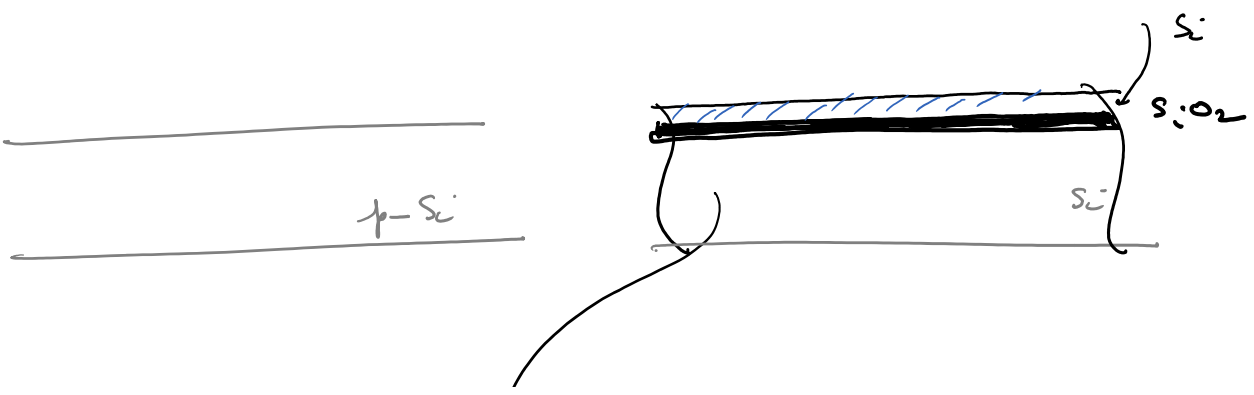
* We want a high S^{-1} value ⇒ a small value for S

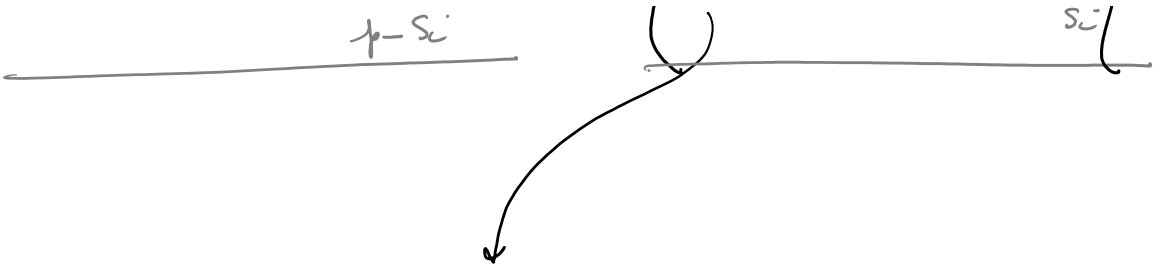
In Bulk CMOS ⇒ $S \simeq 60 \frac{mV}{decade}$

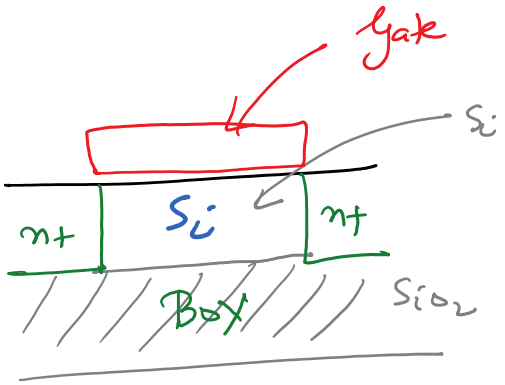
↓

SOI CMOS

↳ Silicon on insulator



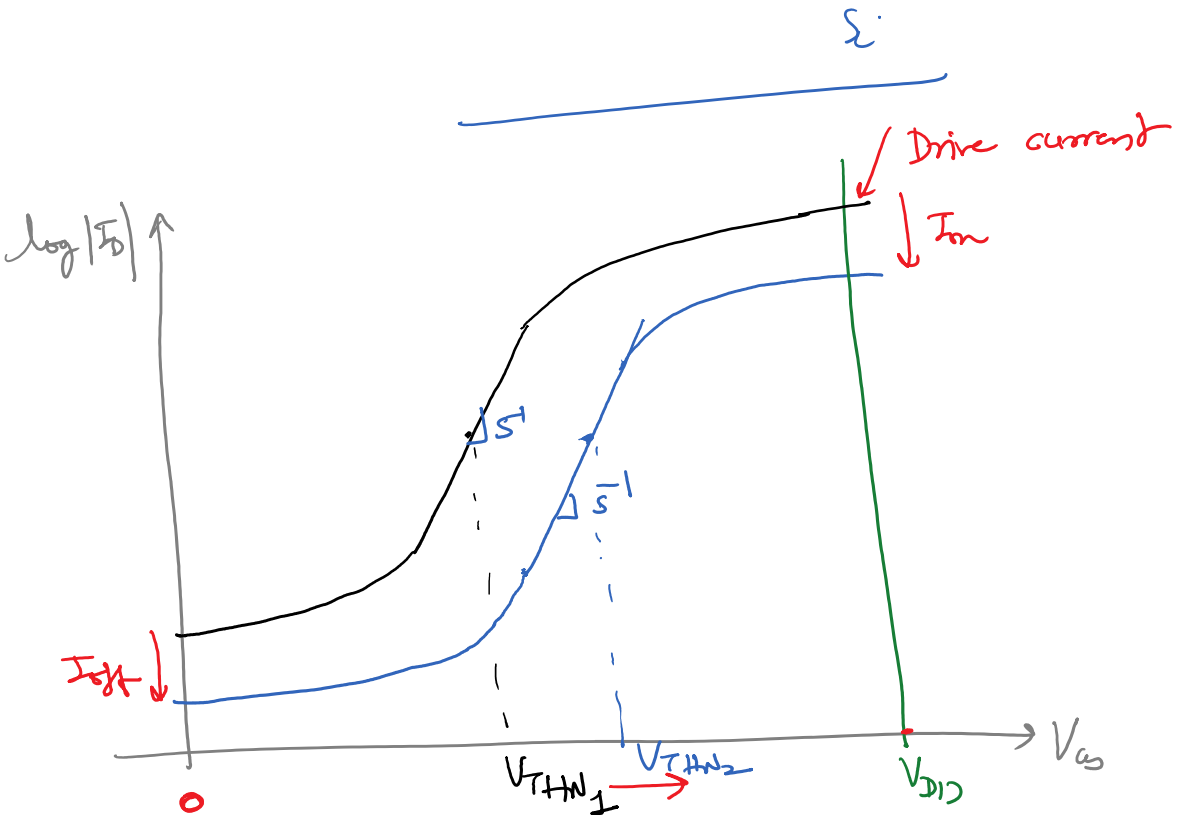




SOI- NMOS

↓

S ⇒ 40mV / decade



⇒ Can trade off leakage current with the drive current (or speed)

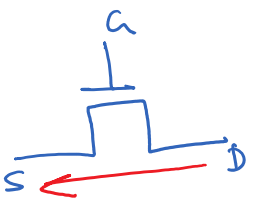
Assortment of transistors

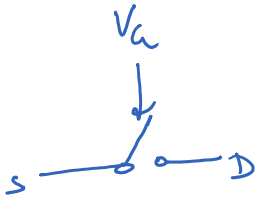
↳ nfet

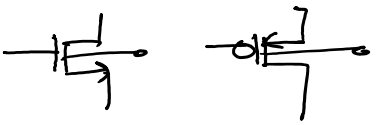
hvt_nfet ← high V_{THN}

lvt_nfet ← low V_{THN}

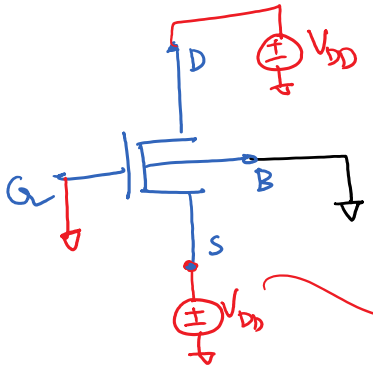
zvt_nfet ← zero V_{THN}







* Design a switch with low leakage current (I_{off})



use body effect

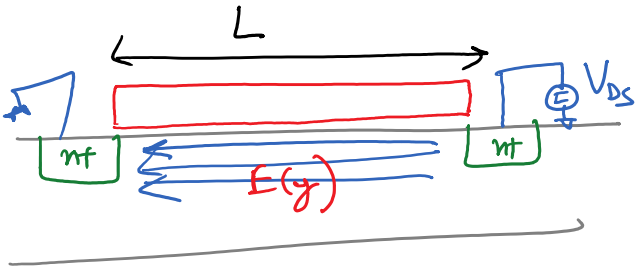
$V_{SB} > 0$

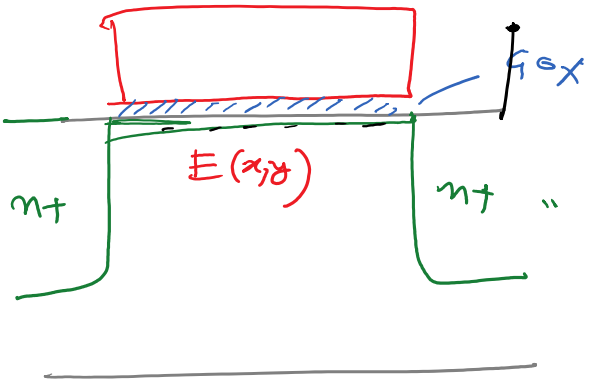
$V_{SB} = V_{DD} \Rightarrow V_{TH} \uparrow$

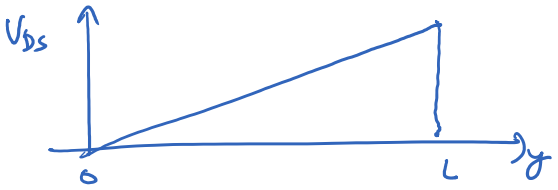
Short-Channel Effects

$L < 1\mu m$

* when the channel length (L) becomes the same order of magnitude as the source/drain depth, the electric field in the device is no longer 1D. ⇒ rather 2D







* Drain also participates in channel's electric behavior to a larger extent.

V_{DS} ⇒ impacts V_{THN}

↳ DIBL ⇒ Drain induced Barrier Lowering

* DIBL ⇐ $V_{THN}\downarrow$ as $V_{DS}\uparrow$
* GIDL ⇐ Gate induced drain leakage (DRAM)
* hot carriers