ECE 445 Intro to VLSI Design
Sample Midterm 2
Apr 8, 2019 **Name:** Key.

Closed Book, Closed Notes, Closed Computer.
Show your steps clearly to get credit.
State clearly any assumptions made.
This exam has 6 questions, for a total of 100 points.

Unless otherwise indicated use the following device parameters for the C5 process for hand calculations:

Parameter	Value
Scale factor (λ)	$0.3\,\mu m$
V_{DD}	5 V
C'_{ox}	$2.8\frac{fF}{\mu m^2}$
V_{THN}	0.8 V
V_{THP}	0.9 V
KP_n	$115\ \frac{\mu A}{V^2}$
KP_p	$60\ \frac{\mu A}{V^2}$

C5 ⇒ 0-5

Long Channel MOSFET equations:

$$V_{THN} = V_{THN0} + \gamma(\sqrt{|2V_{fp}| + V_{SB}} - \sqrt{|2V_{fp}|})$$

$$I_D = \begin{cases} KP_n \frac{W}{L}\left((V_{GS} - V_{THN})\,V_{DS} - \frac{V_{DS}^2}{2}\right), & V_{DS} < V_{GS} - V_{THN} \\ \frac{1}{2}KP_n \frac{W}{L}\left(V_{GS} - V_{THN}\right)^2, & V_{DS} \geq V_{GS} - V_{THN} \end{cases}, \quad V_{GS} > V_{THN}$$

Digital MOSFET Model:

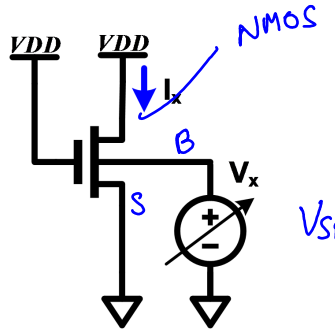
$$R'_{n,p} = \frac{V_{DD}}{\frac{1}{2}KP_{n,p}(V_{DD} - V_{THN})^2}$$
$$R_{n,p} = R'_{n,p}\frac{L}{W}$$

Logical Effort equations:

$F = GBH \triangleq H$ for an inverter chain
$\hat{f} = F^{\frac{1}{N}}$ for the least delay
$D = P + N \cdot \hat{f}$

1. (10 points) For the circuits seen below, plot the current I_x as the voltage V_x is swept from 0 to V_{DD}.

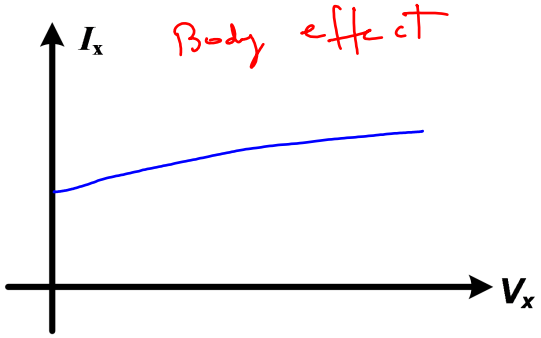
(a)



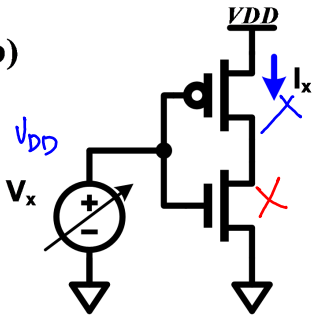
$V_x \uparrow \Rightarrow V_{SB} \downarrow$

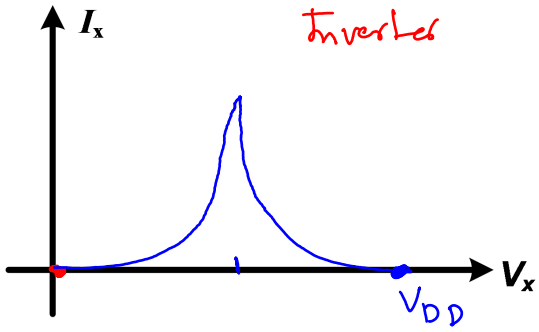
$V_{THN} \downarrow \Rightarrow I_D \uparrow$

$V_{SB} = -V_x$



(b)



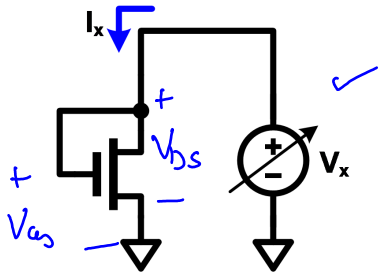


$V_{SD} = V_{DD} - V_x$

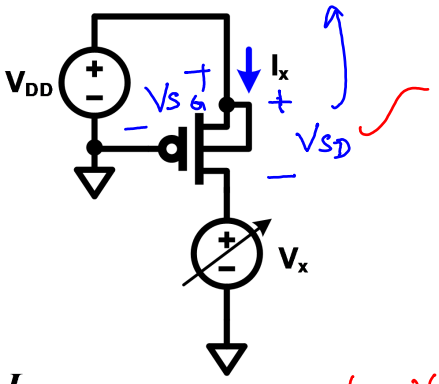
(c)

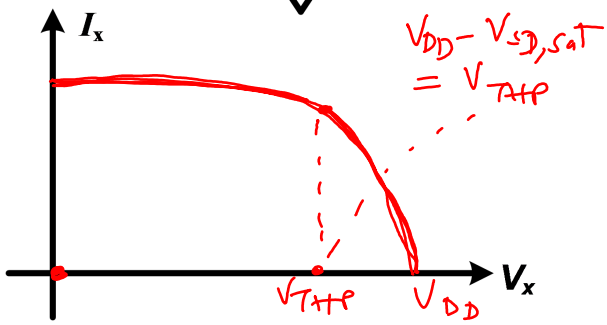
$V_{DS} = V_{GS} > V_{GS} - V_{THN}$

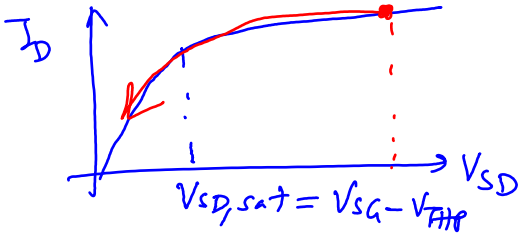
Always in SAT



(d)







2. (a) (5 points) Based on the data provided on the first page, estimate C'_{ox}, R'_n, and R'_p. *Show your work.*

$C_{ox}' = 2.8 \frac{fF}{\mu m^2}$

$R_n' = \frac{V_{DD}}{\frac{1}{2} k_{p_n} (V_{DD} - V_{THN})^2} \simeq 5k\Omega$

$R_p' \simeq 10k\Omega$

(b) (5 points) Fill the following table using the data provided on the first page.

Device	Drawn	Actual size	$R_{n,p}$	$C_{oxn,p}$
NMOS	10/2	3 μm by 0.6 μm		fF
PMOS	20/2	6 μm by 0.6 μm		fF

$R_n = R_n' \cdot \frac{L}{W} = 5k\Omega \cdot \frac{2}{10} = 1k\Omega$

$R_p = R_p' \cdot \frac{L}{W} = 10k\Omega \cdot \frac{2}{20} = 1k\Omega$

$C_{oxn} = C_{ox}'(WL)_n = 50fF$

$C_{oxp} = C_{ox}'(WL)_p = 100fF$

3. (a) (10 points) Estimate the oscillation frequency (f_{osc}) of a 21-stage ring oscillator designed using 10/2 NMOS and 20/2 PMOS devices.

$$f_{osc} = \frac{1}{n \times (t_{pHL} + t_{pLH})} = \frac{1}{n \times 0.7 (R_p + R_n) C_{tot}}$$

$$= 91.74 \text{ MHz}$$

$$C_{tot} \rightarrow \frac{5}{2}(C_{oxn} + C_{oxp}) = 375 \text{ fF}$$

(b) (5 points) Calculate the total dynamic power dissipated in the oscillator?

$$P_d = n \times CV^2 f$$

$$= n \times \frac{5}{2}(C_{oxn} + C_{oxp}) \cdot V_{DD}^2 \cdot f_{osc}$$

$$= 21 \times 375 \text{fF} \times 5^2 \times 91.74 \text{ MHz}$$

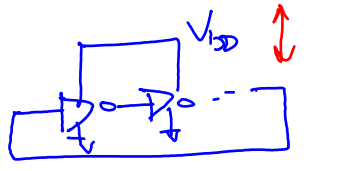
$$= 18.1 \text{ mW}$$

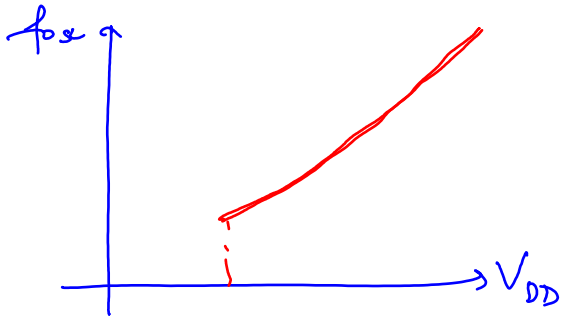
(c) (5 points) How does f_{osc} change when the supply voltage V_{DD} is varied from 0 to 5V? *Explain.*

$$f_{osc} = \frac{1}{n \times 0.7 (R_p + R_n) C_{tot}}$$

$$R_{np} = \frac{V_{DD}}{\frac{1}{2} K_{n,p} (V_{DD} - V_{TH,n,p})^2} \propto \frac{1}{V_{DD} - V_{TH}}$$

$V_{DD} \uparrow \Rightarrow R_{np} \downarrow \Rightarrow f_{osc} \uparrow$





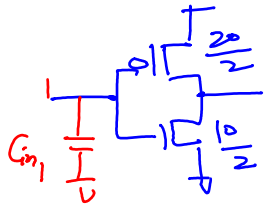
Voltage-controlled Oscillators (VCOs)

4. This problem involves the design a buffer to drive **10 pF** load with the **least delay**. Use the C5 process data from the first page, and the approximated switching model of MOSFETs with $C_{in} = C_{out} = C_{ox}$.

   (a) (5 points) Calculate the input capacitance (C_{in1}) and the time-constant (τ) of a unit inverter (size 20/10).

$C_{in_1} = C_{oxn} + C_{oxp} = 3\,C_{oxn} = 150\,ff$

$\tau_{inv} = 3RC \Rightarrow 3R_n C_{oxn} = 3 \times 1k\Omega \times 50ff$
$= 150\,ps$



unit inverter

20/2 PMOS
10/1 NMOS

   (b) (10 points) Calculate the path effort (F) for a load of 10 pF, and find the number of stages in the buffer for least delay.

Path effort

$F = G \cdot B \cdot H \equiv H = \frac{C_L}{C_{in_1}} = \frac{10pf}{150ff} = 66.67.$

($G = 1$, $B = 1$)

round off

$\hat{N} = \log_4(F) = \frac{\log(F)}{\log(4)} = 3.03 \longrightarrow 3$ stages

Revise $\hat{f} = F^{1/\hat{N}} = (66.67)^{1/3} = 4.055$ ← slightly off from $\hat{f} = 4$.

$\hat{f}$: Stage effort

(c) (5 points) What is the normalized buffer delay (D)? What is the absolute buffer delay (t_d)?

$D = P + N\hat{f}$

$= N + N\hat{f}$

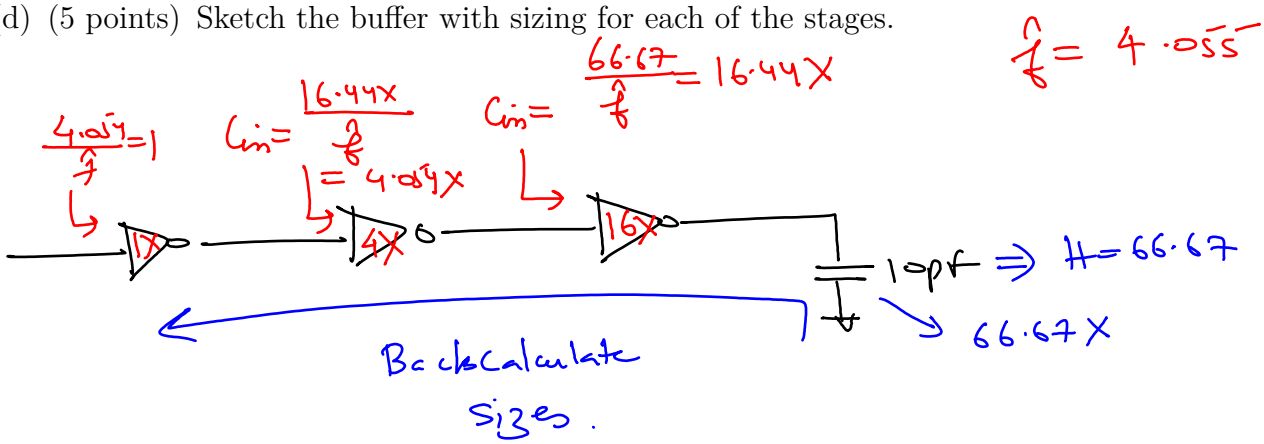
$= 3 + 3 \times 4.05$

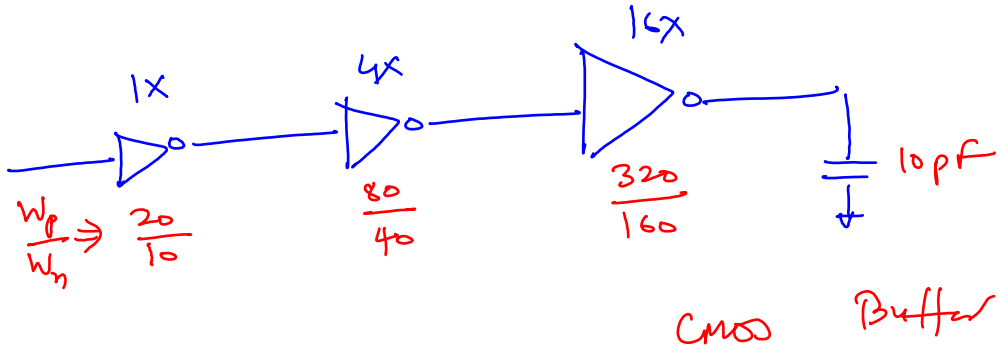
$D = \boxed{15.313}$ normalized delay

$t_d = 0.7\,\tau_{INV} \times D = \boxed{1.585\,ns}$

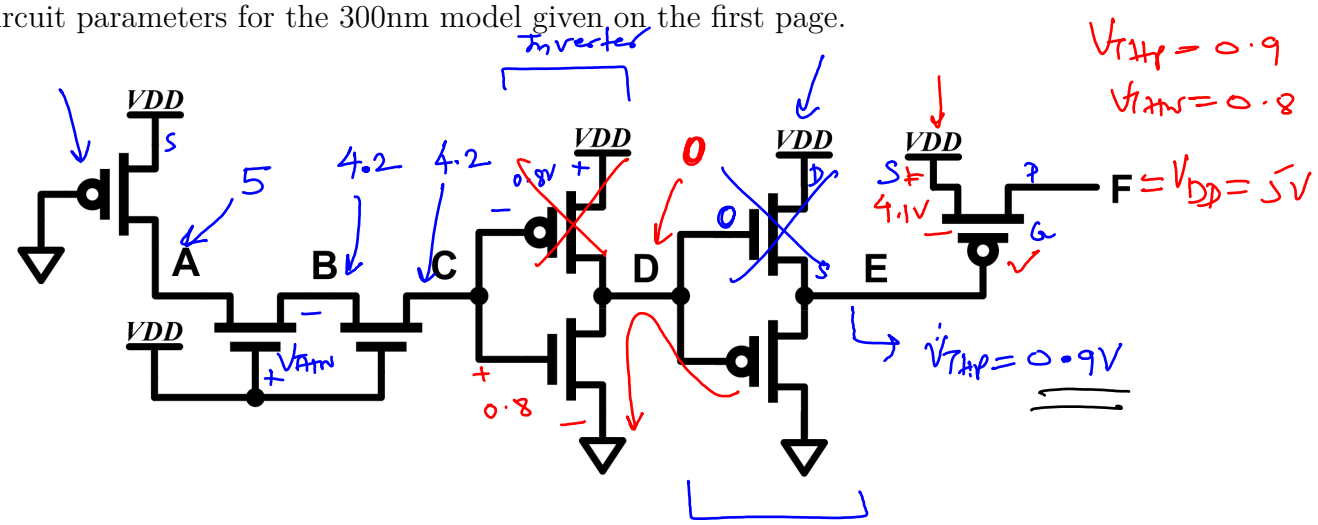
f of 4 gives best delay

(d) (5 points) Sketch the buffer with sizing for each of the stages.

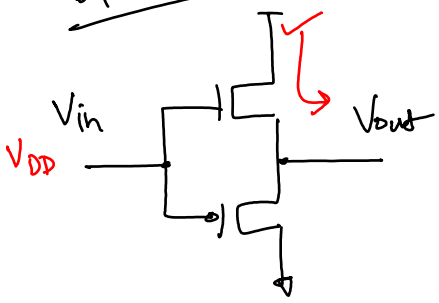


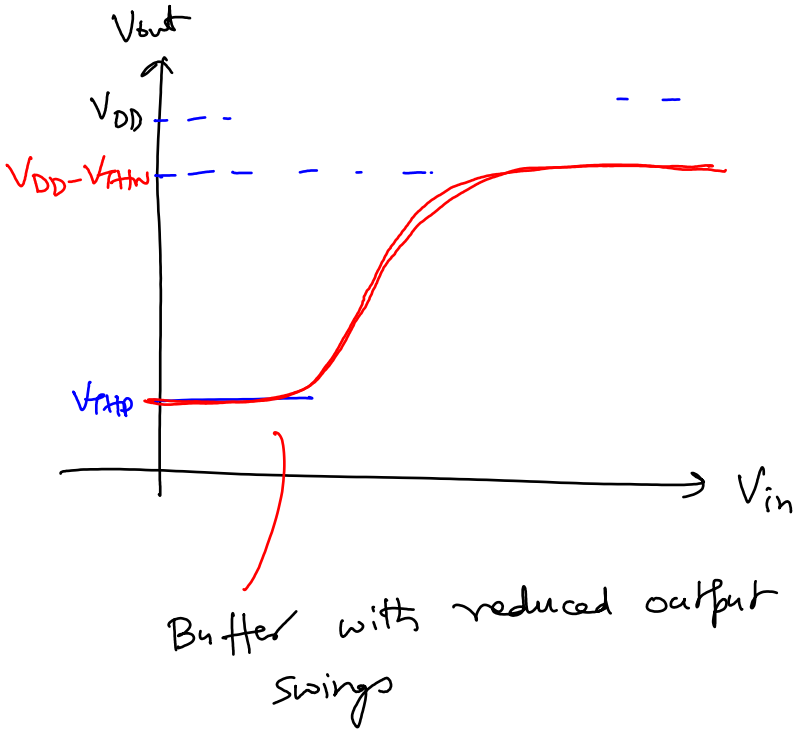


5. (15 points) Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the circuit parameters for the 300nm model given on the first page.

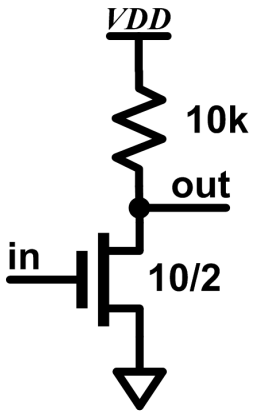


Pass gates ASIDE



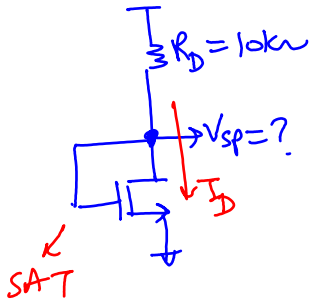


6. Consider the NMOS-only inverter shown below. Use the square-law equations and C5 process data from page 1. *Show steps for partial credit.*



(a) (5 points) Calculate inverter switching point V_{sp}.

$x \Rightarrow V_{sp}$



$$I_D = \frac{V_{DD} - V_{sp}}{R_D} = \frac{1}{2} k_n \frac{W}{L} (V_{sp} - V_{TH})^2$$

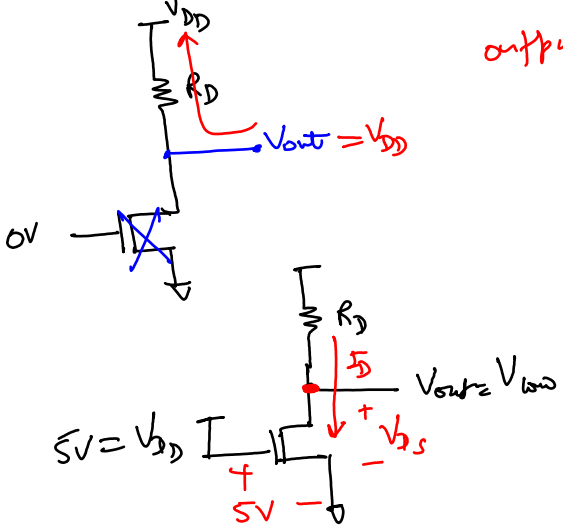
$$\Rightarrow \quad 5 - x = \frac{1}{2} \times 115 \times 10^{-6} \times 10^4 \times \left(\frac{10}{2}\right) (x - 0.8)^2$$

$$\Rightarrow \quad 2.875x^2 - 3.6x - 3.16 = 0$$

$$V_p = x = 1.8472 \text{ V}, \quad -0.595 \text{ V}$$

$$\boxed{V_{sp} = 1.8472 \text{ V}}$$

(b) (5 points) Find the voltage levels for output logic high (V_{high}) and low (V_{low}).



output

$V_{high} = V_{DD}$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = k_n \frac{W}{L} \left[(V_{DD} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$x \Rightarrow V_{DS}$

$$\Rightarrow \quad 5 - x = 5.75 \left[4.2x - \frac{x^2}{2} \right]$$

$$\Rightarrow \quad 2.875x^2 - 25.15x + 5 = 0$$

$$\Rightarrow \quad x = 8.543, \quad 0.2035$$

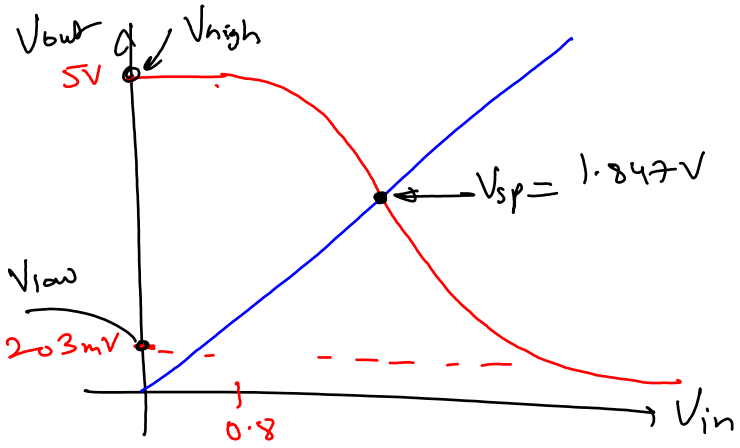
Triode

$V_{DS} < V_{DS,sat} = 4.1 \text{ V}$

$V_{low} = 0.203$ or 203 mV

Static current flows from V_{DD}.

(c) (5 points) Plot the voltage transfer curve (VTC) for the inverter and **clearly** label V_{sp}, V_{high} and V_{low} values on the curve.

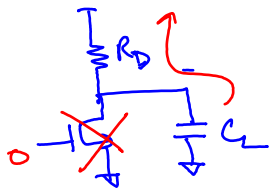


(d) (5 points) Estimate the delays t_{pLH} and t_{pHL} for the inverter driving a 100 fF load.

$t_{pLH} = 0.7\, R_D\, [C_L + C_{out}]$

$= 0.7 \times 1k\Omega \cdot [100f + 50fF]$

$\simeq 1ns$

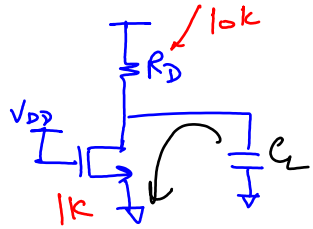


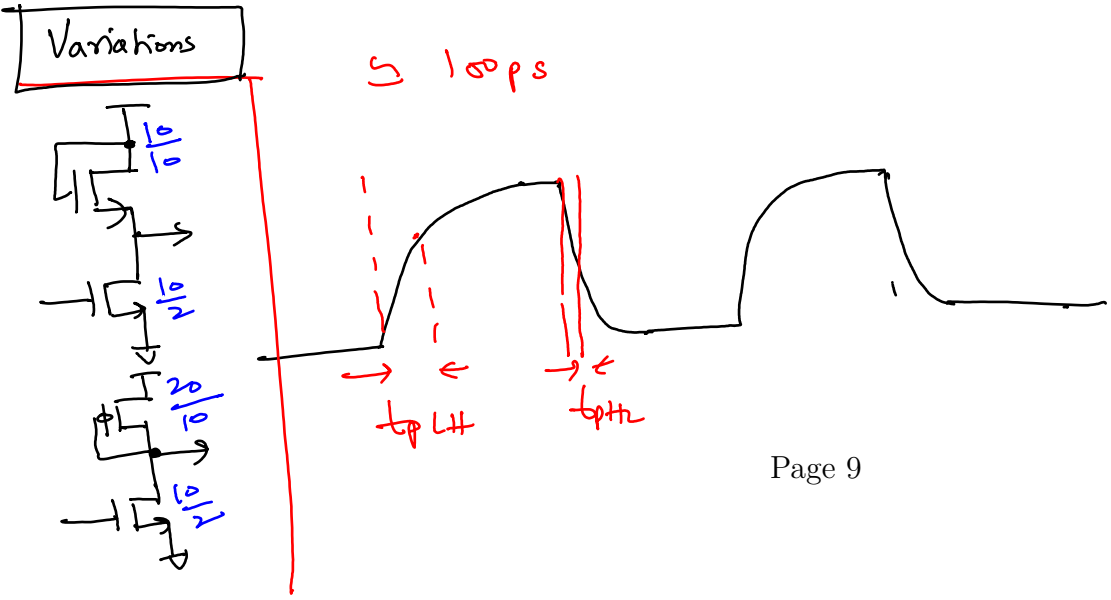
$t_{pHL} = 0.7\,(R_D \| R_n)(C_L + C_{out})$

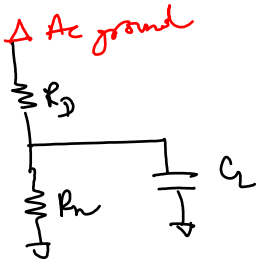
$\simeq 0.7\, R_n (C_L + C_{out})$

$= 0.7 \times 1k\,(100f + 50f)$

$\simeq 100ps$







$\tau = (R_D \| R_n) C_L$

$R_n = 1k\Omega$

$R_D = 10k\Omega$

$R_n \| R_D \simeq R$