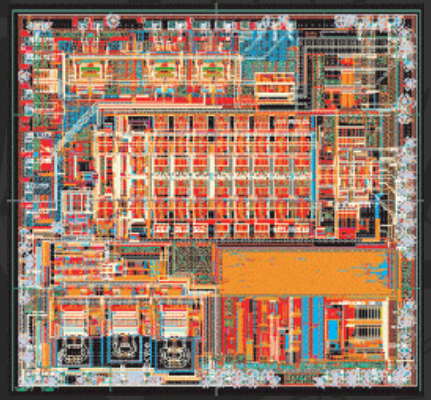
ECE 445 INTRO TO VLSI DESIGN

COURSE INTRODUCTION



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College of Engineering

COURSE OUTLINE

Instructor : Dr. Vishal Saxena

Office BEL 318

Email: vsaxena AT uidaho DOT edu

Time : MWF, 8:00-9:20 AM

Course dates : Jan 9 – May 3, 2019

Location : JEB 021

Office Hours : MW 11:30AM -12:30 PM (or by appointment)

Website : http://lumerink.com/courses/ece445/s19/ECE445.htm

COURSE OBJECTIVES

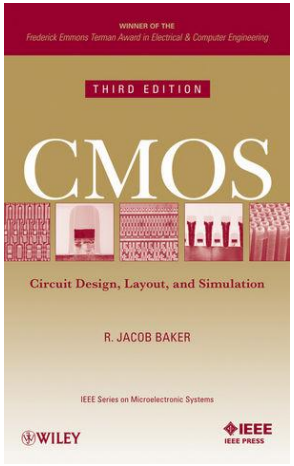
- This course focuses on design of CMOS very large scale integrated (VLSI) circuits and their applications.
- At the end of the course, it is expected that you will be able to design, analyze, layout, and simulate custom integrated circuits using CAD tools.

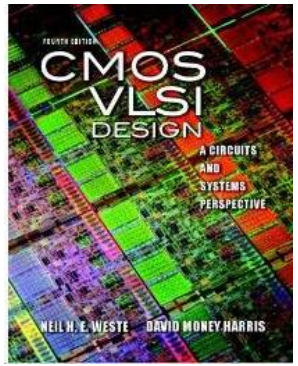
COURSE TOPICS

- An introduction to CMOS IC design, layout, and simulation
- MOSFET operation and parasitics
- Digital design fundamentals
- Digital logic design and analysis
  - Logic sequencing
  - Custom circuits: Charge pumps
- Extensive amount of circuit design, layout and simulation in Cadence design environment
- Pre-requisite
  - Brush-up concepts from ECE 310 (Microelectronics)

TEXTBOOK

- CMOS Circuit Design, Layout and Simulation – R. J. Baker, 3rd Ed., Wiley-IEEE, 2010.
  - Circuit design and simulation examples and tutorials from the book site. (http://cmosedu.com)
  - Book cadence examples available on the server.
- CMOS VLSI Design: A Circuits and Systems Perspective, N. Weste and D. Harris, 4th Ed., Addison-Wesley, 2010.
  - Used for advanced topics in digital logic and sequencing towards the end of the course.
- For handouts see course page.





COURSE PEDAGOGY AND GRADING

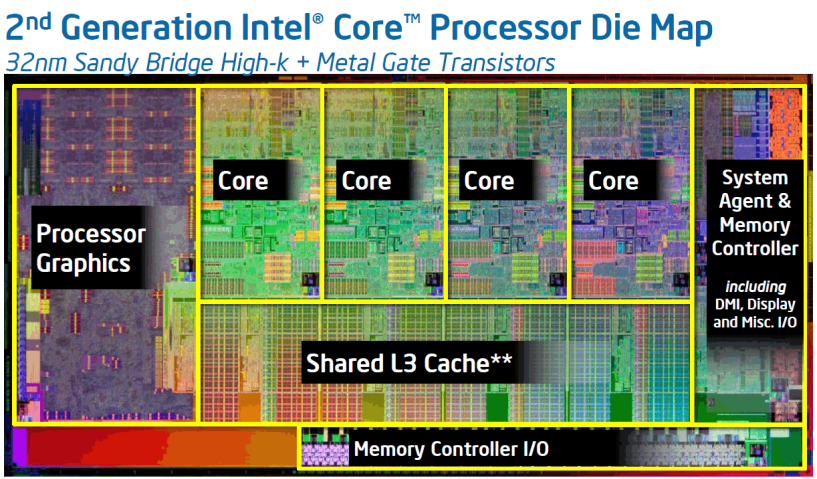
- Combination of lecture notes and slides
  - Lecture notes/slides will be posted online at the end of the week
    - Take your own notes in class instead of listening passively

- Workload (Grading)
  - 20% Midterm Exam 1
  - 20% Midterm Exam 2
  - 20% Homeworks
  - 20% Project
  - 20% Final Exam

COURSE POLICIES

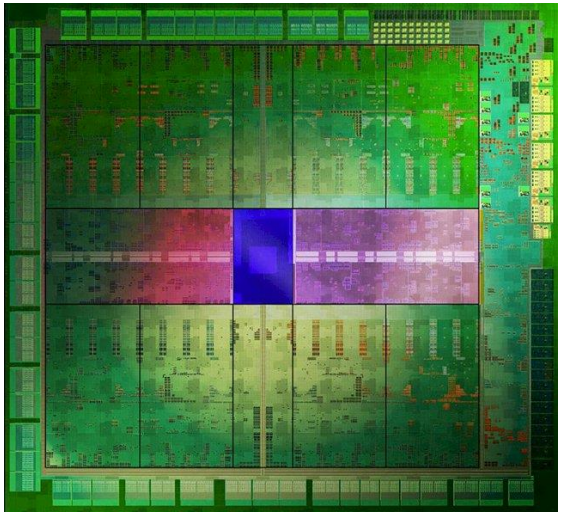
- Late work is highly discouraged (see policy on the course page)
- All assigned work is due at the beginning of class on due date
- Verify your HW answers with the posted solutions to understand the material.
- Come prepared for the Sample Exam study sessions.
- Final exam will not be returned at the end of the semester
- Avoid internet surfing in class on any device
- Plagiarism and outsourcing of work is not acceptable
  - Detailed policies are available in the Syllabus on the course site.

DIGITAL VLSICS IN ACTION



Intel Quad-core Processor

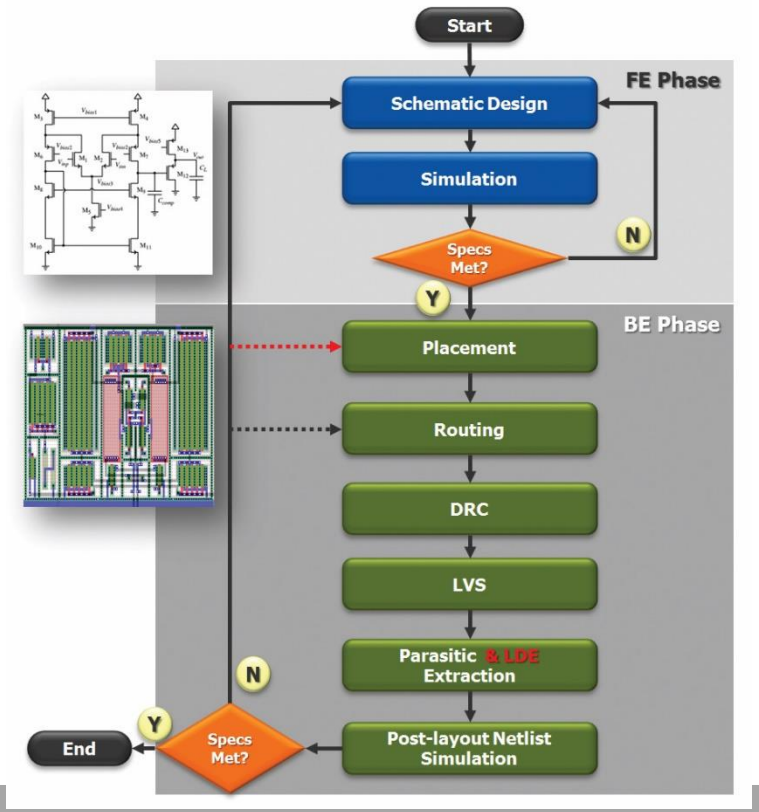
https://www.notebookcheck.net/Review-Intel-HD-Graphics-3000-graphics-solution.43710.0.html



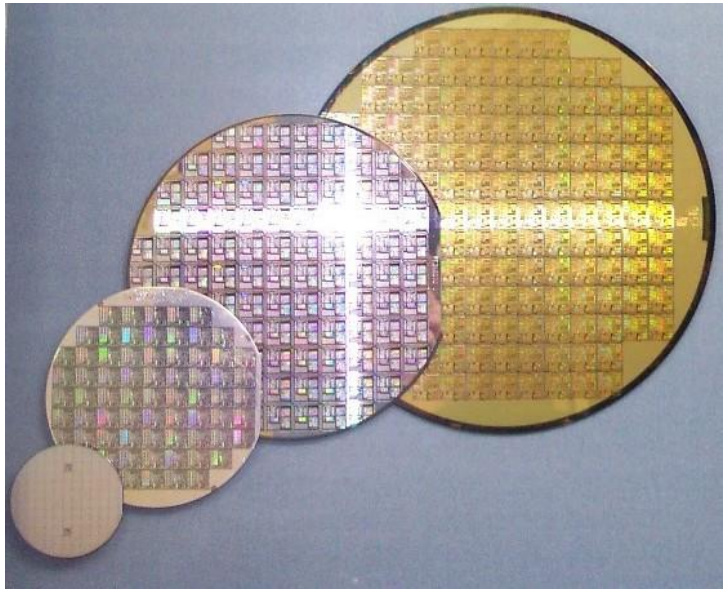
Nvidia "Kepler1" GK104 GPU

https://www.theregister.co.uk/2012/05/18/inside_nvidia_kepler2_gk110_gpu_tesla/

CUSTOM IC DESIGN FLOW

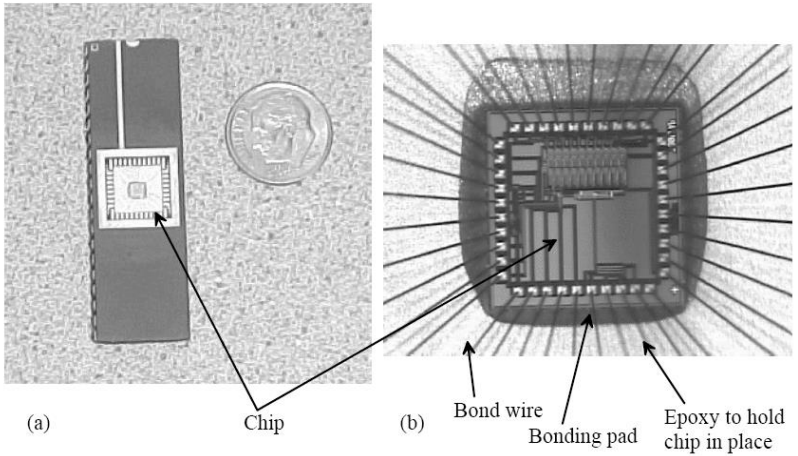


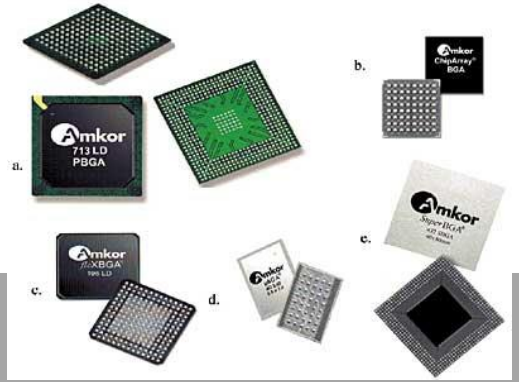
STANDARD WAFER SIZES

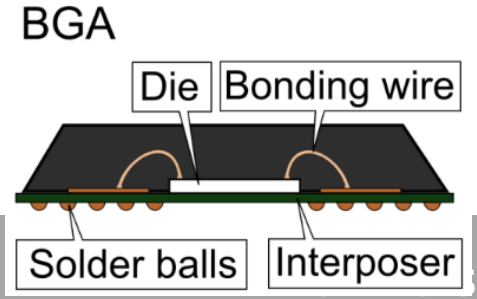


- 1 inch.
- 2 inch (50.8 mm). Thickness 275 µm.
- 3 inch (76.2 mm). Thickness 375 µm.
- 4 inch (100 mm). Thickness 525 µm.
- 5 inch (127 mm) or 125 mm (4.9 inch). Thickness 625 µm.
- 150 mm (5.9 inch, usually referred to as "6 inch"). Thickness 675 µm.
- 200 mm (7.9 inch, usually referred to as "8 inch"). Thickness 725 µm.
- 300 mm (11.8 inch, usually referred to as "12 inch" or "Pizza size" wafer). Thickness 775 µm.
- 450 mm ("18 inch"). Thickness 925 µm

PACKAGES AND DICES







DIP PACKAGING

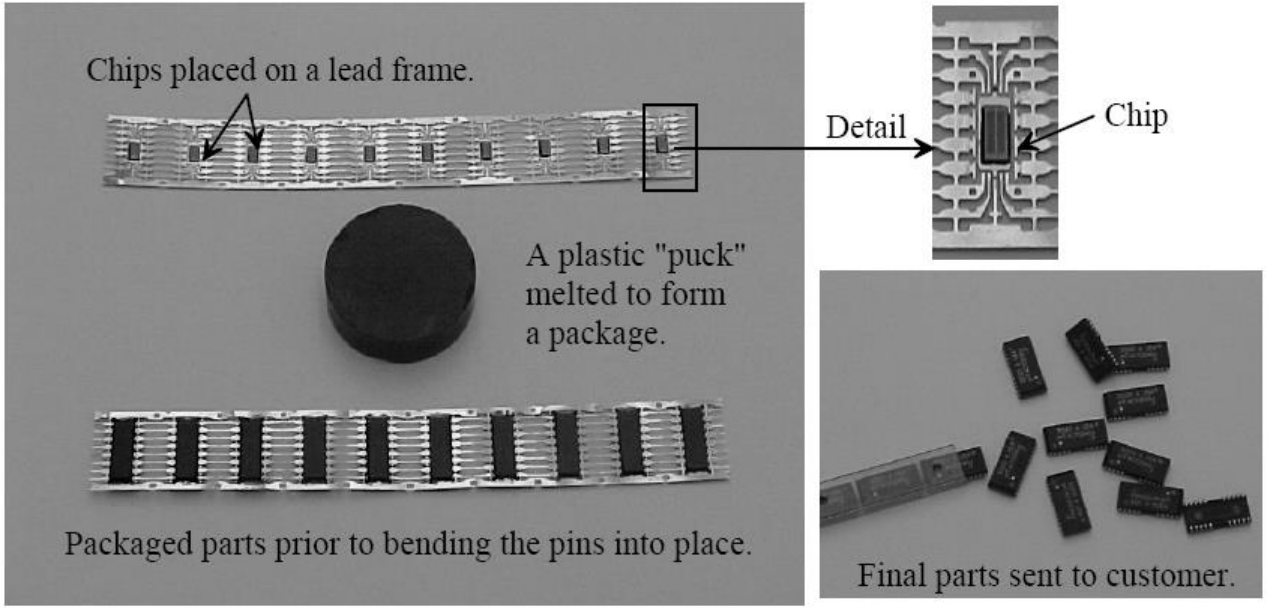
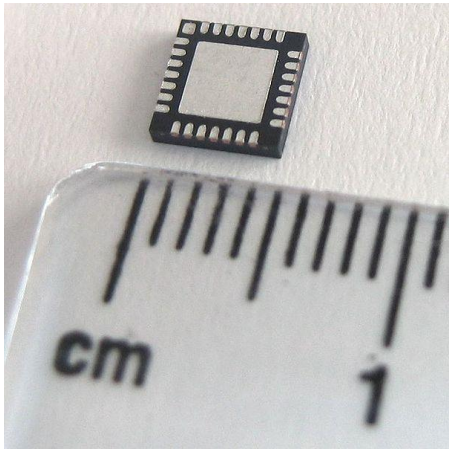


Figure 1.4 Plastic packages are used (generally) when the chip is mass produced.

RECENT PACKAGES



QFN

BGA

Refer to: http://en.wikipedia.org/wiki/Chip_package

LAYOUT AND CROSS-SECTIONAL VIEWS

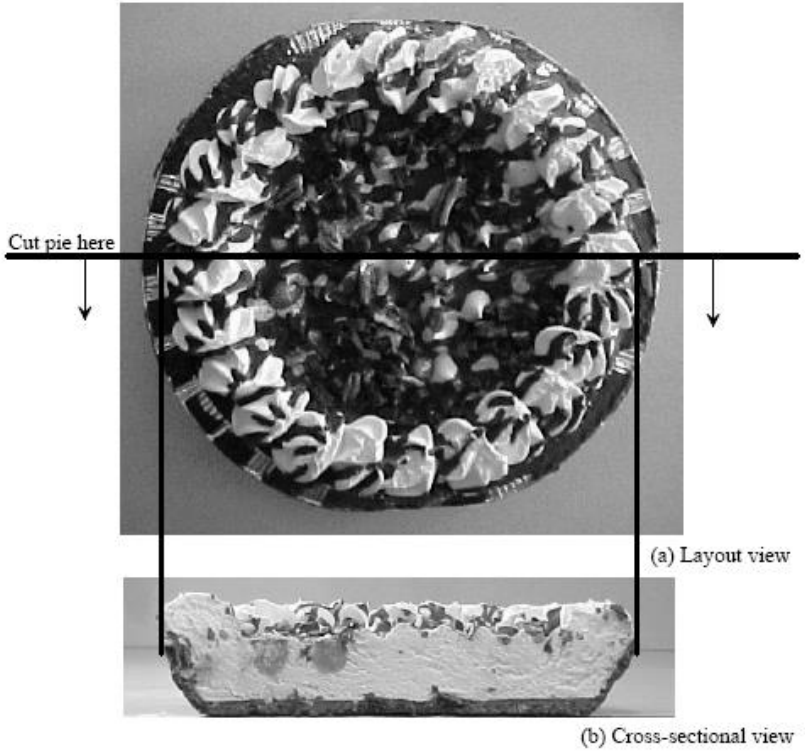
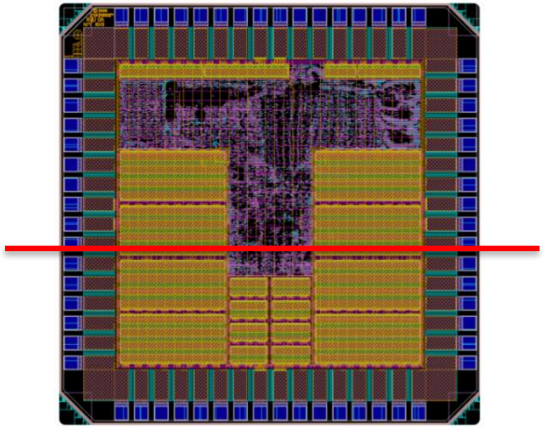
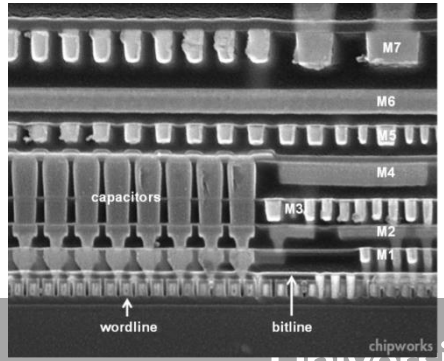


Figure 1.5 Layout and cross sectional view of a pie (minus pie tin).





Back to the basics of IC Design.