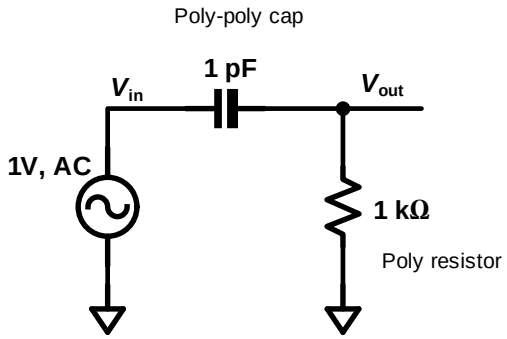
ECE 5410 Physical Integrated Circuit Design
Sample Midterm 1
Sep 25, 2010 **Name:** _____

Closed Book, Closed Notes, Closed Computer. Show your steps clearly to get credit. State clearly any assumptions made. This exam has 9 questions, for a total of 100 points.

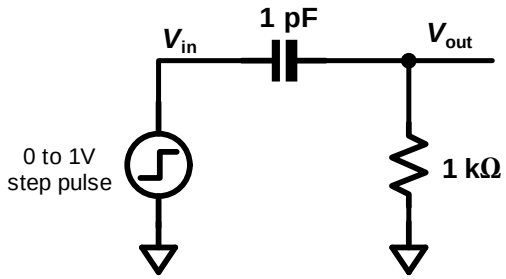
1. A C-R circuit, shown below, has been realized using a poly-poly capacitor and a poly resistor. The bottom plate of the capacitor is connected to the output and has a parasitic poly-substrate capacitance given by 20% of the poly-poly capacitor value. For this circuit



   (a) (10 points) Derive transfer function, and sketch the Bode magnitude and phase plots.

(b) (5 points) A sinusoidal input of 1V amplitude and a frequency of 100 MHz is applied to the circuit. Sketch the properly labeled time-domain input and output waveforms (v_{in} and v_{out}) in the circuit. Clearly specify the time-delay between the two signals.

(c) (5 points) Now, a unit step input is applied to the C-R circuit as shown below. What is the delay (t_d, i.e. the time taken to reach 50% of the final output) of the circuit? Sketch input and output time-domain waveforms and show t_d on the plot.



2. For a distributed RC line

   (a) (5 points) Derive the following expression for the delay

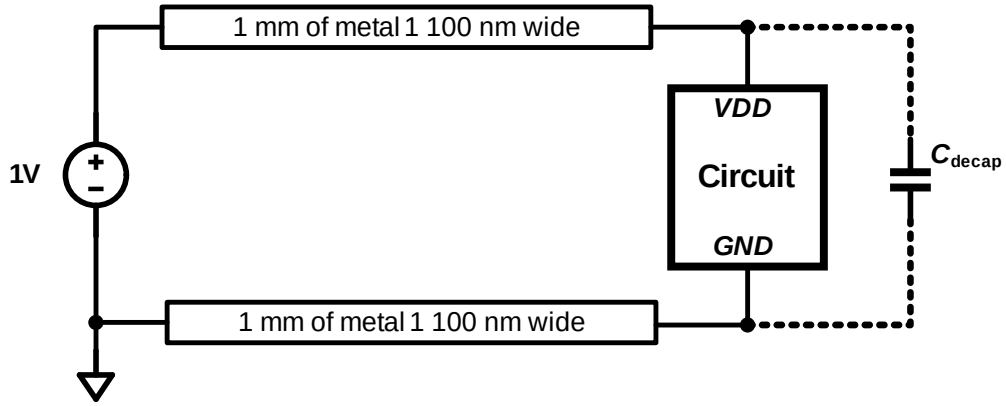
$$t_d = 0.35 R_0 C_0 l^2$$

   where R_0 and C_0 are the resistance and capacitance of a section and there are l sections in the RC line.

   (b) (5 points) Estimate and the delay through a metal wire that measures 100 nm in width and is 10 μm in length if it is periodically loaded with 100 fF every 500 nm and the sheet resistance of the metal line is $0.2\frac{\Omega}{\square}$.

3. (10 points) Show an experimental circuit to measure diode reverse recovery time. Show the waveforms associated with the circuit and explain what is happening in each region.

4. A digital circuit is wired to a 1V DC supply using metal1 ($R_{\square} = 0.1\frac{\Omega}{\square}$) wires as shown in the figure below. If the circuit pulls a current of $50\mu A$ for a pulse duration of 10 ns,



(a) (5 points) How much is the peak supply droop and ground bounce in the circuit?

(b) (5 points) Estimate the size of the decoupling capacitor required if the voltage across the circuit should not change by 10 mV during the pulse time.

5. (a) (5 points) Sketch the layout of a 100/2 NMOS device made using five 20/2 MOSFETs.

   (b) (5 points) Label the MOSFETs source and drain on your layout and which one has the largest parasitic capacitance? Explain.

6. (a) (4 points) The gate voltage of an NMOS capacitor is swept from -5V to +5V, while keepin other terminals at ground. Sketch the C-V curve and label the accumulation, depletion and inversion regions on the curve.

(b) (3 points) If the potential of the substrate isV_{fp}, in which region is the NMOS operating for the following values of the surface potential (ψ_s)

(i) $\psi_s = V_{fp}$:

(ii) $\psi_s = 0$:

(iii) $\psi_s = -V_{fp}$:

(c) (3 points) Give a definition of the threshold voltage (V_{THN}) in terms of the surface potential (ψ_s). How does the threshold voltage change with the source to bulk potential (V_{SB})?

7. Using the layout and cross-sectional views of an NMOS,

   (a) (5 points) Explain lateral diffusion (L_{diff}) and oxide encroachment (W_{enc}).

   (b) (5 points) Assuming the NMOS to be in cut-off region, what the overlap capacitances in the NMOS arising due to L_{diff} and W_{enc}?

8. (10 points) Sketch the layout and cross-sectional view of a **1 pF** poly1-poly2 capacitor in C5 process. The poly1-poly2 capacitance is 800 $\frac{aF}{\mu m^2}$. Clearly show your calculations.

9. (10 points) Draw the schematic corresponding to the following layout in C5 process and appropriately label the sizes and values of the devices. Here, the scale factor is $0.3\mu m$. The poly1-poly2 capacitance is 800 $\frac{aF}{\mu m^2}$.