Practice Problems

ECE 5410 – Integrated Circuit Physical Design

December 4, 2014

Problem 1: Problems A12.3, A13.1-2, A13.4-6 from the extra problem set available on the textbook website. **Make sure** you can estimate delays as shown in textbook examples 13.3 to 13.6.

Problem 2: Design and size the logic gates using **Static CMOS** and **Footed Dynamic (a.k.a. PE)** logic to implement the following logic functions. Make sure that the transistors are sized such that the gates have the same drive strength as the unit inverter with $W_p = 2$ and $W_n = 1$.

NAND: $Y = \overline{ABC}$ and $Y = \overline{ABCD}$

NOR: $Y = \overline{A + B + C}$ and $Y = \overline{A + B + C + D}$

XOR: $Y = A \oplus B$ and $Y = A \oplus B \oplus C$

XNOR: $Y = \overline{A \oplus B}$ and $Y = \overline{A \oplus B \oplus C}$

AOI: $Y = \overline{AB + CD}$, $Y = \overline{AB + CD + EF}$, $Y = \overline{ABC + DEF}$, $Y = \overline{A(B + C) + DE}$, $Y = \overline{A(B + C) + D(E + F)G}$, $Y = \overline{A(B + C + D) + EFG}$

Problem 3: Sketch the compact **Layout** for the following gates implemented using Static CMOS Logic:

$Y = \overline{AB}$**,** $Y = \overline{A + B}$, $Y = \overline{ABC}$, $Y = \overline{A + B + C}$, $Y = A \oplus B$, $Y = \overline{A \oplus B}$

Problem 4: Design and size the logic gates using **CVSL** Logic to implement the following logic pairs. Use minimum number of transistors in your designs.

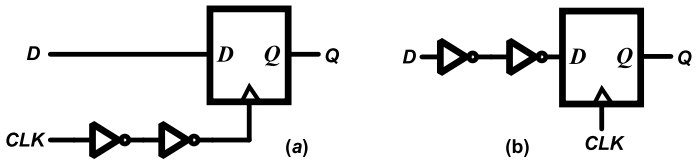
XOR3: $Y = A \oplus B \oplus C$ and $Y = \overline{A \oplus B \oplus C}$

XOR4: $Y = A \oplus B \oplus C \oplus D$ and $Y = \overline{A \oplus B \oplus C \oplus D}$

Complex Logic: $Y = \overline{AB + C(E \oplus F)}$

Problem 5: Sketch the schematics of positive and negative edge-triggered CMOS Flip-flops (FF). Explain setup and hold times in a FF. How would you estimate the t_{setup}, t_{hold} and t_{pcq} for these FFs.

What happens to t_{setup}, t_{hold}, and t_{pcq} if; (a) the clock is delayed using a two inverter buffer and (b) the data is delayed as shown in the figure below.



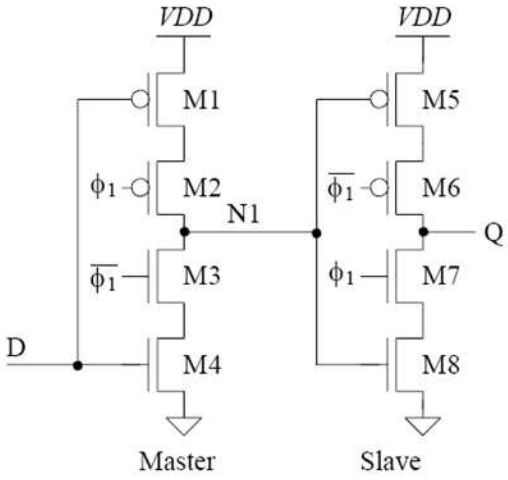
Problem 6: The logic for a Full-Adder circuit is given by

$$S = (A \oplus B) \oplus C_i$$

$$C_{out} = AB + C_i(A + B)$$

where C_i is the input carry, C_{out} is the carry output, and S is the sum. Using minimum number of transistors possible, design and size logic gates using CMOS Logic to implement the full-adder.

Problem 7: Show that the following dynamic circuit functions like a flip-flop:



Problem 8: An inverter has to be designed using an unskewed 2-input NAND gate in your design library. It can be done in two ways: (a) connect both the inputs together, or (b) connect one of the inputs to V_{DD}. Which of these two designs is faster and why?

Problem 9: Write an expression for the delay of N transmission gates (TGs) in series driving a load C_L.

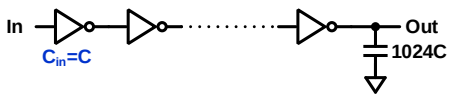
Problem 10: Draw the schematic of a non-overlapping clock generator. How will you increase the dead time between the two clock phases? Implement the non-overlapping clock generator using NOR gates instead of NAND.

Problem 11: Implement a 8X1 MUX using TGs.

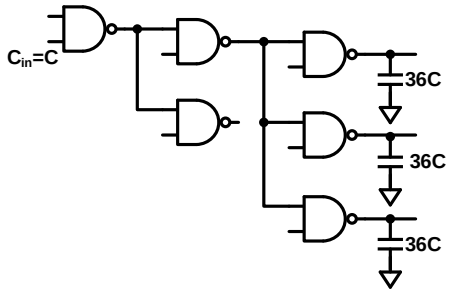
Problem 12: Find the normalized input capacitance (C_{in}), logical effort (g) and parasitic delay (p) for the static logic gates in Problem 1. Refer to the logical effort slides.

Problem 13: Logical Effort Examples

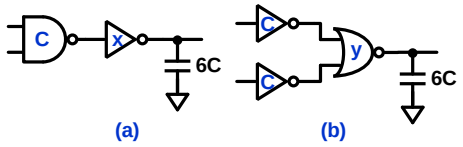
a) Determine the number of inverter stages and their sizes (drive capabilities) in the buffer chain below for minimum delay.



b) Determine the sizes (drive capabilities) of the NAND gates in the logic chain below for minimum delay.



c) Comsider the two designs of a 2-input AND gate shown below. Give an intuitive argument about which design will be better. Backup your argument with a calculation of path effort, delay, and input capacitances x and y to achieve this delay.



Problem 14: Explain metastability in latches. State at least three methods of mitigating metastability.

Problem 15:

a) Estimate delay in the following unskewed gate driving an fan-out of 4 (Fo4) inverter load: (a) 2 input NAND and NOR gates, (b) 3- input NAND and NOR gates. Assume only one input is changing at a time. State your assumptions.

b) If the arrival times of the inputs A, B, and C are given by $t_A > t_C > t_B$, then draw these gates for minimum delay.

c) Find the contamination and propagation delays for these gates with no-load condition.

Problem 16: Using the timing parameters in the Table below:

	t_{setup}	t_{pcq}	t_{ccq}	t_{hold}
Flip-flop	65 ps	50 ps	25 ps	30 ps
Inverter	x	5 ps	5 ps	x

a) Determine the maximum logic propagation delay (t_{pd}) available within a 500 ps clock cycle (2 GHz clock rate). Assume zero clock skew.

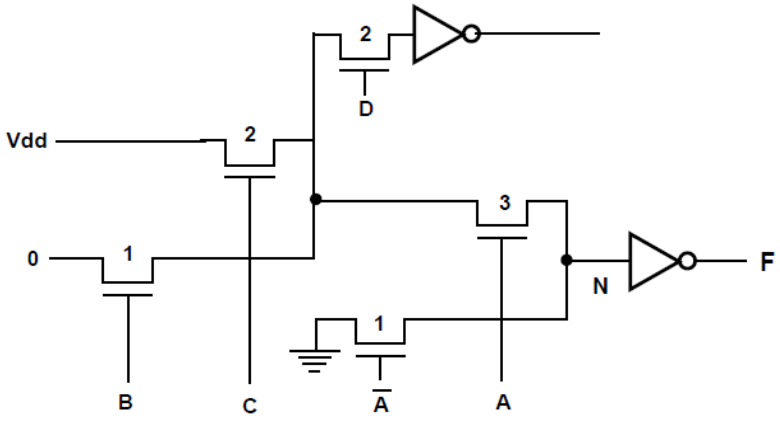
b) Determine the logic contamination delay (t_{cd}).

c) What is the maximum achievable clock rate for the logic delay of $t_{pd} = 200$ps ?

d) A clock divider requires placing flip-flops in series (Q1 feeding to D1 and so on). What errors you may face in this circuit? Redesign the circuit using inverters to mitigate the hold failure.

Advanced Problems

Problem 17: The inverters in the circuit below have minimum-sized transistors and the widths of the pass transistors are shown in the figure. Assume that the depletion/diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C. In addition, $V_{DD} = 5V$, $V_{THN} = 0.8V$ and $V_{THP} = 0.9V$. The sequence ABCD = (0011, 1001) is given as input to the circuit. Write down the voltage on node N just after the sequence is applied.



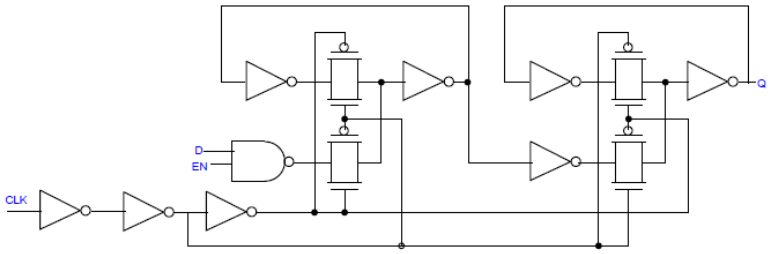
Problem 18: The components of the flip-flop below have the following rise/fall delays (in pico seconds).

Nand gate: 75/125

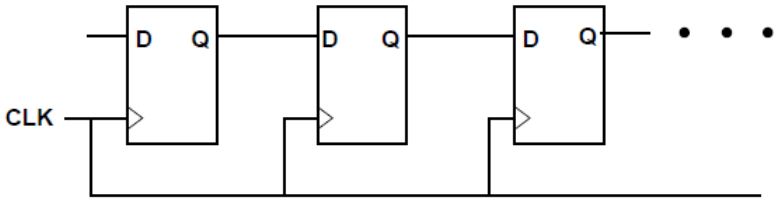
Transmission gate: 75/75

Inverter**:** 50/50

What are the flip-flop parameters t_{setup}, t_{hold}, t_{ccq} and t_{pcq} for this circuit?



Problem 19: The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay (t_{pcq}) of 150 ps, and a minimum clock-Q delay (t_{ccq}) of 100 ps.



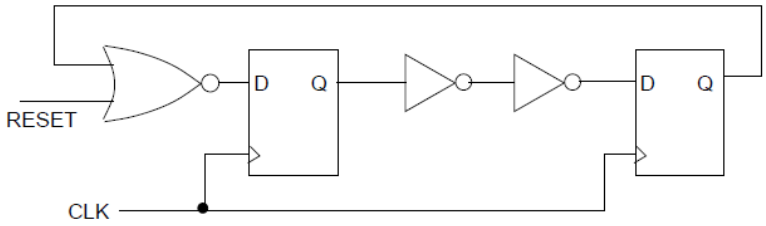
a) How fast can the circuit be clocked?
b) What is the limit on the hold time of the flops at this frequency?
c) What is the limit on the hold time of the flops at a frequency of 1 GHz?
d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Problem 20: What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.

Inverter: t_{pd} = 200 ps, t_{cd}= 100 ps

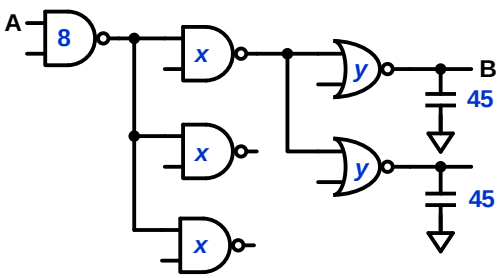
2-input NOR: t_{pd} = 200 ps, t_{cd} = 150 ps

D Flip-flop: t_{pcq} = 200 ps, t_{ccq} = 0 ps, t_{setup} = 300 ps, t_{hold} = 100 ps.

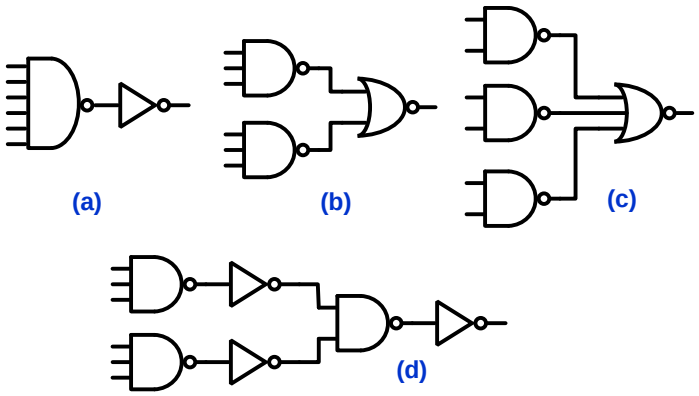


a) How fast can the circuit be clocked?
b) What is the limit on the hold time of the flops at this frequency?
c) What is the limit on the hold time of the flops at a frequency of 1 GHz?
d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Problem 21: Logical Effort- Estimate the minimum delay of the path from A to B and choose transistor sized to achieve this delay. The initial NAND2 gate presents a load of 8X transistor width on the input and the output load is equivalent to 45X of the transistor width. **Ans**: $D_{min} = 22$, $y = 15$, $x = 10$.



Problem 22: Consider four design of a 6-input AND gate shown below. Develop an expression for the delay of each path if the electrical effort is H. What design is fastest for $H = 1$? For $H = 5$? for $H = 20$? Explain your answers intuitively.



Problem 23: (a) Using logical effort show that the time-period of an N-stage ring oscillator is given by $T = 4N$, and the frequency of oscillation by $f_{osc} = \frac{1}{4N\tau_{inv}}$.

(b) Now, if the inverter is designed using NAND2 gates, find the time-period and frequency of oscillation. Here, one of the inputs of the NAND2 gate is connected to an Enable input signal.

Charge Pump Problems

Problem 24

Draw the schematic of a charge pump (showing the clocks needed) required to generate $V_{pump} \geq 4V_{DD}$ in C5 process with $V_{DD} = 5V$. Ignoring body-effect, what is the steady-state pump output voltage?

Problem 25

Draw the schematic of a charge pump (showing the clocks needed) required to generate $V_{pump} \approx -0.5V$ in C5 process. You can pick a suitable value for V_{DD}.