Homework 8

ECE 445 – Intro to VLSI Design

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the ECE servers for the homework problems.

Problem 1: Standard cell design- Use On-Semi C5 process, $V_{DD} = 5V$ and minimum lengths ($L = 2\lambda$).

a) Design and layout the following gates using CMOS static logic. Ensure that the transistors are sized such that the gates have the same drive strength as an equivalent inverter with NMOS sized $\frac{10}{2}$. Minimize layout area and parasitics by using techniques such as parallel poly gates and shared diffusion.

i) 3-input NAND: $Y = \overline{ABC}$

ii) 3-input NOR: $Y = \overline{A + B + C}$

iii) 2-input XOR: $Y = A \oplus B$

b) Compare schematic and post-layout (extracted) simulation results for a load capacitances of 100 fF, 200 fF and 1 pF. How do they compare with you hand-calculations?

(c) Find the normalized input capacitance (C_{in}), logical effort (g) and parasitic delay (p) for the above gates. Refer to the logical effort slides.

Problem 2: Logical Effort

Determine the sizes (drive capabilities) of the NAND gates in the logic chain below for minimum delay. Refer to the logical effort slides.