Homework 4

ECE 445 – Intro to VLSI Design

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.

Problem 1: Write a short note covering lateral diffusion and oxide encroachment, and all the resulting overlap capacitances. Use both layouts and cross-sectional views to help with the clarity of your tutorial.

Problem 2: Layout a poly-poly 1 pF capacitor in the C5 technology. Clearly show your capacitor size calculations and demonstrate that your layout passes DRC checks. Extract the capacitance value from your layout and ensure that it is within 1% range of the required 1 pF value. The process data can be found here.Note that in our Cadence NCSU setup, poly2 layer is designated as **elec** (i.e. top electrode). (See ECE445 Tutorial 3).

Problem 3: Create schematic and layout for the following transistors in C5 ($0.5\mu m$ CMOS) technology. Place gate (G), drain (D), source (S) and body (B) pins on the transistors using metal1 (See CMOSEdu Cadence Tutorial 2).

NMOS of size 10/2 (i.e $\frac{W}{L}=\frac{3\mu m}{0.6\mu m}$) and

PMOS of size 20/2 ($\frac{W}{L}=\frac{6\mu m}{0.6\mu m}$).

Show the **extracted layout** views for each of the transistors. No Spectre simulations are required in this problem.

Problem 4: Layout the following devices using the C5 technology, in **as square an area** as possible (remember a MOSFET has four terminals). Show that your layout passes DRC checks and also show the extraction results. (See ECE445 Tutorial 3).

1. A **100/2** PMOS. You may use the NMOS pcell (using multiplier option) to create a multi-finger layout and then connect the terminals together to form the transistor.
2. A **10/100** NMOS.