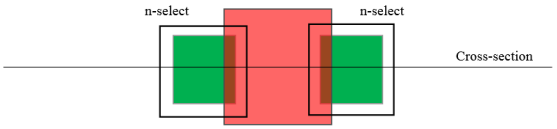
Homework 3

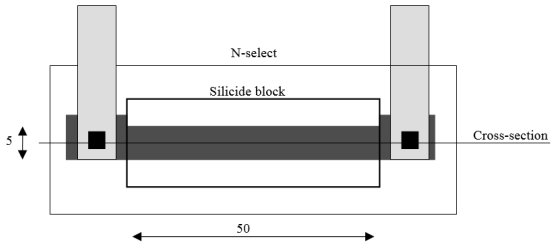
ECE 445 – Intro to VLSI Design

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.

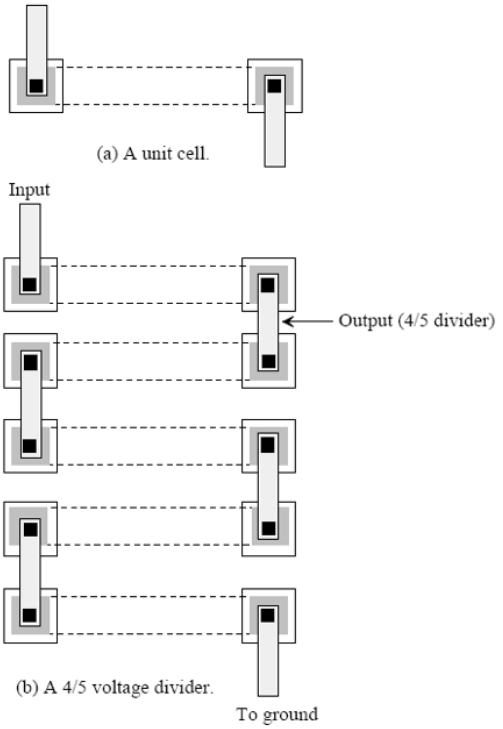
Problem 1: For the incorrect layout of a MOSFET seen below sketch the cross-sectional view along the line indicated. Make sure to clearly indicate the FOX regions. How will you fix this layout?



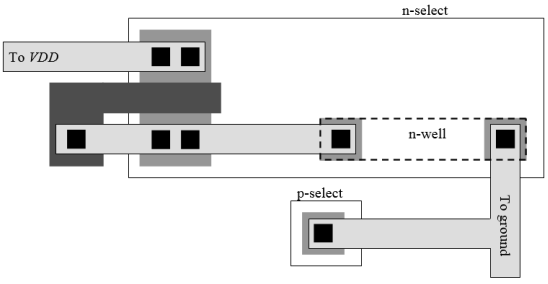
Problem 2: Using the sheet resistances seen in **Table 4.1** of the CMOS textbook, estimate the resistance seen in between the two metal1 connections. Also sketch the cross-sectional view along the line indicated.



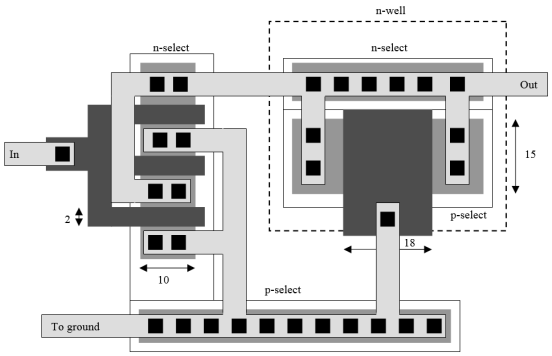
Problem 3: Cadence Layout: Using Cadence Virtuoso and On Semi C5 technology node, **lay out** a 4/5 n-well resistor divider using unit cells of 10kΩ as shown below (see CMOS textbook Figure 5.4). **Extract** your layout. Make sure your design passes **LVS** and **DRC**. You may refer to **Cadence Tutorial 1** on the course site.



Problem 4: Sketch the schematic corresponding to the layout seen below. Label all four terminals of the MOSFET in your schematic and comment on how the body of the MOSFET is tied to ground. Which terminal, of the MOSFET, would you label the drain and which would you label the source? Why?



Problem 5: Sketch the corresponding schematic for the following layout. Make sure the body connections of the MOSFETs are clearly seen in your schematic.


n-well
n-select
n-select
Out
In
15
2
p-select
18
10
p-select
To ground