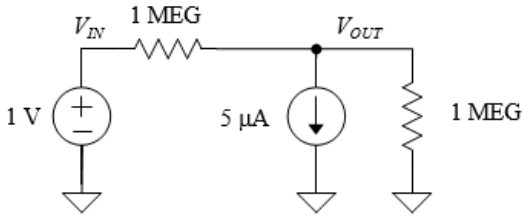
Homework 1

ECE 445 — Intro to VLSI Design

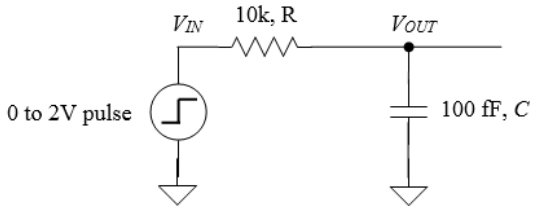
Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the servers for the homework problems.

Problem 1: Using dc operating point anaysis (.dc), simulate the operation of the circuit seen below. Compare your hand calculated values for the node voltages to the Spectre simulation results. What happens to the simulation results if we change the resistor values from 1MEG (10^6) ohms to 1M (1 milli or 10^{-3}) ohms? Note that some circuit simulators are "smart enough" to recognize that 1M is likely a megaohm resistor and therefore interpret 1M as 1MEG (but be careful!).

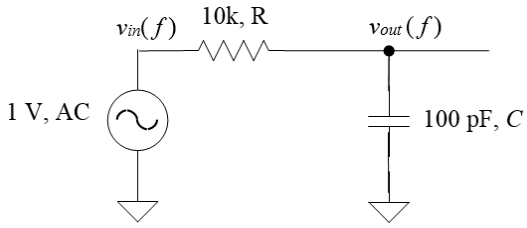


Problem 2: RC circuits:

a) Show, using equations, that the time it takes to reach 1 V (half of the input pulse amplitude) after the input pulse transitions from 0 to 2 V is given by 0.7RC. Verify this with a transient (.tran) simulation. **Hint:** Look up example schematics from the textbook that are available in your path (assuming you have correctly set up your course directory).



b) Derive transfer function of the following circuit. Using these equations sketch Bode responses (log-log plots). Use AC analysis (.ac) to verify your plots and equations.

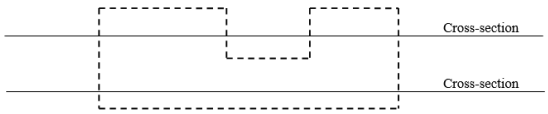


c) Suppose the input, in part (b), a 1V peak sinusoid with a frequency of 1 MHz. Sketch, by hand, the input and output waveforms in the circuit (in the time domain). Use transient

d) Repeat parts (a), (b) and (c), if the resistor and capacitor are swapped to create a C-R circuit.

Problem 3: N-well:

a) For the n-well layout seen below sketch the cross-sectional view at the places indicated. If the p-substrate is at ground potential what is the minimum value of potential allowed at any point on the n-well? Why?



b) Estimate the value of a $2\mu m \times 200\mu m$ if the n-well's sheet resistance is $1k\Omega/\square$. If the bottom zero-bias depletion capacitance of the n-well to substrate is $100aF/\mu m^2$ (a is atto or 10^{-18}), the sidewall capacitance is $50aF/\mu m$, then estimate the delay through the resistor. Use simulations to verify your estimate.

c) For the n-well in part (b), the built-in potential between it and the p-substrate is 750mV and the grading coefficient, m, is 0.3 then sketch how the capacitance between the n-well and p-substrate changes as the potential

on the n-well is increased (the p-substrate is at ground potential.)

d) As the potential of the n-well increases what happens to the depletion layer thickness between the p-substrate and the n-well? Would you expect the delay through the n-well in part (b) to be dependent on the voltage between the n-well and the p-substrate? Why?

Problem 4: Diode reverse-recovery: Sketch the output voltage in the following circuit (and estimate the storage time). Verify your answer with simulations. Assume that the circuit has reached steady state prior to the input pulse transitioning from +10V to -10V. Use the diode model parameters below: (**Hint:** look up book Cadence example Fig2_19).

.model Dtrr is=1e-15 tt=10e-9 cj0=1e-12 vj=0.7 m=0.33