ECE 445: Introduction to VLSI Design

Spring 2019

ECE Department, University of Idaho

Instructor : Dr. Vishal Saxena (Dr. Saxena)
Email : vsaxena AT uidaho.edu
Time : MW 8:00 AM - 9:20 AM
Course dates : Jan 9 – May 3, 2019
Location : JEB 021
Course Homepage: http://lumerink.com/courses/ECE445/s19/ECE445.htm
Office Hours : Posted on course page.

Prerequisites: ECE 310, or an equivalent course.

Textbooks:

- CMOS Circuit Design, Layout and Simulation – R. J. Baker, 3rd Edition, Wiley-IEEE, 2010.
- CMOS VLSI Design: A Circuits and Systems Perspective, N. Weste and D. Harris, 4th Ed., Addison-Wesley, 2010.

Course content – An introduction to digital CMOS IC design, layout and simulation. MOSFET operation and parasitics. Digital design fundamentals: combinational logic design, logic families, sequential circuit design and datapath subsystems. Logical effort, delay, power and design methodology and tools. Charge pump circuits.

Course Topics:

- Overview of CMOS Mask Layers: The n-well, layout of n-well, design rules, sheet resistance.
- Review of p-n junction: Built-in potential, depletion width, depletion capacitance, transit-time, diode reverse-recovery time.
- Distributed RC line and Elmore delay. Metal layers and delay calculations, Supply noise, Decoupling. Bond pads (capacitance, pitch, ESD).
- Active n-select (nactive), p-select (pactive), poly and silicide-block layers, self-aligned gate process. N-well resistor with contacts, polysilicon resistors, NMOS/PMOS layout, poly-poly capacitor.
- Overview of Layout cells and pcells in the Cadence design kit.
- ***MOS Physics:*** Accumulation, depletion, inversion. Bottom plate capacitance, lateral diffusion, oxide encroachment. MOS Overlap Capacitances: CGSO, CGDO, CGBO.
- ***Review of MOSFET Physics:*** CV plot, overlap capacitances in MOSFET. Threshold voltage derivation (V_{THN}), body factor. MOSFET: I-V characteristics, triode, pinch-off, saturation.
- MOSFET channel length modulation. Subthreshold characteristics & slope, leakage current, ***Short-channel effects*** (DIBL, GIDL, Gate-leakage, hot-electron effect, etc.)
- CMOS Scaling and Challenges (ITRS/IRDS trends)

- **MOSFET Digital Models for design:** Effective Switching resistance (R_n and R_p), process dependent time-constants, delay definitions. Miller capacitance.
- ***Pass gates*,** Transmission Gate (TG), delay.
- ***CMOS Inverter***: DC characteristics, noise margin, switching point, beta ratio.
- ***Ring oscillator***, dynamic power (CV^2f) consumption, tristate inverters. ***Logical Effort*** and Buffer sizing.
- ***Static logic design***: Sizing, skew, layout, input order. Sizing and application of Logical Effort. Pseudo-NMOS logic, CVSL logic.
- ***Clocked circuits:*** SR latches, cross-coupled inverter latch. Flip-flops, setup and hold time, FF delays. Dynamic latch and FFs. Flip-flop $t_{setup}/t_{hold}/t_{pcq}$ calculations.
- ***Logic Sequencing***- Max and min delays, clock skew.
- ***Dynamic logic gates:*** Footed dynamic logic, monotonicity, and Domino logic.
- ***Introduction to Memory Architectures***: DRAM (1T1C cell, charge sharing, sense-amps, Row and Column decoders), SRAM (6T-cell, read margin), Flash (SLC, NOR/NAND array, FN Tunneling, sense-amp, MLC), Emerging devices.

CAD software information:
The course will require extensive use of Cadence Design System Tools in Linux environment. Design projects will involve schematic, simulation and layout using a realistic process development kit (PDK).

For the design/fabrication of chips in this class, On Semiconductor 0.5µm (C5 with two polysilicon layers and 3 levels of metal) will be used with a MOSIS technology code of SCN3ME_SUBM with a lambda of 0.3µm. Refer to the wiki page for information on design rules and process test results and corner parameters.

Workload (Grading):
20% Midterm Exam 1
20% Midterm Exam 2
20% Homeworks
20% Design Project
20% Final Exam

Policies:

- Homework and exam scores become final one week after they are returned to the class.
- Submission will not be accepted if the solutions are distributed by any means.
- Late submissions of assignments and project reports are not encouraged; however, if you cannot finish in time and submit late before the solutions are available, a 25% per day compounding deduction may be applied on the final grade. (Ex.:100 points assignment submitted 3 days late will be graded on 42 points, 1 day on 75, 2 days 56, 4 days 32, etc.).
- Assignments have to be turned in during class session. I will not accept any assignment dropped in my office mailbox without getting my permission earlier. You may consult

with others on assignments, provided you only submit your attempt at the work. Identical assignments will receive a grade of zero and be considered as academic dishonesty case.

- Final exam will not be returned at the end of the semester.
- Only students presenting medical or official university excuses to the instructor will be allowed to take a make-up exam or other missed assignments. Whenever possible, arrangements should be made with the instructor prior to the regularly scheduled exam or assignment due date. Making these arrangements is entirely the responsibility of the student. Make up exams or other assignments may differ from those given at the regularly scheduled time, and whether an absence is deemed to be excusable is at the discretion of the instructor.

Academic Honesty:
Academic honesty is governed by Article II of the University of Idaho's Student Code of Conduct http://www.webs.uidaho.edu/fsh/2300.html. Cheating on classroom or outside assignments, including examinations is a violation of this code. Incidents of academic dishonesty will be kept on file by the instructor and may be reported to the dean of students. Such instances of academic dishonesty may warrant expulsion from the course and a failing grade. All students should be aware that even one incident of academic dishonesty may also merit expulsion from the University.

Disability Support:
Center for Disability Access and Resources for Reasonable Accommodations Statement: Reasonable accommodations are available for students who have documented temporary or permanent disabilities. All accommodations must be approved through the Center for Disability Access and Resources located in the Bruce M. Pitman Center, Suite 127 in order to notify your instructor(s) as soon as possible regarding accommodation(s) needed for the course.

- Phone :(208) 885-6307
- Email : cdar@uidaho.edu
- URL : www.uidaho.edu/current-students/cdar

Civility Clause:
University of Idaho Classroom Learning Civility Clause
In any environment in which people gather to learn, it is essential that all members feel as free and safe as possible in their participation. To this end, it is expected that everyone in this course will be treated with mutual respect and civility, with an understanding that all of us (students, instructors, professors, guests, and teaching assistants) will be respectful and civil to one another in discussion, in action, in teaching, and in learning.

Should you feel our classroom interactions do not reflect an environment of civility and respect, you are encouraged to meet with your instructor during office hours to discuss your concern. Additional resources for expression of concern or requesting support include the Dean of Students office and staff (5-6757), the UI Counseling & Testing Center's confidential services (5-6716), or the UI Office of Human Rights, Access, & Inclusion (5-4285).

Concealed Firearms:
The University of Idaho bans firearms from its property with only limited exceptions. One exception applies to persons who hold a valid Idaho enhanced concealed carry license, provided

those firearms remain concealed at all times. If an enhanced concealed carry license holder's firearm is displayed, other than in necessary self-defense, it is a violation of University policy. Please contact local law enforcement (call 911) to report firearms on University property.