ECE 445 Intro to VLSI Design
Sample Midterm 2
Apr 8, 2019 **Name:** _____

Closed Book, Closed Notes, Closed Computer. Show your steps clearly to get credit. State clearly any assumptions made. This exam has 6 questions, for a total of 100 points.

Unless otherwise indicated use the following device parameters for the C5 process for hand calculations:

Parameter	**Value**
Scale factor (λ)	$0.3\,\mu m$
V_{DD}	5 V
C'_{ox}	$2.8\frac{fF}{\mu m^2}$
V_{THN}	0.8 V
V_{THP}	0.9 V
KP_n	115 $\frac{\mu A}{V^2}$
KP_p	60 $\frac{\mu A}{V^2}$

Long Channel MOSFET equations:

$V_{THN} = V_{THN0} + \gamma(\sqrt{|2V_{fp}| + V_{SB}} - \sqrt{|2V_{fp}|})$

$$I_D = \begin{cases} KP_n \frac{W}{L}\left((V_{GS} - V_{THN})\,V_{DS} - \frac{V_{DS}^2}{2}\right), & V_{DS} < V_{GS} - V_{THN} \\ \frac{1}{2}KP_n \frac{W}{L}\left(V_{GS} - V_{THN}\right)^2, & V_{DS} \geq V_{GS} - V_{THN} \end{cases}, \quad V_{GS} > V_{THN}$$

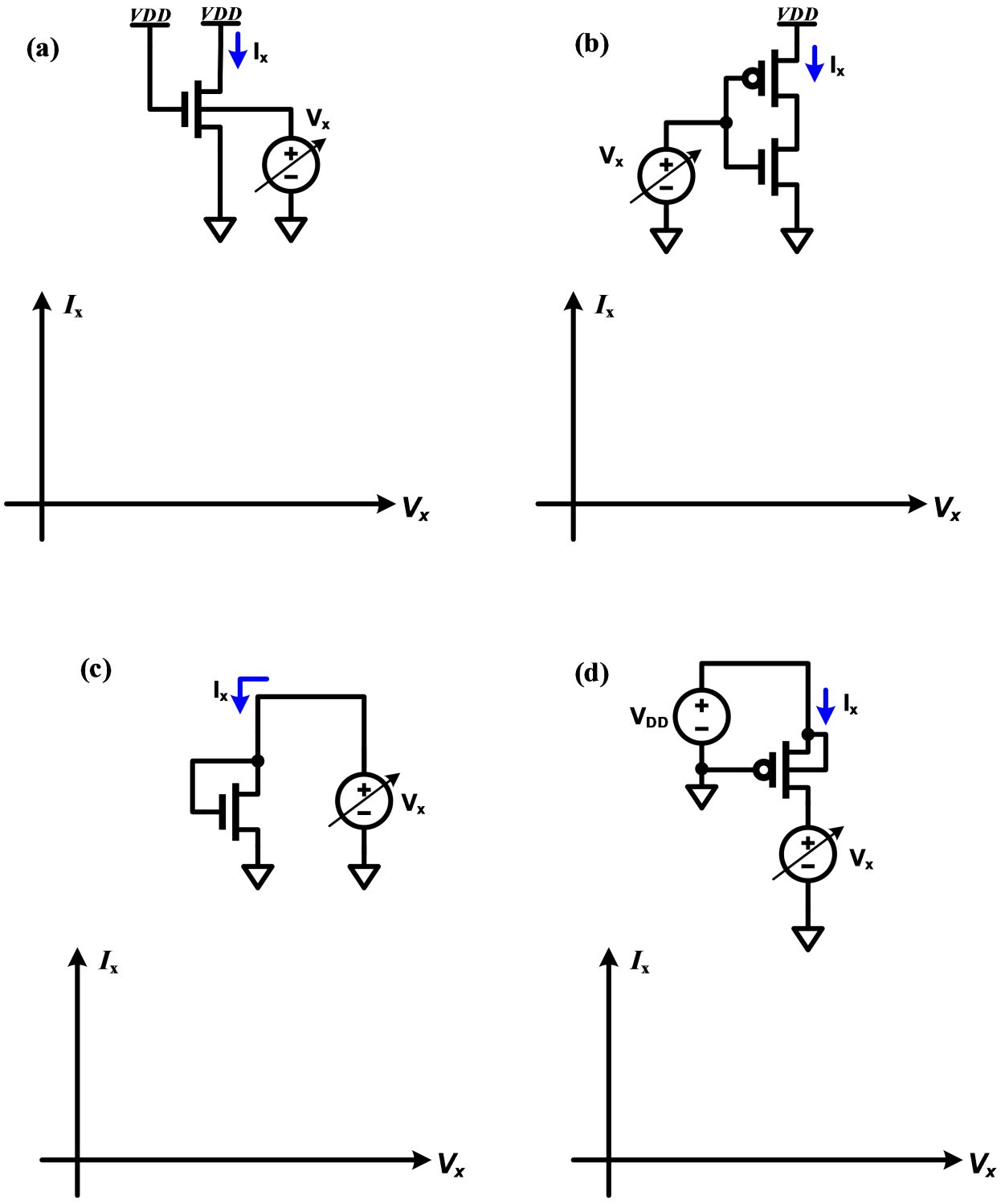
Digital MOSFET Model:

$R'_{n,p} = \frac{V_{DD}}{\frac{1}{2}KP_{n,p}(V_{DD} - V_{THN})^2}$
$R_{n,p} = R'_{n,p}\frac{L}{W}$

Logical Effort equations:

$F = GBH \triangleq H$ for an inverter chain
$\hat{f} = F^{\frac{1}{N}}$ for the least delay
$D = P + N \cdot \hat{f}$

1. (10 points) For the circuits seen below, plot the current I_x as the voltage V_x is swept from 0 to V_{DD}.



2. (a) (5 points) Based on the data provided on the first page, estimate C'_{ox}, R'_n, and R'_p. *Show your work.*

(b) (5 points) Fill the following table using the data provided on the first page.

Device	**Drawn**	**Actual size**	$R_{n,p}$	$C_{oxn,p}$
NMOS	10/2	$3\,\mu m$ by $0.6\,\mu m$		fF
PMOS	20/2	$4.5\,\mu m$ by $0.6\,\mu m$		fF

3. (a) (10 points) Estimate the oscillation frequency (f_{osc}) of a 21-stage ring oscillator designed using 10/2 NMOS and 20/2 PMOS devices.

(b) (5 points) Calculate the total dynamic power dissipated in the oscillator?

(c) (5 points) How does f_{osc} change when the supply voltage V_{DD} is varied from 0 to 5V? *Explain.*

4. This problem involves the design a buffer to drive **10 pF** load with the **least delay**. Use the C5 process data from the first page, and the approximated switching model of MOSFETs with $C_{in} = C_{out} = C_{ox}$.

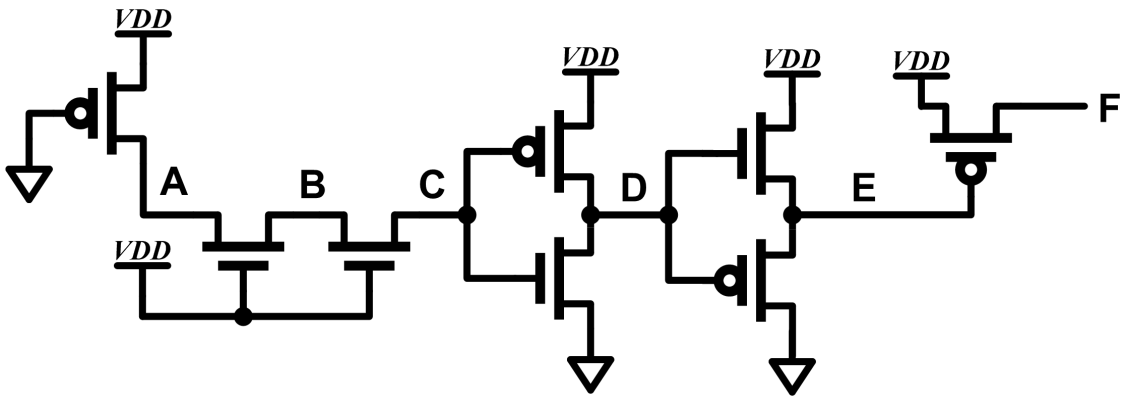
   (a) (5 points) Calculate the input capacitance (C_{in1}) and the time-constant (τ) of a unit inverter (size 20/10).

   (b) (10 points) Calculate the path effort (F) for a load of 10 pF, and find the number of stages in the buffer for least delay.

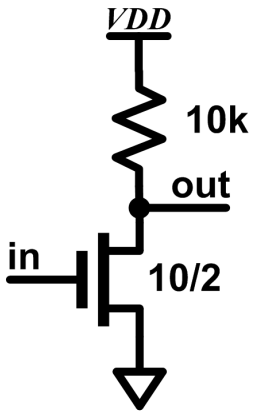
(c) (5 points) What is the normalized buffer delay (D)? What is the absolute buffer delay (t_d)?

(d) (5 points) Sketch the buffer with sizing for each of the stages.

5. (15 points) Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the circuit parameters for the 300nm model given on the first page.



6. Consider the NMOS-only inverter shown below. Use the square-law equations and C5 process data from page 1. *Show steps for partial credit.*



(a) (5 points) Calculate inverter switching point V_{sp}.

(b) (5 points) Find the voltage levels for output logic high (V_{high}) and low (V_{low}).

(c) (5 points) Plot the voltage transfer curve (VTC) for the inverter and **clearly** label V_{sp}, V_{high} and V_{low} values on the curve.

(d) (5 points) Estimate the delays t_{pLH} and t_{pHL} for the inverter driving a 100 fF load.