Quiz 2
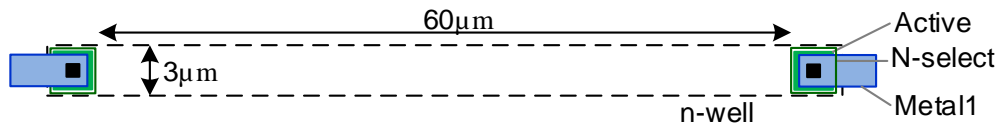
ECE 510/410 Digital IC Design   Name:_____

Fall 2015

1. a) Estimate the resistance of a 3μm×60μm n-well resistor if the n-well's sheet resistance is 800 Ω/□.

(5 points)

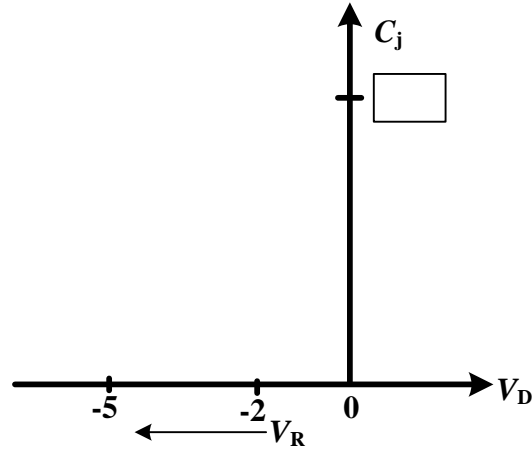**b)** If the bottom zero-bias depletion capacitance of the n-well to substrate is 100 aF/μm^2 (a is atto or 10^{-18}), the sidewall capacitance is 50 aF/μm, then estimate the delay through the resistor.

(5 points)

c) If the built-in potential between n-well and the p-substrate (V_{bi}) is 0.7 V and the grading coefficient, $m=0.5$ then sketch the depletion capacitance (C_j) between the n-well and p-substrate, as the reverse bias potential (V_R) on the n-well is increased from 0 to 5 V (the p-substrate is at ground potential). Fill in the value of C_{j0} in the box.

(5 points)

2. Find the expression for the delay seen at the outputs (V_{outA} and V_{outB}) in the circuit shown below:

(5 points)