

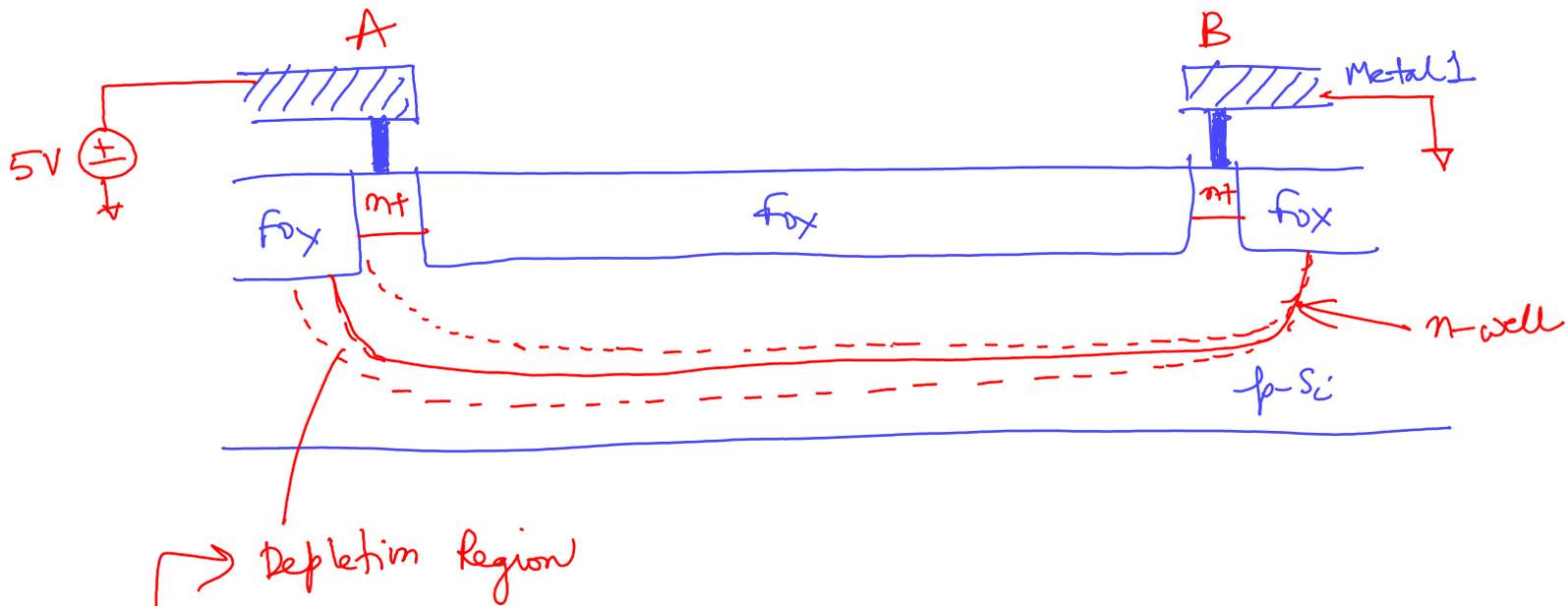
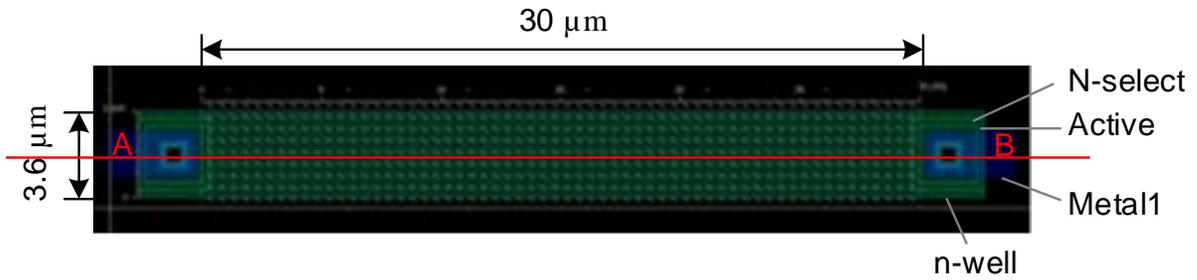
Quiz 3

ECE 510/410 Digital IC Design

Fall 2014

Name: Key

1. a) Sketch the cross-sectional view along the line in the N-well resistor layout shown below. Label all the relevant layers up to Metal-1 in your sketch. **(5 points)**



- b) If a **bias of 5V** is applied at the terminal A while keeping terminal B at ground, sketch the depletion region in your sketch for part (a). Which terminal of the resistor will have larger sheet resistance? **(5 points)**

$$R_{sheet} = \frac{\rho}{t}$$

⇒ due to the depletion region, terminal A will have higher sheet resistance due to smaller thickness.

2. Sketch **layout** and **cross-sectional** views of a **4-terminal** N-channel MOSFET (**NMOS**) showing overlap capacitances  $C_{gs}$  and  $C_{gd}$ . Label all the relevant layout layers up to Metal-1 in your sketch. **(10 points)**