

Quiz 2

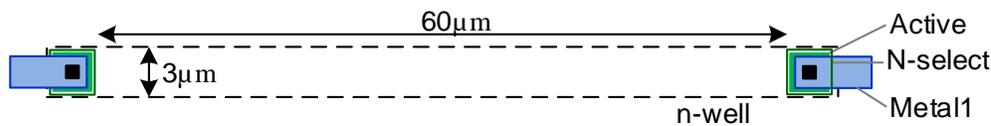
ECE 510/410 Digital IC Design

Fall 2015

Name: Key

1. a) Estimate the resistance of a $3\mu\text{m} \times 60\mu\text{m}$ n-well resistor if the n-well's sheet resistance is $800 \Omega/\square$.

(5 points)



$$R = R_{\square} \frac{L}{W} = 800 \Omega \times \frac{60 \mu\text{m}}{3 \mu\text{m}} = 16 \text{ k}\Omega$$

b) If the bottom zero-bias depletion capacitance of the n-well to substrate is $100 \text{ aF}/\mu\text{m}^2$ (a is atto or 10^{-18}), the sidewall capacitance is $50 \text{ aF}/\mu\text{m}$, then estimate the delay through the resistor.

(5 points)

$$C_{\text{tot}} = 100 \frac{\text{aF}}{\mu\text{m}^2} \times 60 \mu\text{m} \times 3 \mu\text{m} + 2 \times 60 \mu\text{m} \times 50 \frac{\text{aF}}{\mu\text{m}}$$

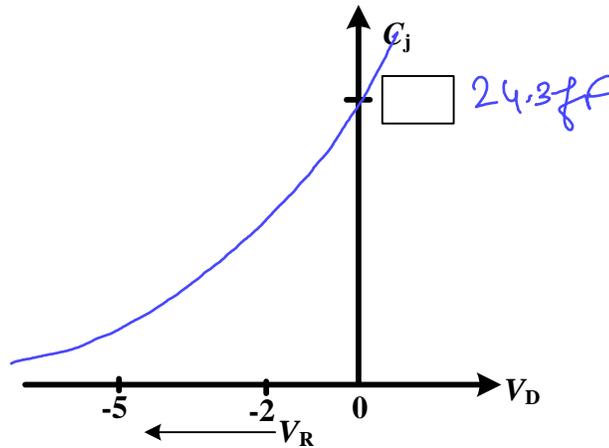
$$= 24.3 \times 10^3 \times 10^{-18} = 24.3 \text{ ff}$$

$$\Rightarrow t_d = 0.35 R_{\text{tot}} C_{\text{tot}}$$

$$= 0.35 \times 16 \text{ k}\Omega \times 24.3 \text{ ff} = 136 \text{ ps Ans.}$$

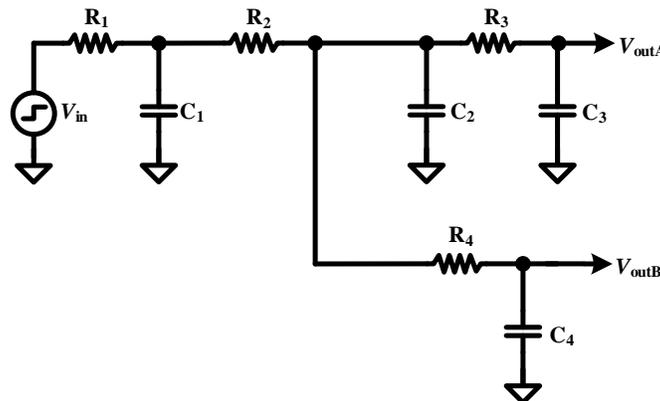
c) If the built-in potential between n-well and the p-substrate (V_{bi}) is 0.7 V and the grading coefficient, $m=0.5$ then sketch the depletion capacitance (C_j) between the n-well and p-substrate, as the reverse bias potential (V_R) on the n-well is increased from 0 to 5 V (the p-substrate is at ground potential). Fill in the value of C_{j0} in the box.

(5 points)



2. Find the expression for the delay seen at the outputs (V_{outA} and V_{outB}) in the circuit shown below:

(5 points)



$$t_{dA} = 0.7 \left[R_1 C_1 + (R_1 + R_2) (C_2 + C_4) + (R_1 + R_2 + R_3) C_3 \right]$$

$$t_{dB} = 0.7 \left[R_1 C_1 + (R_1 + R_2) (C_2 + C_3) + (R_1 + R_2 + R_4) C_4 \right]$$