Elmore Delay in RC Networks

September 16, 2010

The Elmore delay model estimates the delay of an RC ladder as shown in Fig. 1. The Elmore delay (T_D) is the sum over each node in the ladder of the resistance R_{n-i} between that node and the source (V_{in}), multiplied by the capacitance on the node:

$$T_D = \sum_{i=1}^{N} R_{n-i} C_i = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j \tag{1}$$

here R_{n-i} denotes the total resistance from the source to the node i.

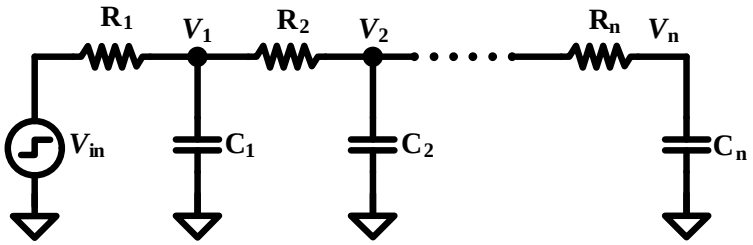

Figure 1: RC ladder

For a distributed RC ladder with all resistances equal to $R_\square$and all capacitances equal to $C_\square$, the Elmore delay is simplified as

$$T_D = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{i=1}^{N} C_\square \left(i \cdot R_\square\right) = R_\square C_\square \sum_{i=1}^{N} i \approx R_\square C_\square \frac{l^2}{2} \tag{2}$$

Note that the 50% output propagation delay (t_d), discussed in the class, is given by 0.7 times the Elmore delay, i.e. $t_d = 0.7 \cdot T_D$.

In general, a wire branching into many destination can be modeled as an RC tree. The Elmore delay from the source to node i of an RC tree is given by

$$T_{D_i} = \sum_{k=1}^{N} R_{ki} C_k \tag{3}$$

where N is the number of nodes in the tree, C_k is the capacitor on node k and R_{ki} is the effective resistance between the input and node k in common with the path between the input and node i. This expression simplifies to the simple product of resistance and capacitance for each node in an RC ladder. In RC trees, the capacitance on branches away from the path to the output is conservatively lumped as if it were at the branch point on the path. The following example will illustrate this method.

Example 1

Find the Elmore delay the the nodes V_{out3} and V_{out4} in the RC tree shown in Fig. 2.

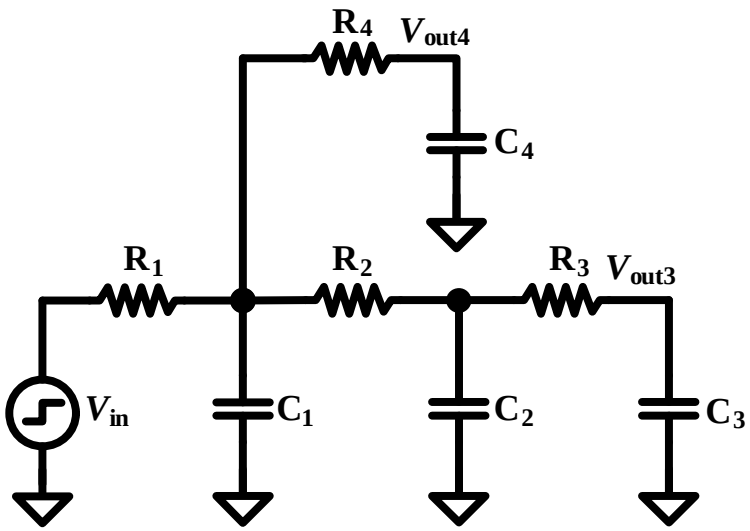

Figure 2: RC Tree

Applying the equation 3 for finding the Elmore delay at node V_{out3}, we can redraw Fig. 2 as shown in Fig. 3. Here the capacitor C_4 is not in the signal path and thus it is lumped at the branching point (i.e. resistance R_4 is ignored in the delay estimation).

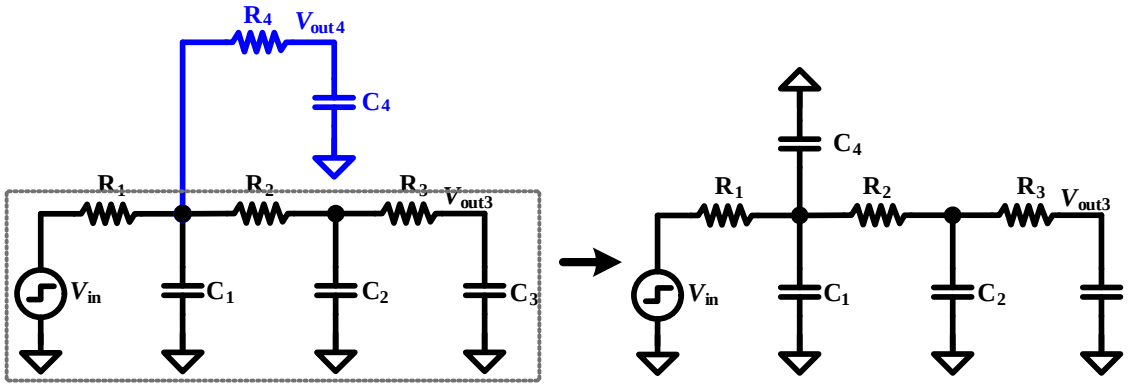

Figure 3: Estimation of Elmore delay at V_{out3} in the RC tree.

The Elmore delay at V_{out3} is now easily calculated as

$$T_{D3} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + R_1 C_4 \tag{4}$$

Similarly, for finding the Elmore delay at node V_{out4}, Fig. 2 is redrawn as shown in Fig. 4. Here the capacitors C_2 and C_3 are not in the signal path and thus are lumped at the branching point (i.e. resistances R_2 and R_3 are dropped in the delay estimation).

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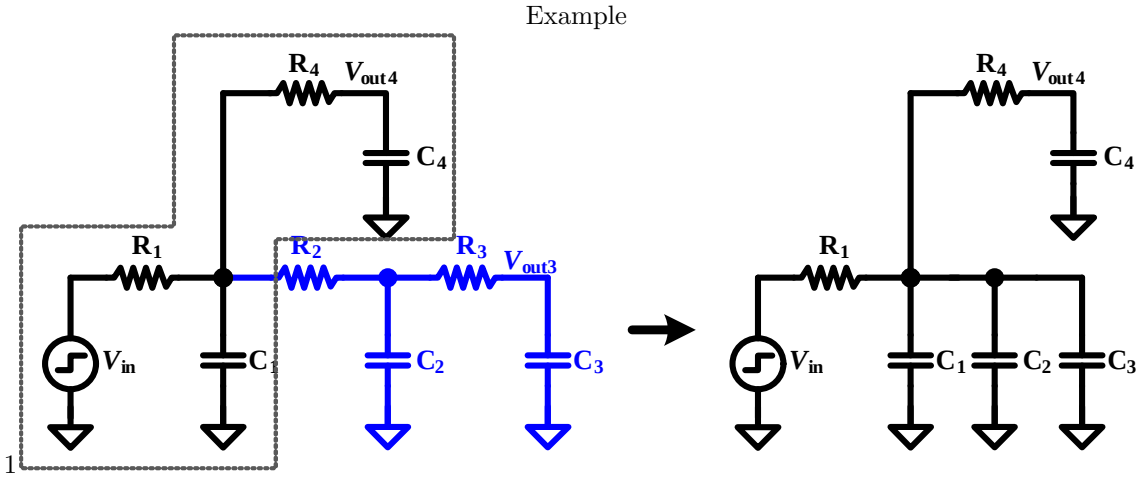

Figure 4: Estimation of Elmore delay at V_{out3} in the RC tree.

Thus, the Elmore delay at V_{out4} is given by

$$T_{D4} = R_1C_1 + R_1C_2 + R_1C_3 + (R_1 + R_4)\,C_4 \tag{5}$$

Reference

[1] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," 3rd ed., Addison Wesley, 2005.