# Clocked Circuits

## Additional Slides

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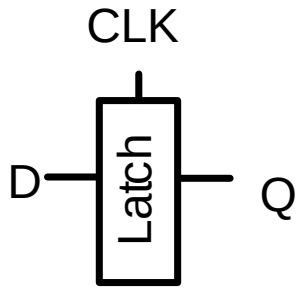
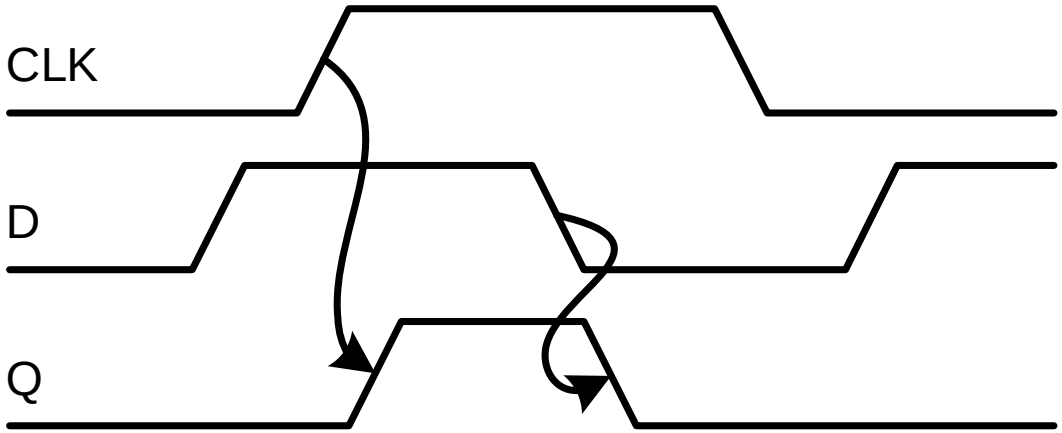
# D Latch

- When CLK = 1, latch is transparent
  - D flows through to Q like a buffer
- When CLK = 0, the latch is opaque
  - Q holds its old value independent of D



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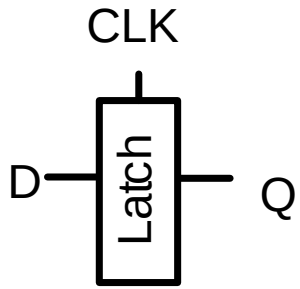


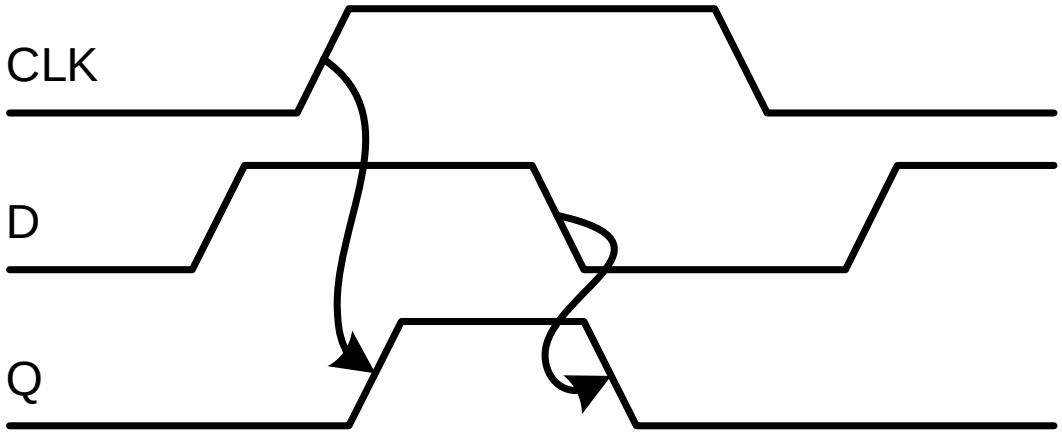

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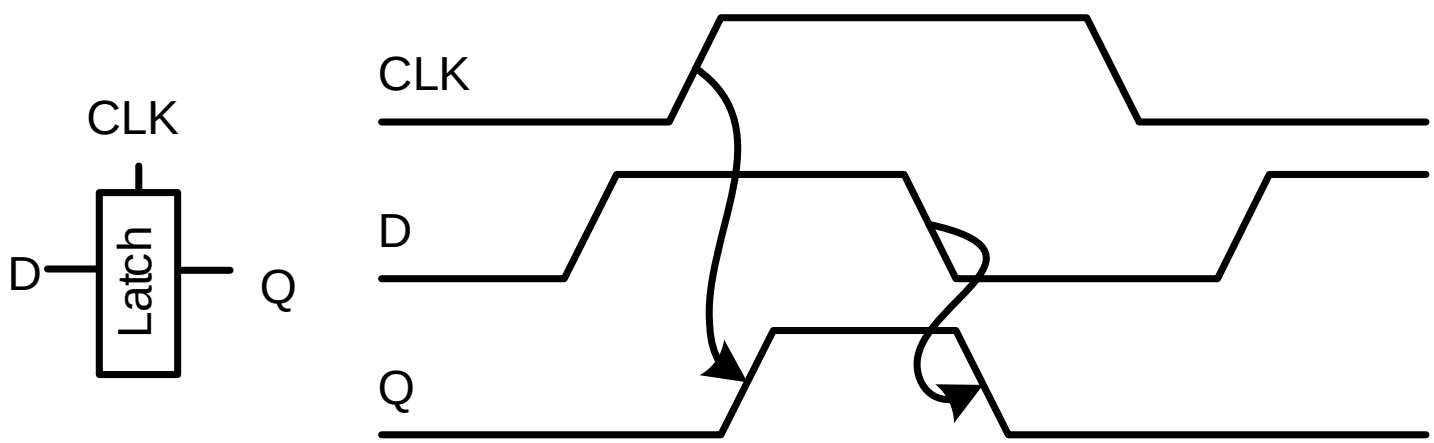

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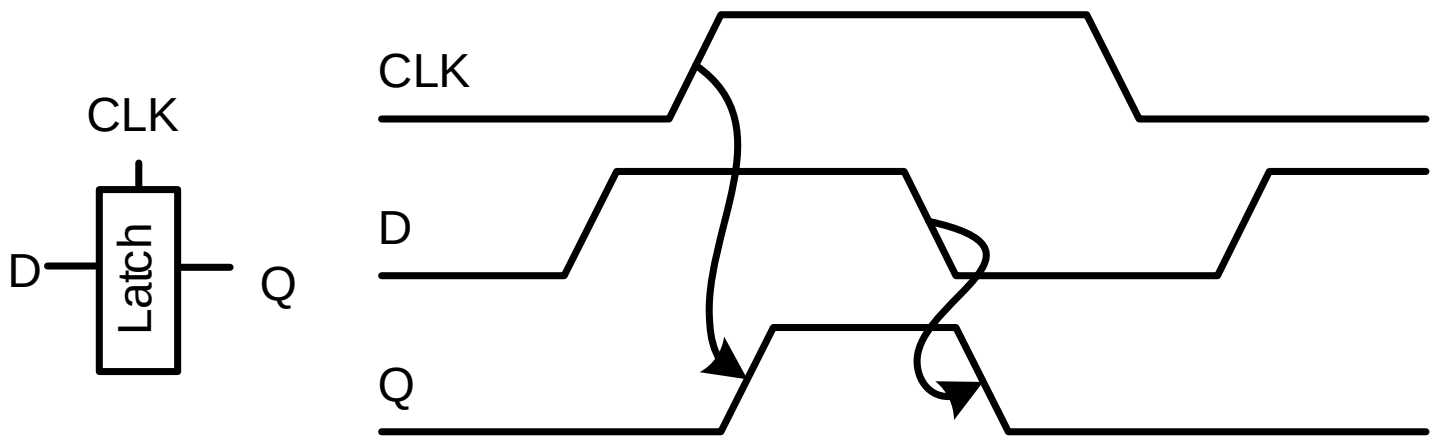
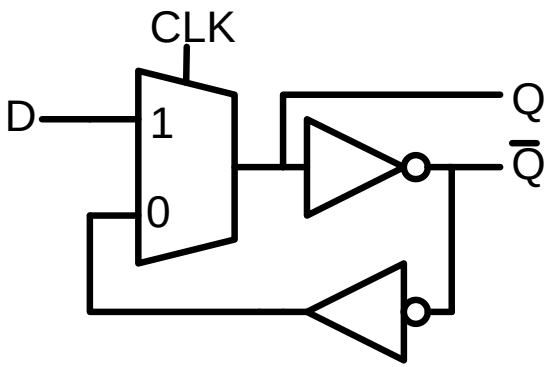
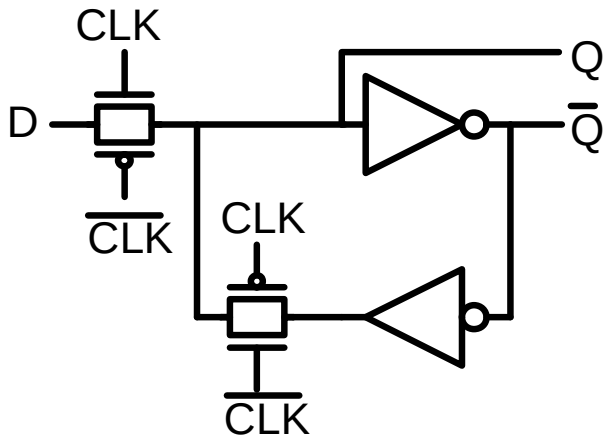


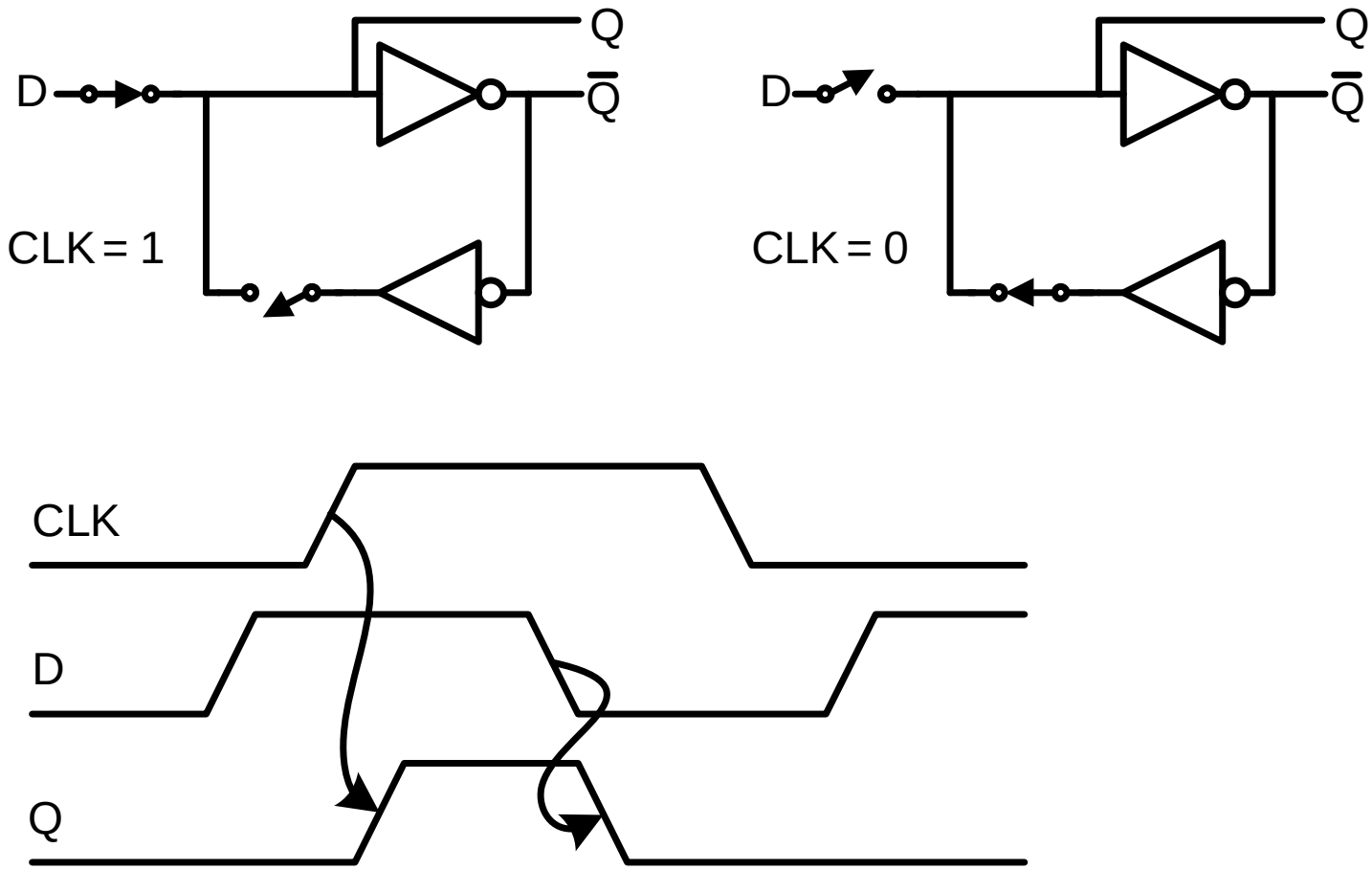
# D Latch Design

- Multiplexer chooses D or old Q



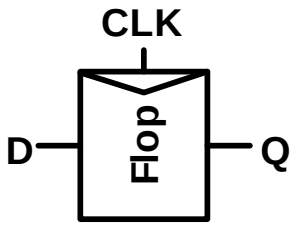



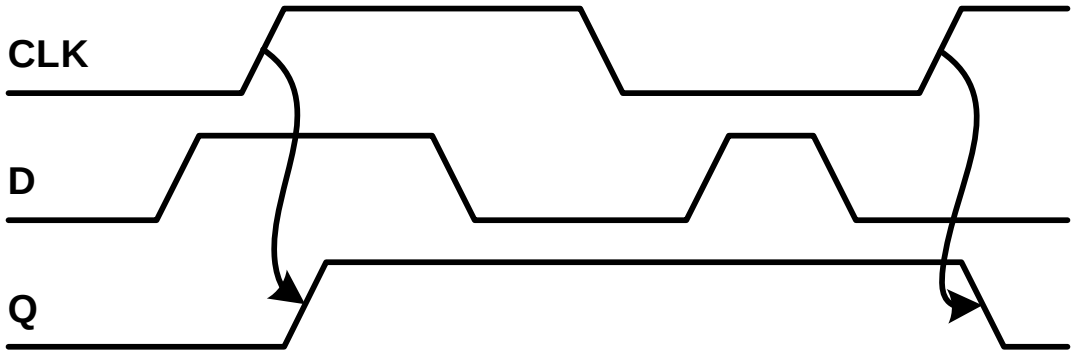
# D Latch Operation



# D Flip-flop

- When CLK rises, D is copied to Q
  - At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop*



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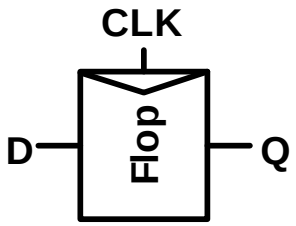


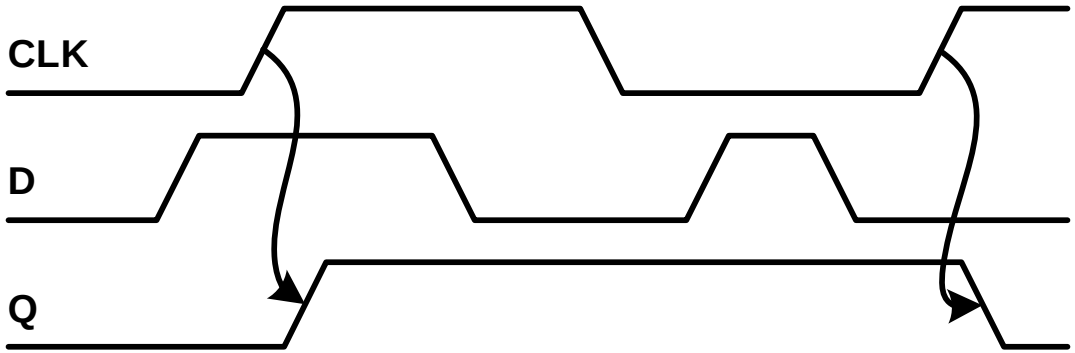

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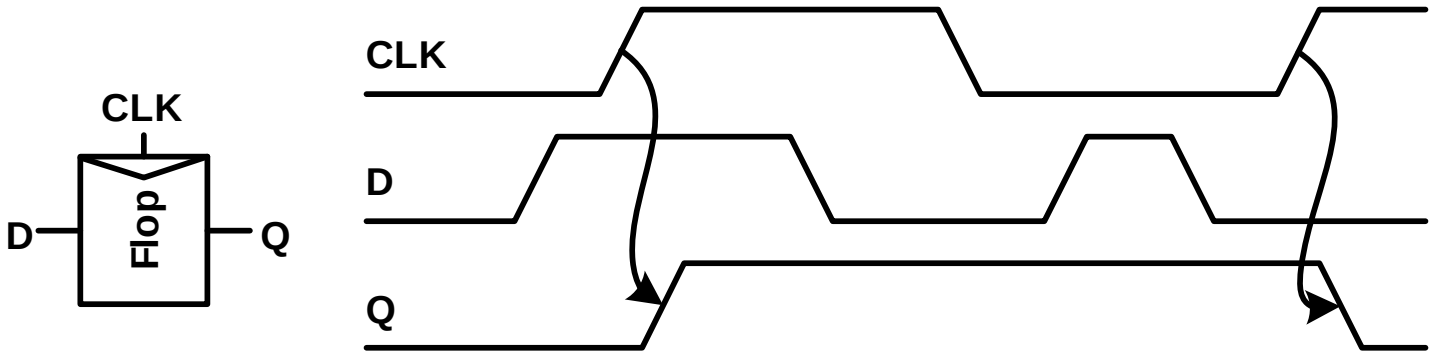
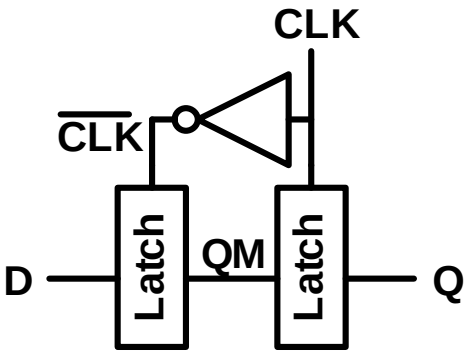
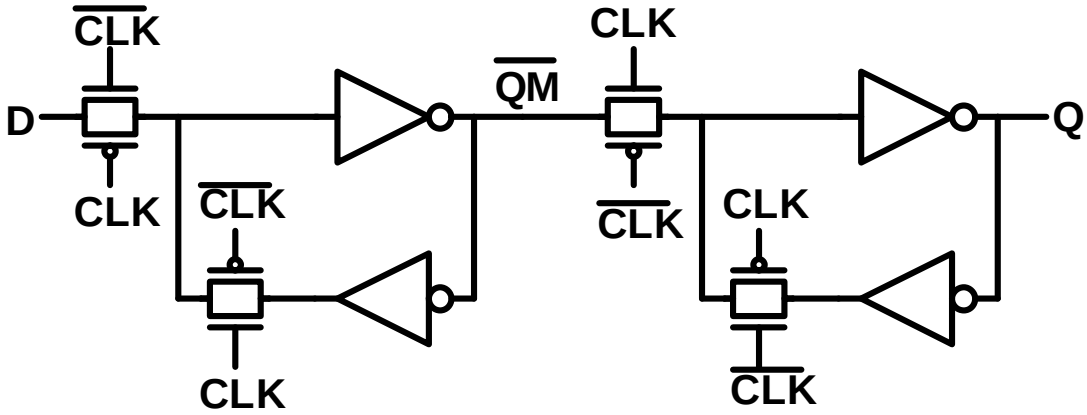


# D Flip-flop Design

- Built from master and slave D latches



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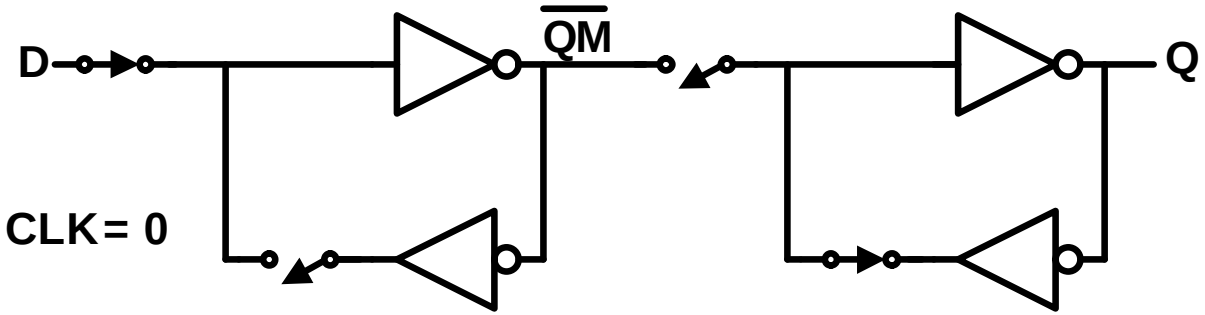


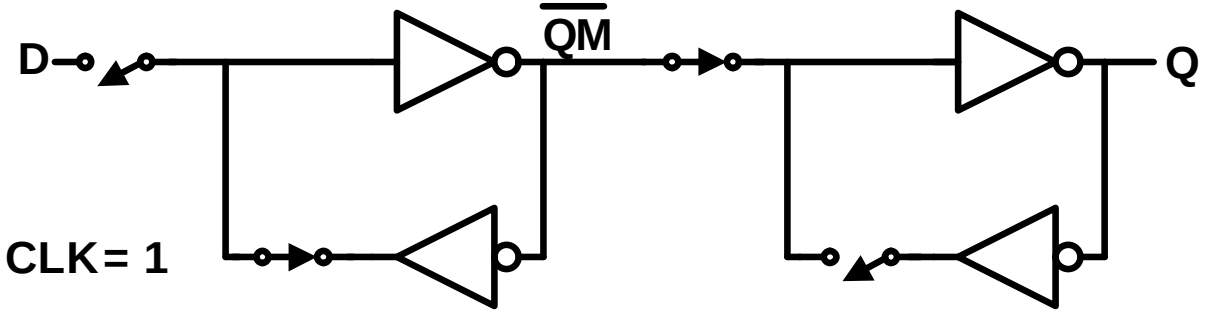


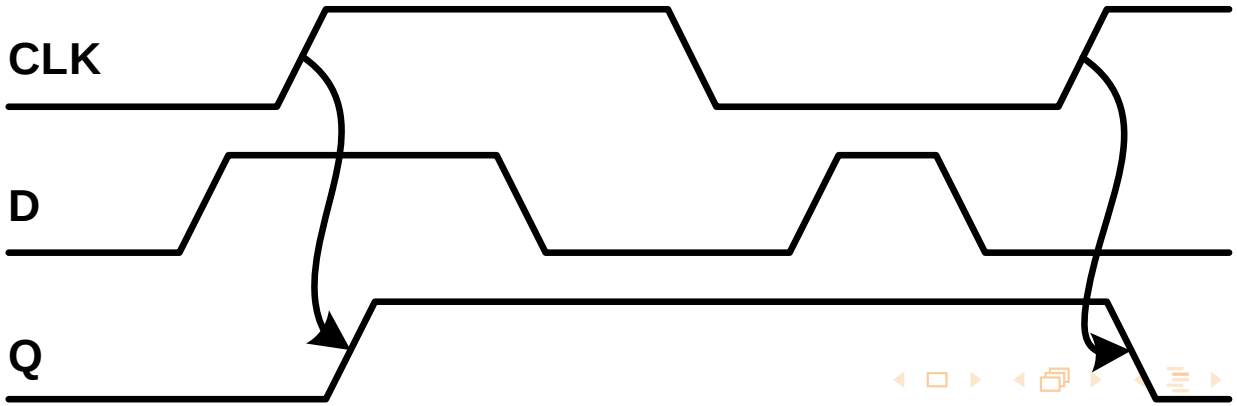

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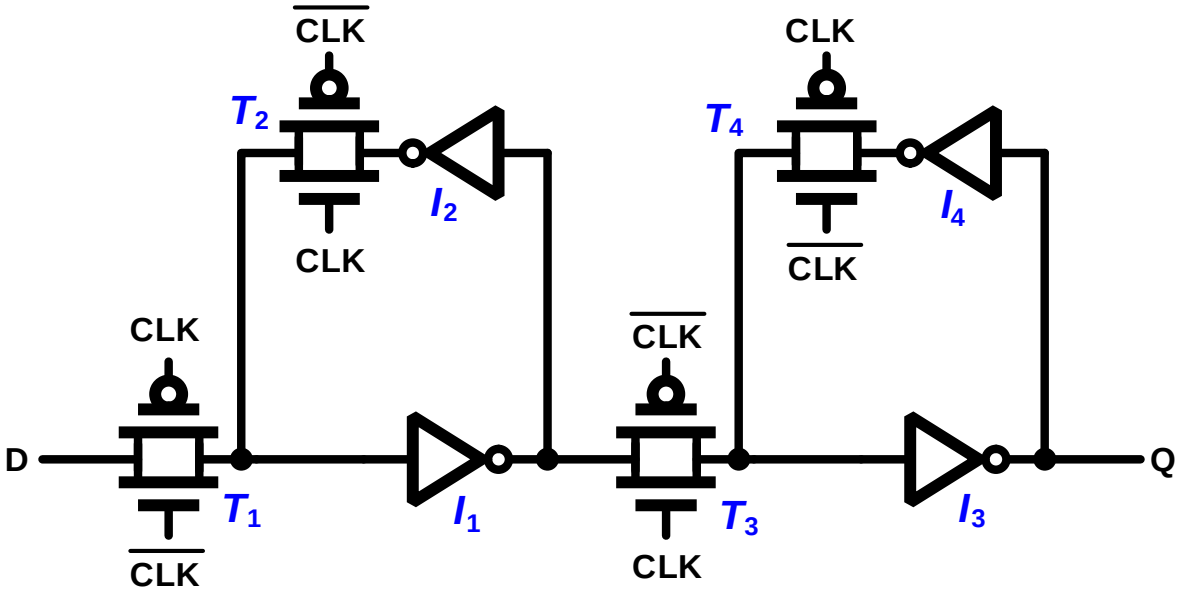


- $t_{setup} = t_{T_1} + t_{I_1}$
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- $t_{pcq} = t_{T_3} + t_{I_3}$

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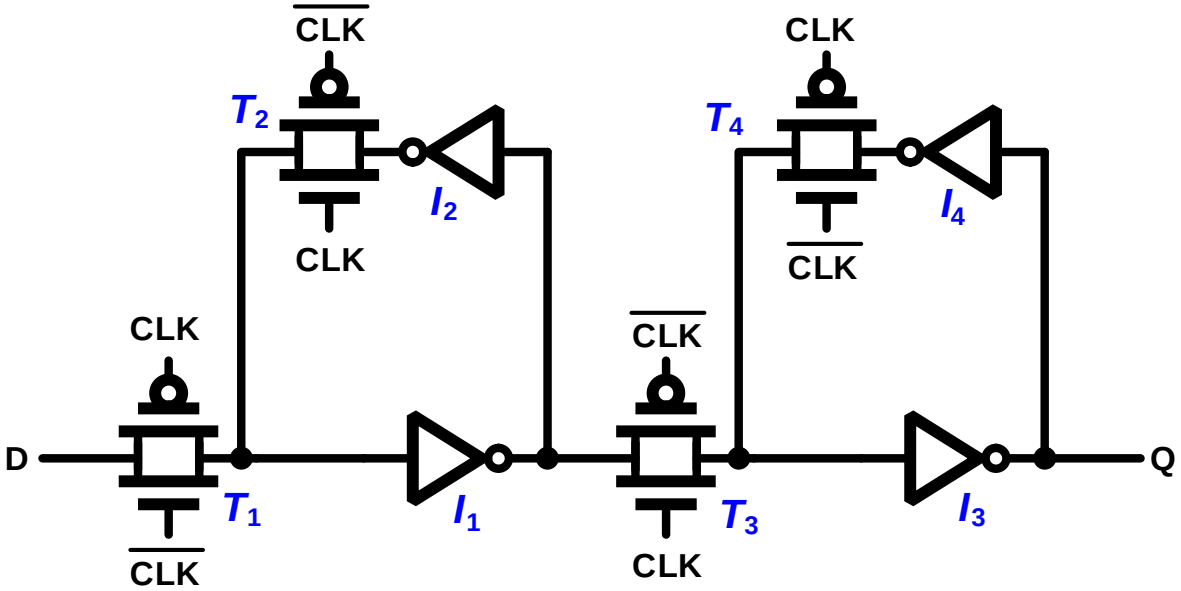


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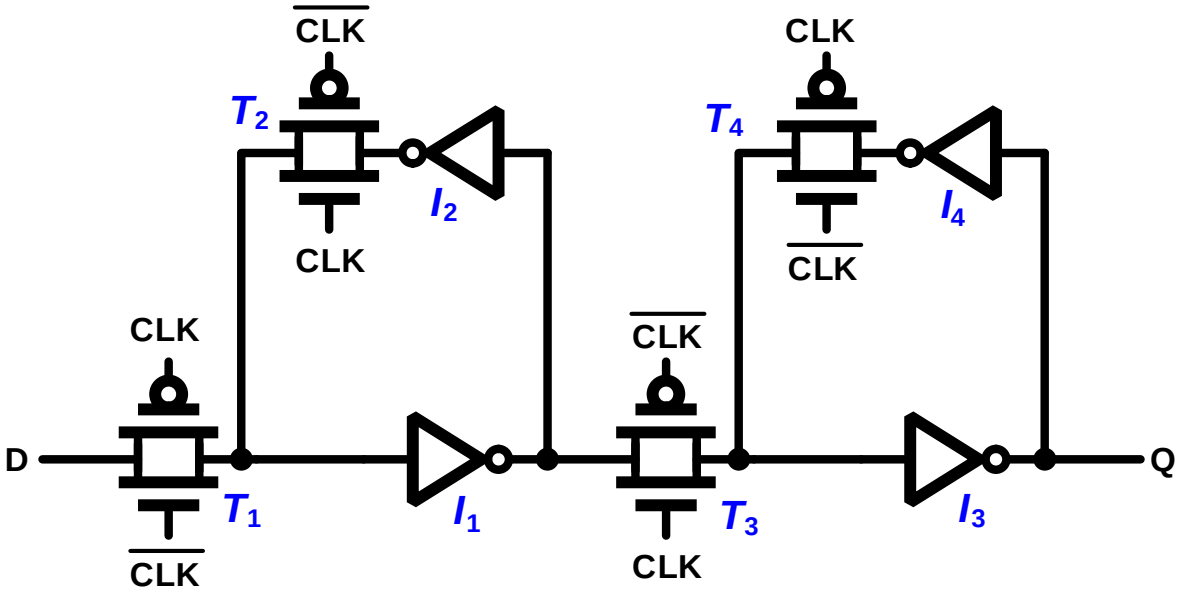


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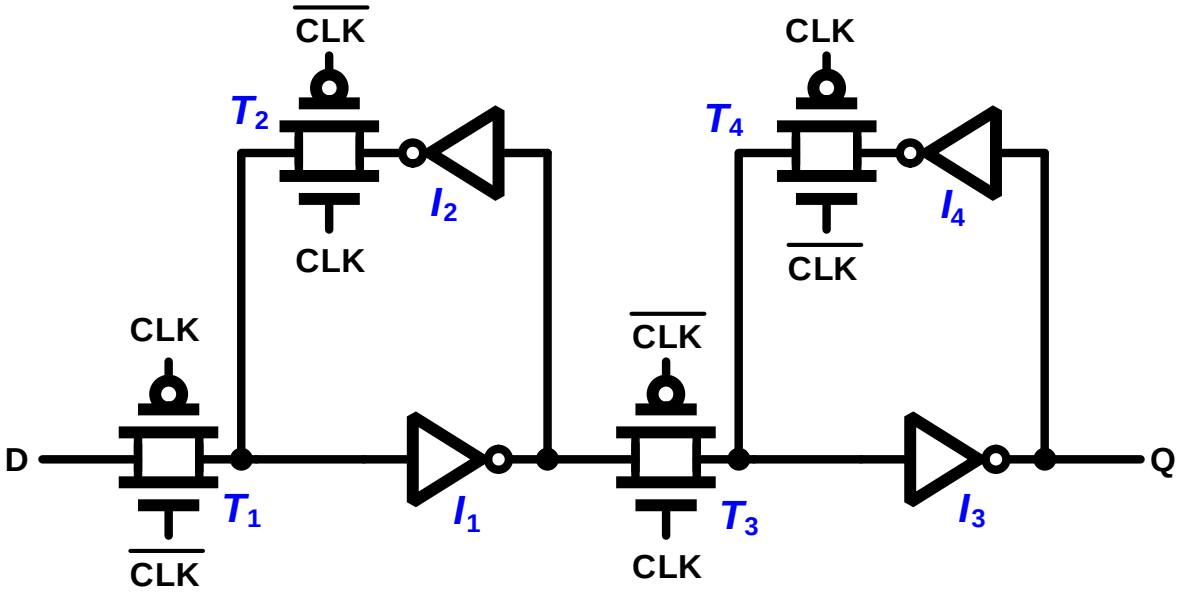


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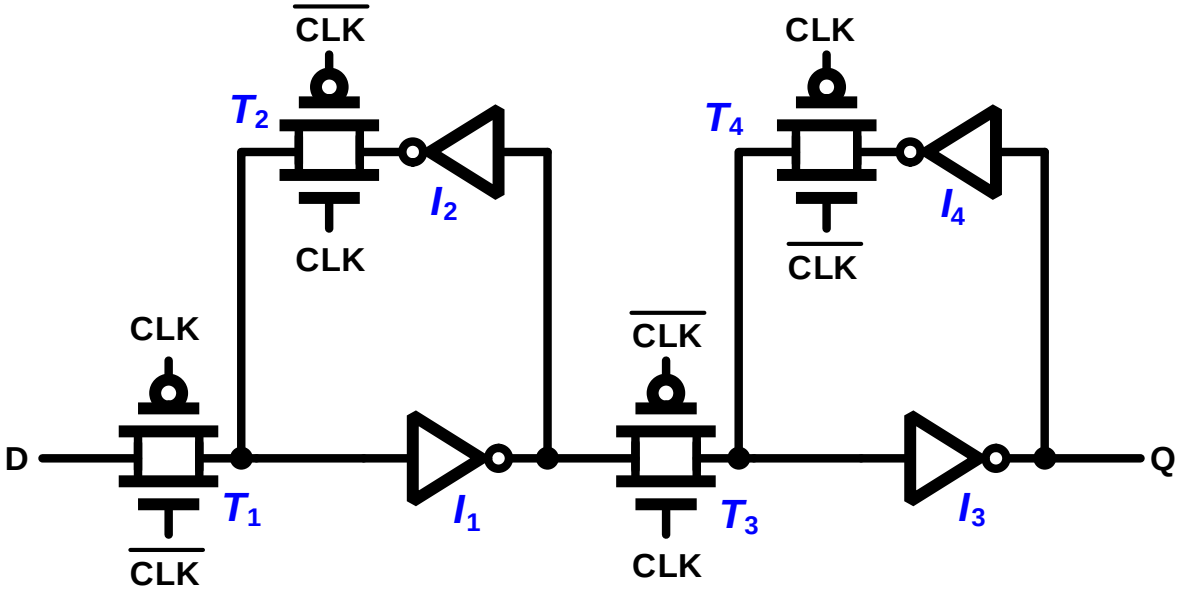


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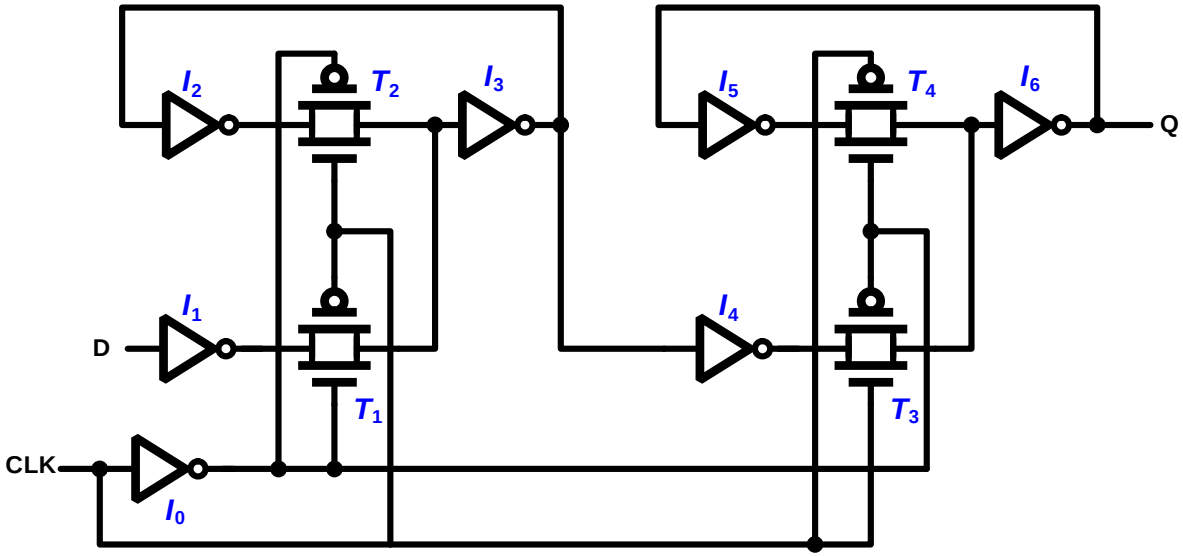


- $t_{setup} = t_{I_1} + t_{T_1} + t_{I_3} + t_{I_4}$
- $t_{hold} = t_{I_0} - (t_{I_1} + t_{T_1} + t_{I_3})$(Note that the $\overline{CLK}$ and $CLK$ have an overlap equal to an inverter delay ($t_{I_0}$))
  - Need to hold input (D), otherwise the master will latch new D value.
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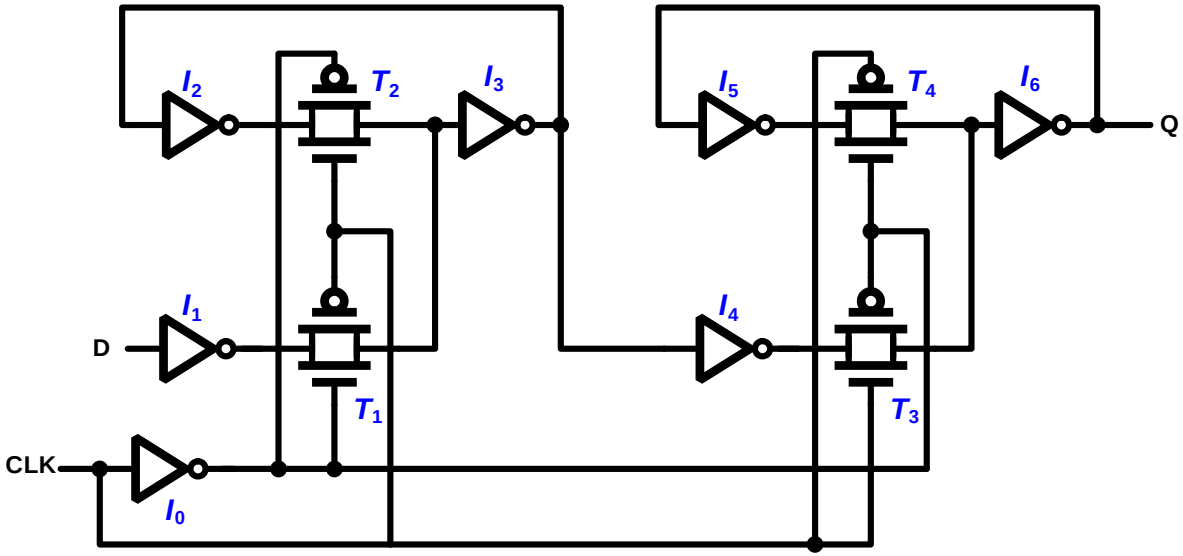


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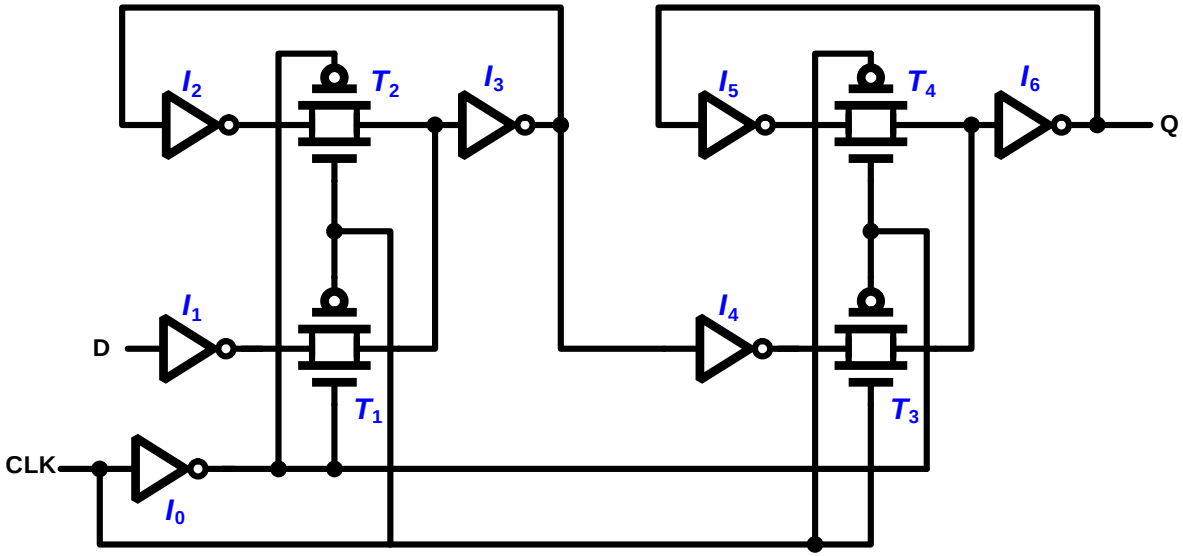


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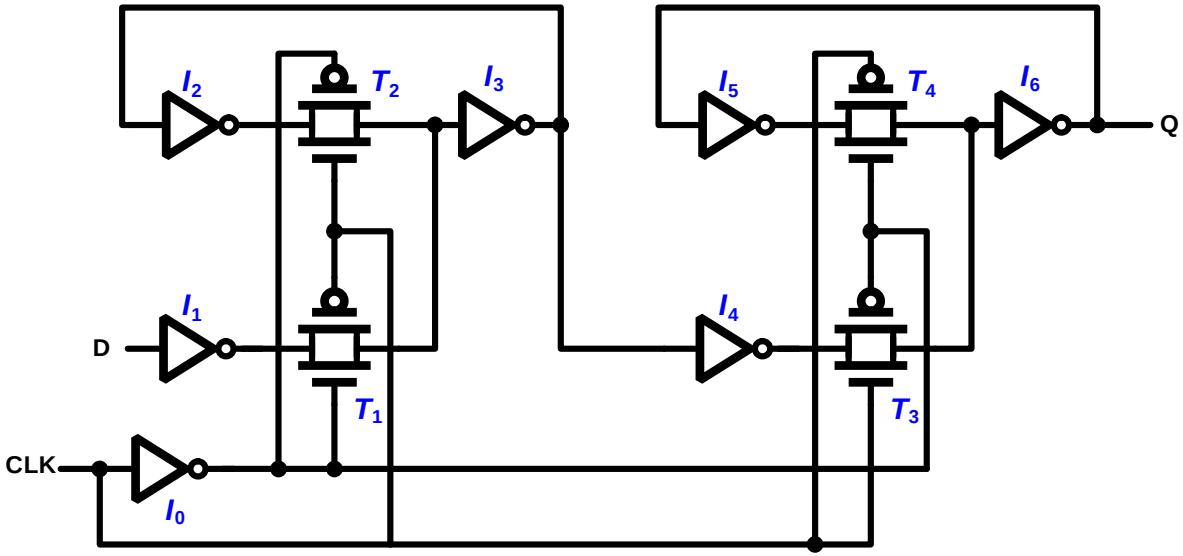


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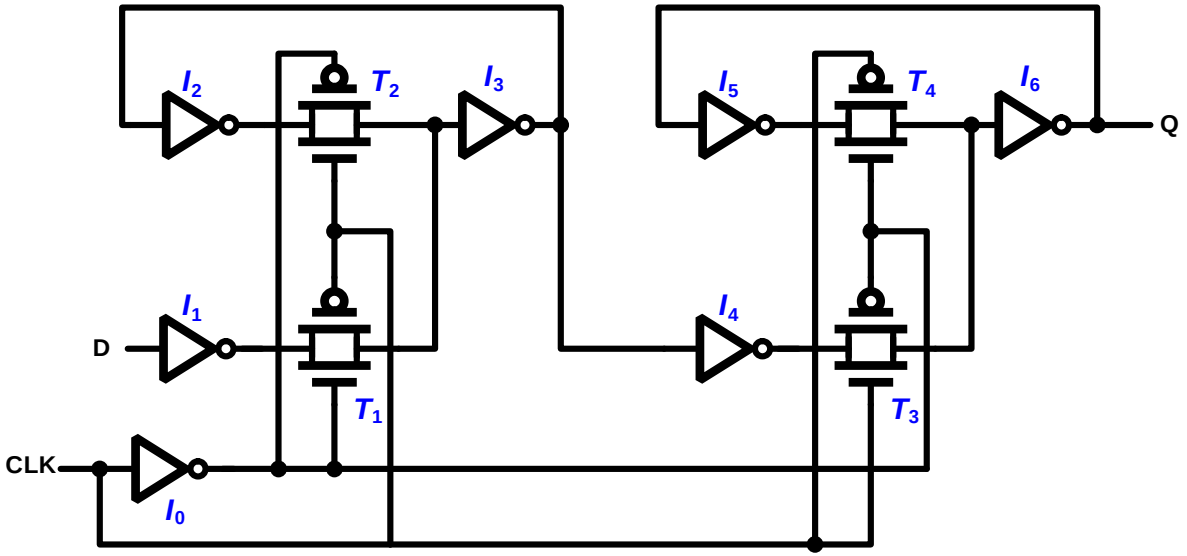


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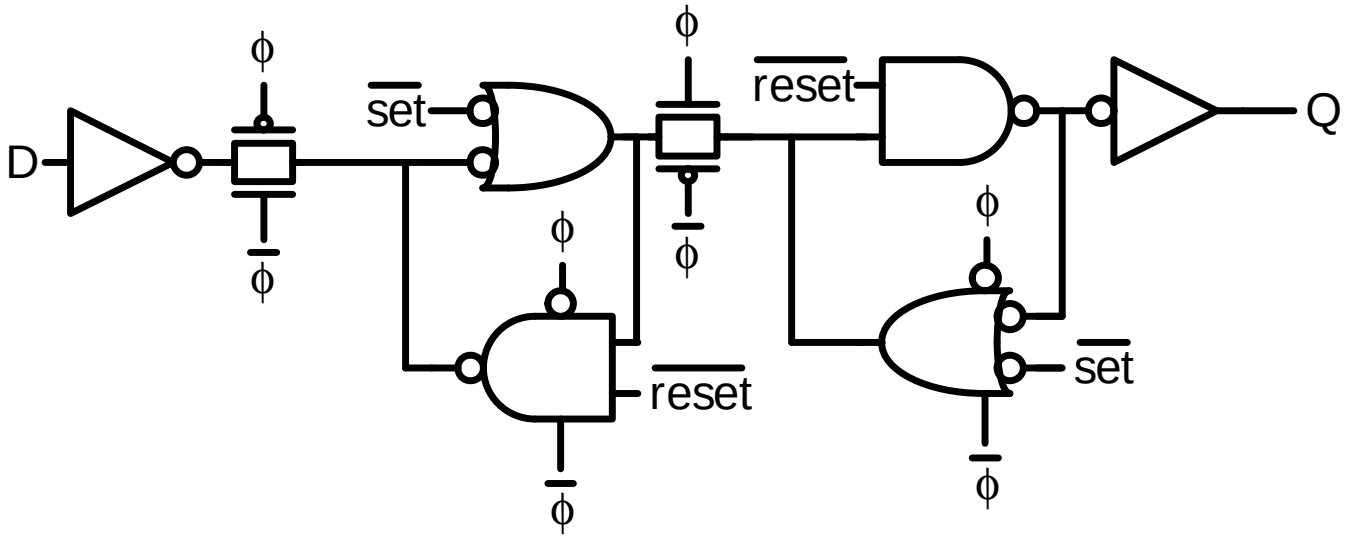
- Set forces output high when enabled
- Flip-flop with asynchronous set and reset



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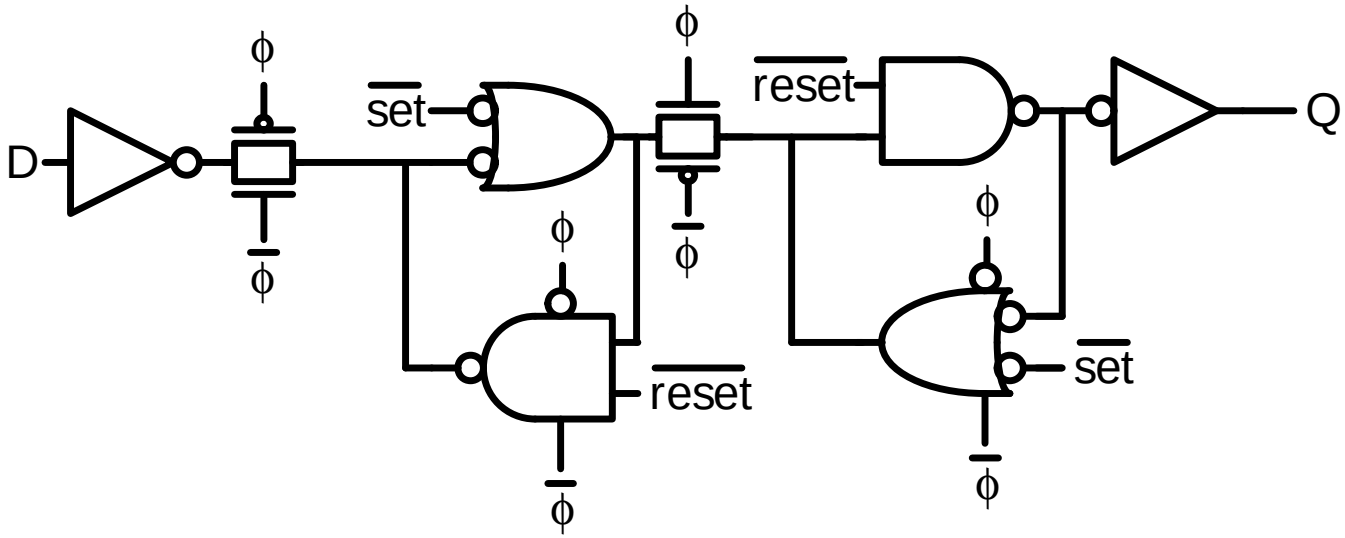

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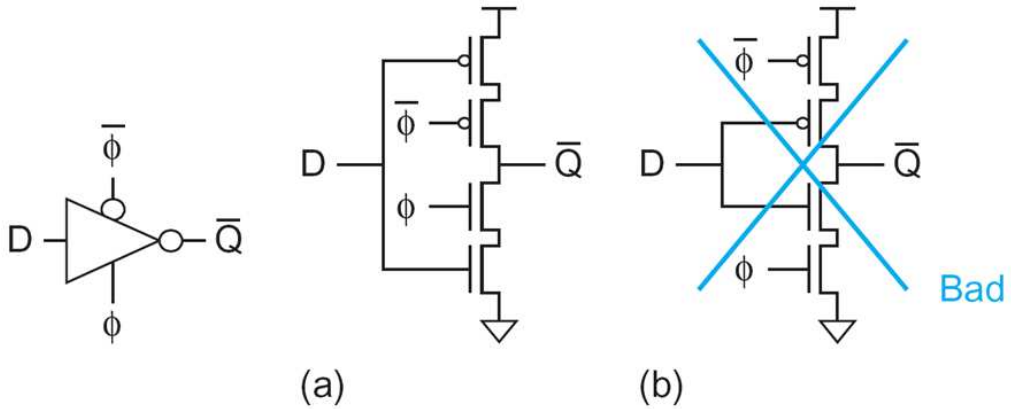
  - sometimes called clocked CMOS ($C^2MOS$) latch
  - second design is inferior as the input noise passed into the output when the latch is opaque



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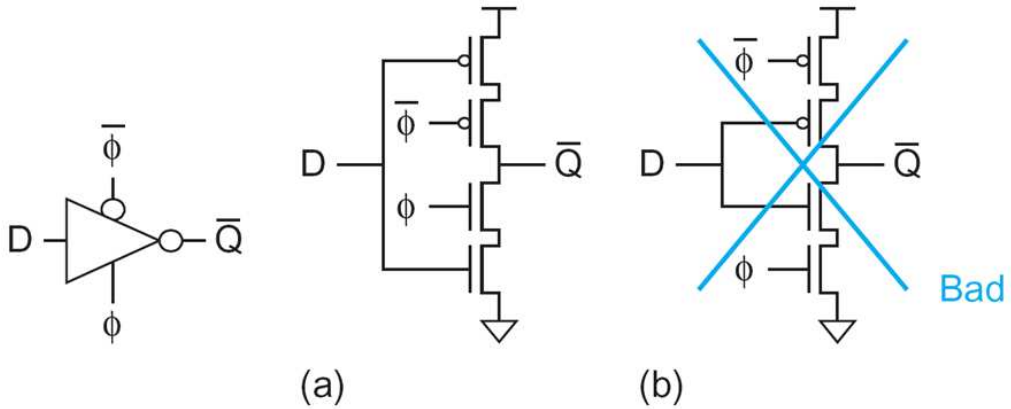

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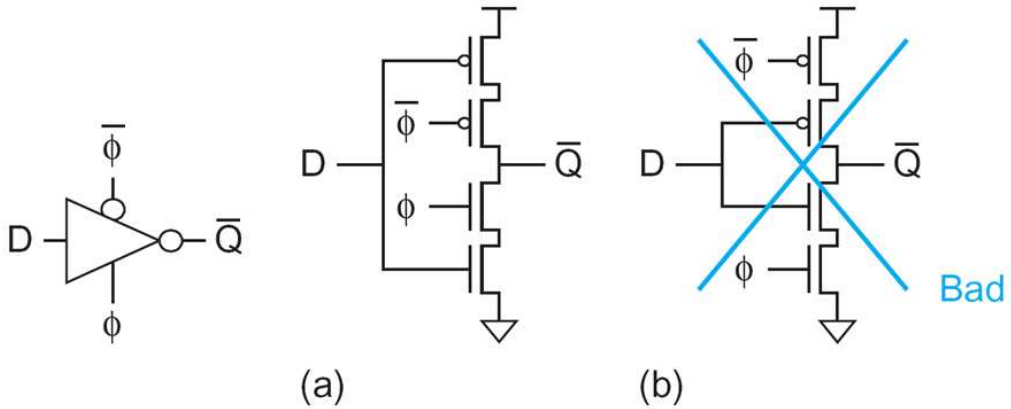
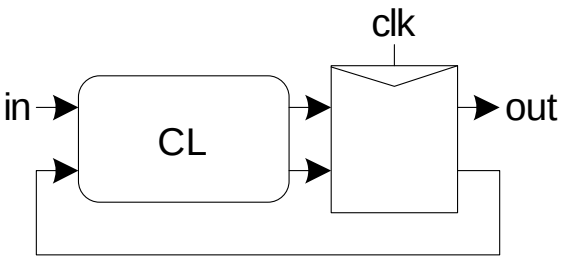
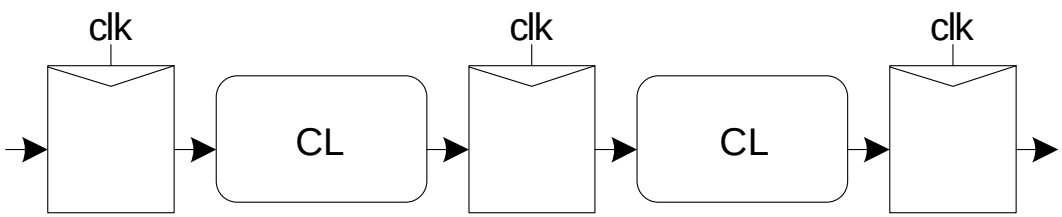


# Sequencing

- Combinational logic
  - output depends on current inputs
- Sequential logic
  - output depends on current and previous inputs
  - Requires separating previous, current, future
  - Called state or tokens
  - Ex: FSM, pipeline




Finite State Machine

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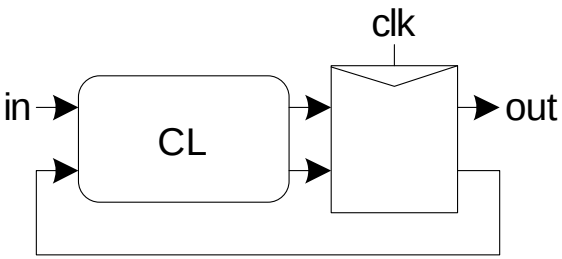


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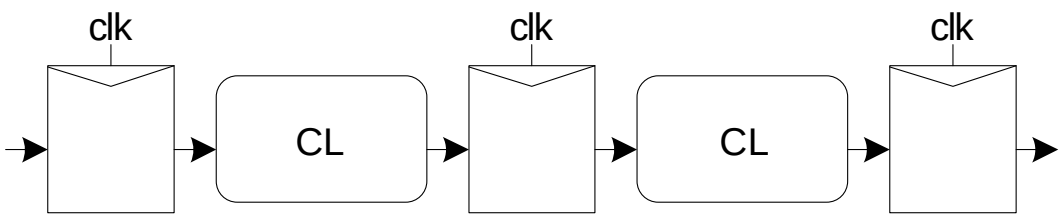


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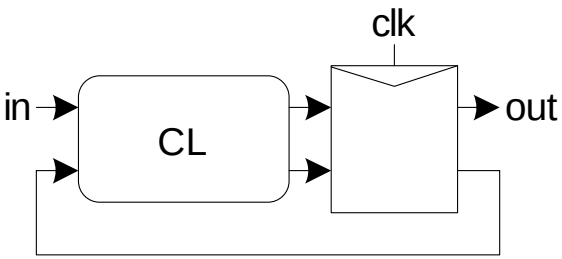


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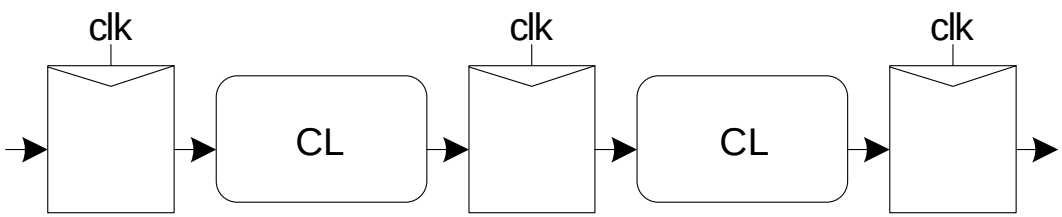


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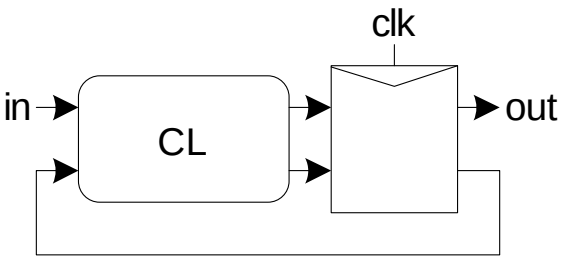


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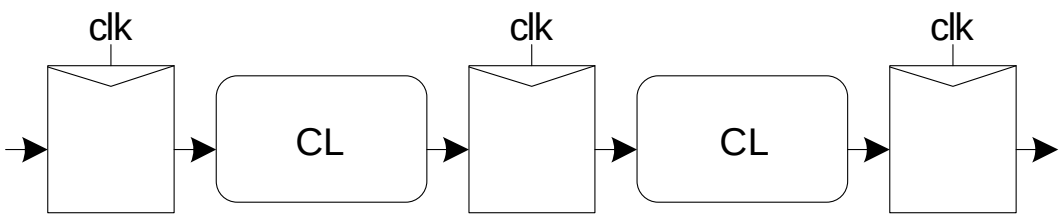


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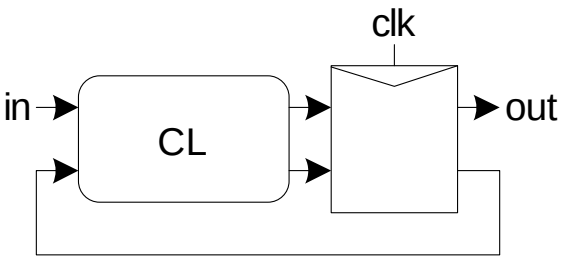


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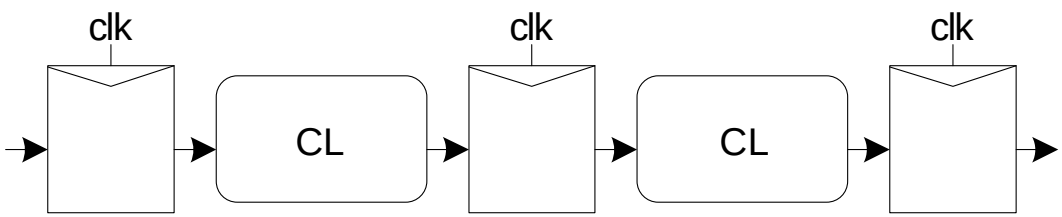


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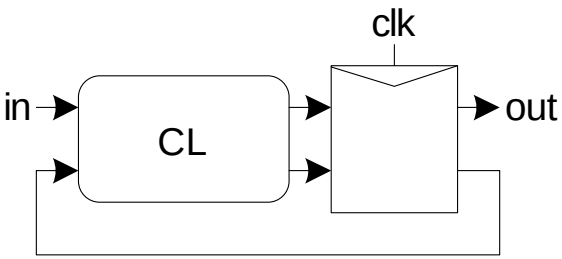
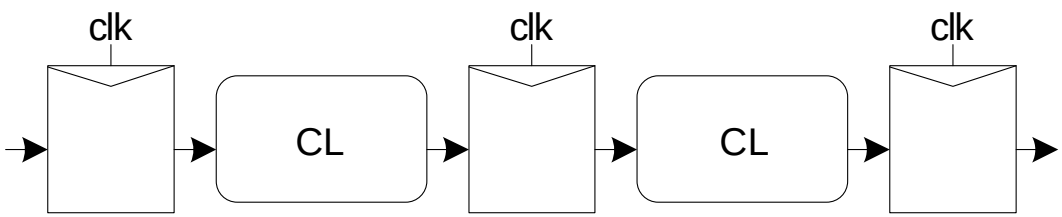


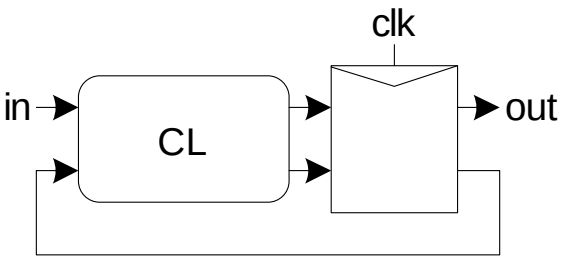

Finite State Machine




Pipeline

# Sequencing

- Combinational logic
  - output depends on current inputs
- Sequential logic
  - output depends on current and previous inputs
  - Requires separating previous, current, future
  - Called state or tokens
  - Ex: FSM, pipeline

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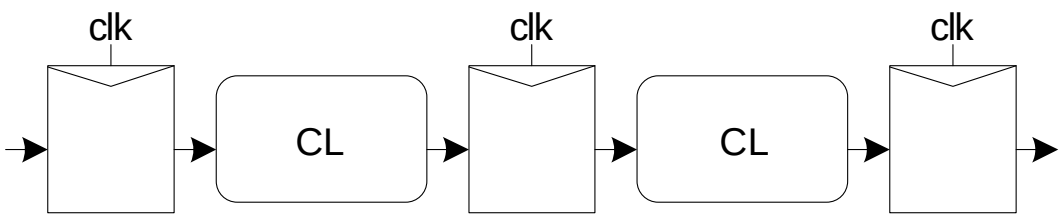


Pipeline

# Sequencing contd.

- If tokens moved through pipeline at constant speed, no sequencing elements would be necessary
- Ex: fiber-optic cable
  - Light pulses (tokens) are sent down cable
  - Next pulse sent before first reaches end of cable
  - No need for hardware to separate pulses
  - But dispersion sets min time between pulses
- This is called wave pipelining in circuits
- In most circuits, dispersion is high
  - Delay fast tokens so they don't catch slow ones.

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# Sequencing Overhead

- Use flip-flops to delay fast tokens so they move through exactly one stage each cycle.
- Inevitably adds some delay to the slow tokens
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- Some people call this clocking overhead
  - But it applies to asynchronous circuits too
  - Inevitable side effect of maintaining sequence

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# Sequencing Elements

- Latch: Level sensitive
  - a.k.a. transparent latch, D latch
- Flip-flop: edge triggered
  - a.k.a. master-slave flip-flop, D flip-flop, D register

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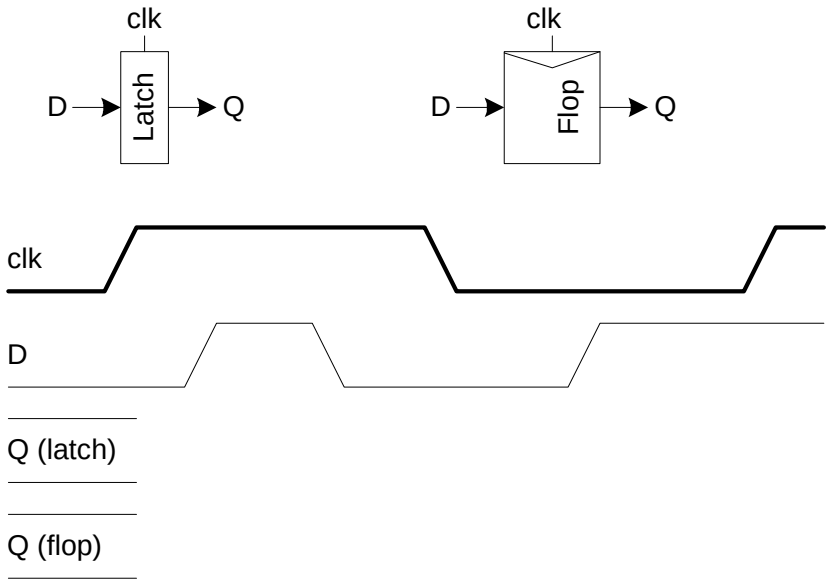
# Timing Diagrams

- Transparent
- Opaque
- Edge-trigger



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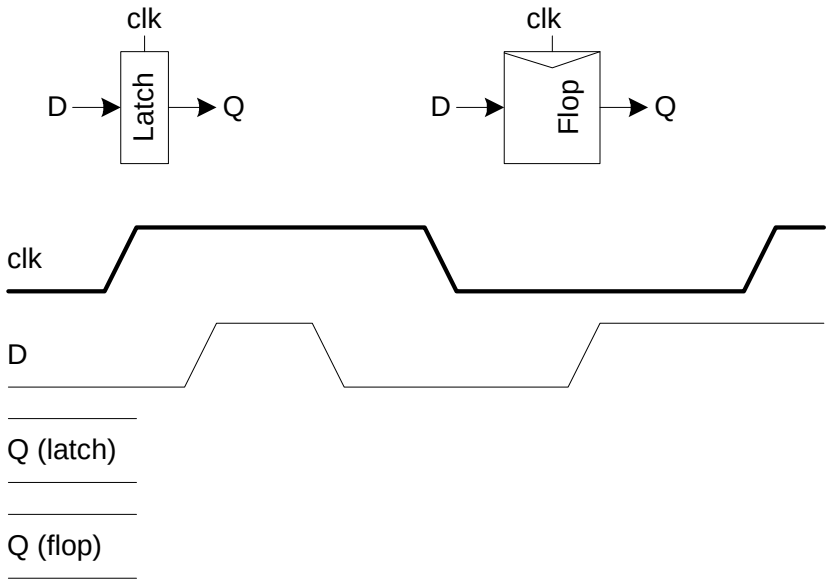

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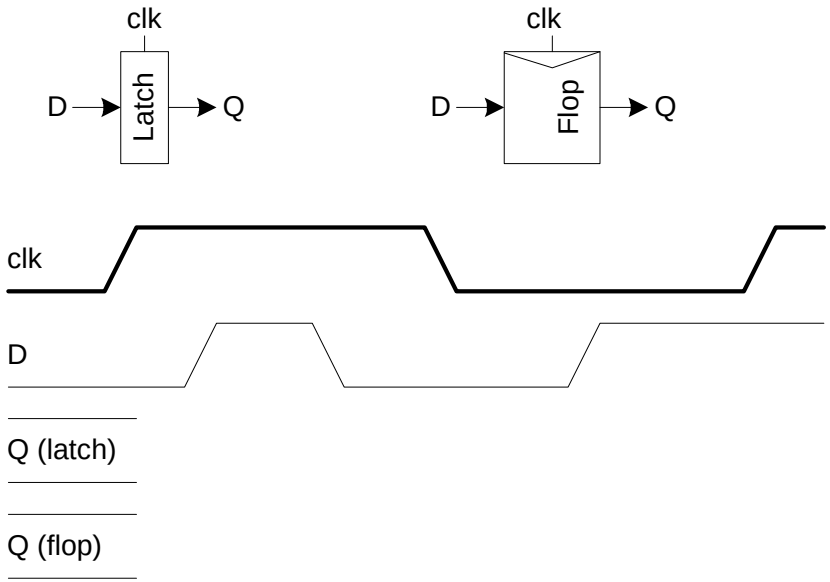

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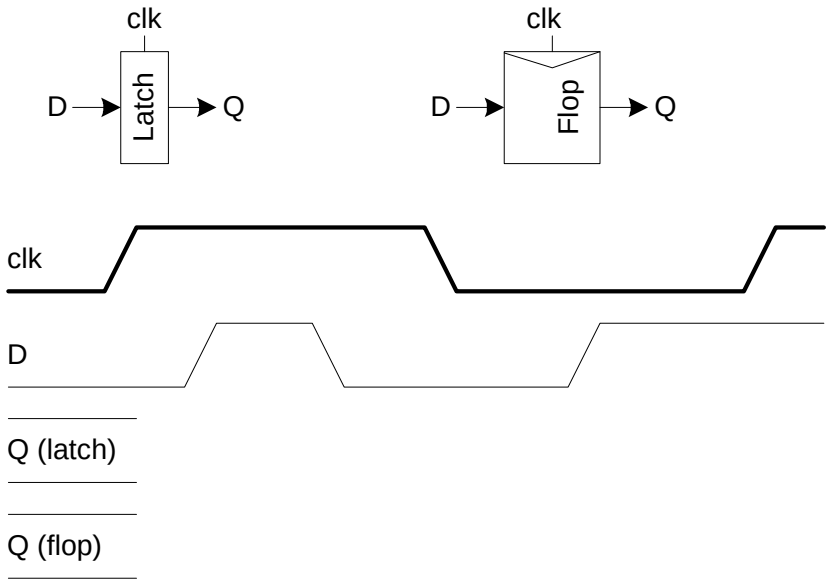

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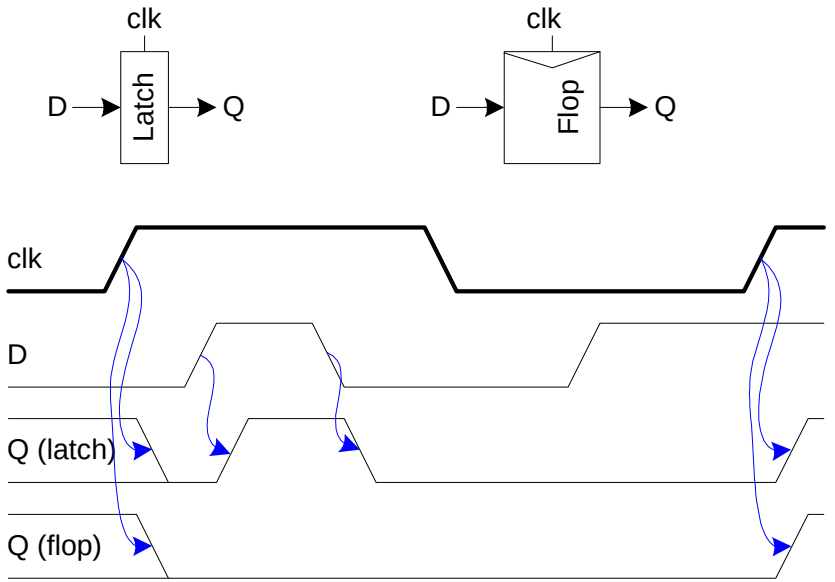
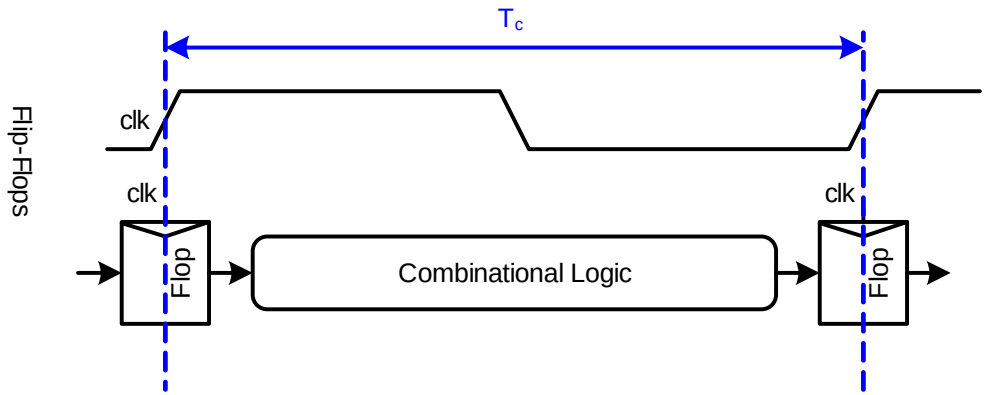


# Sequencing Methods

- Flip-flops
- 2-phase latches
- Pulsed Latches



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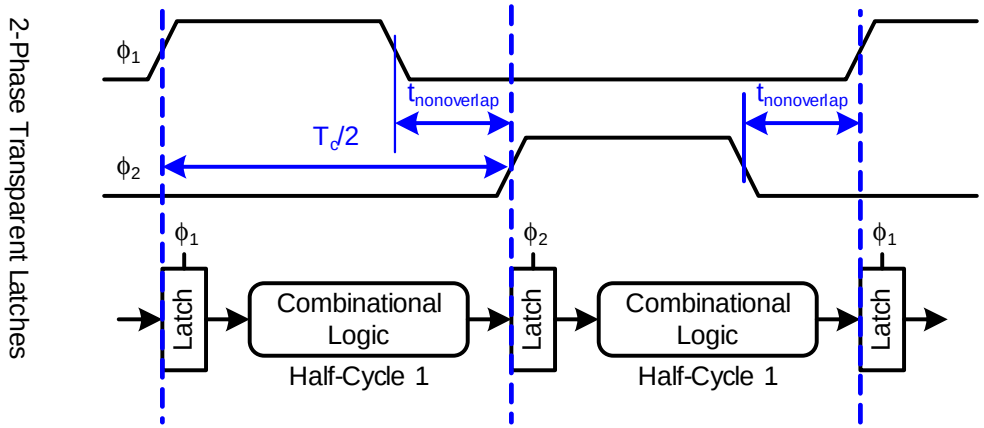

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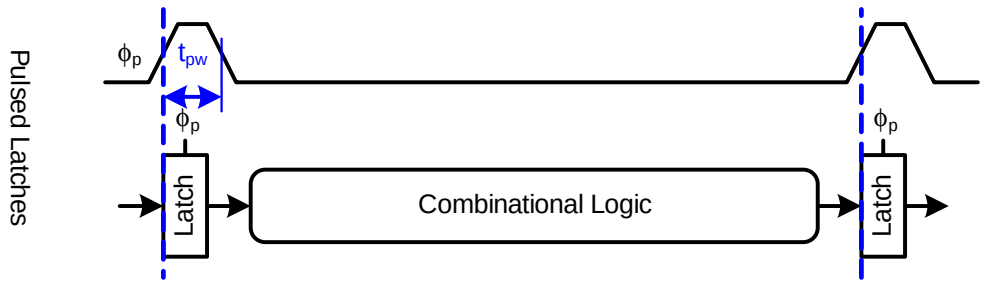

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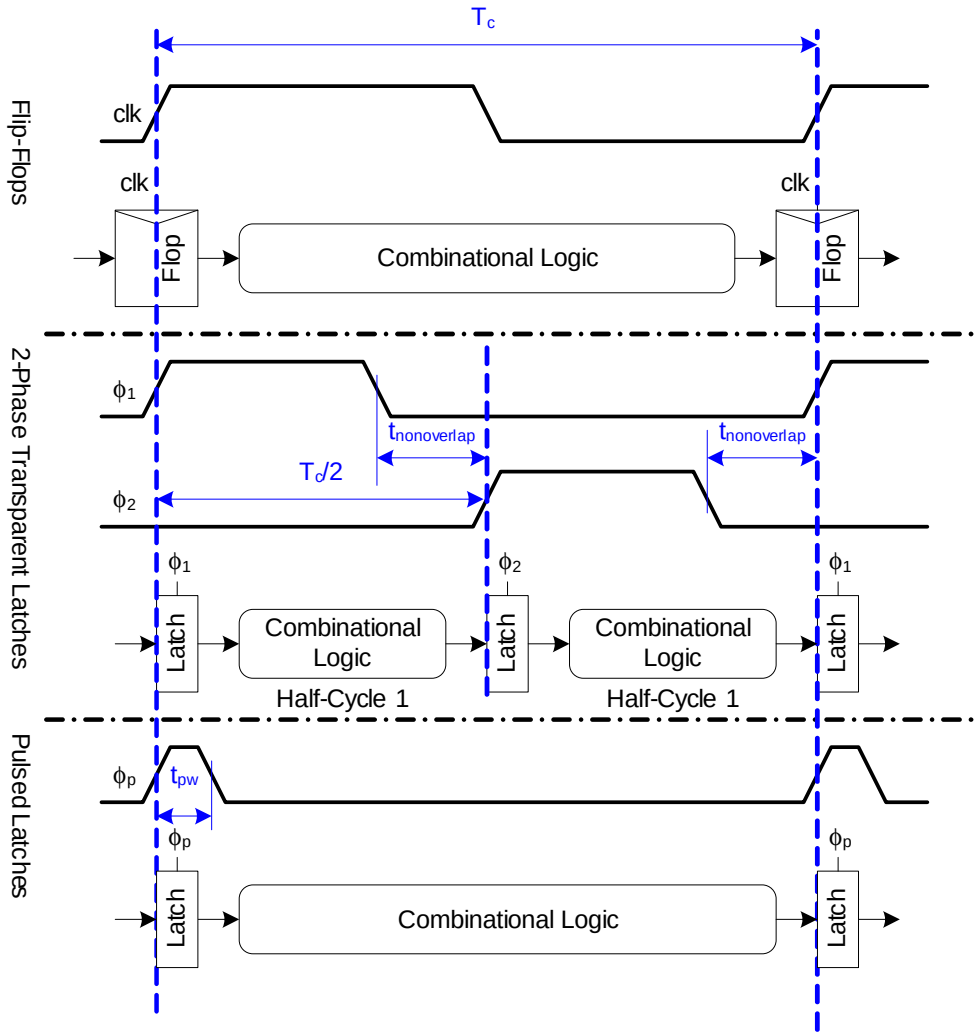
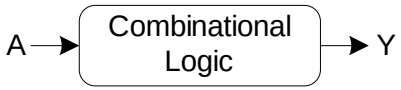
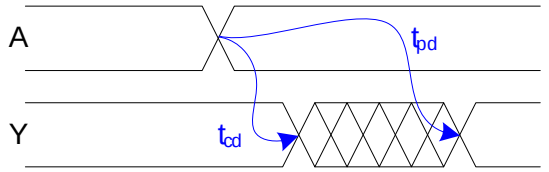


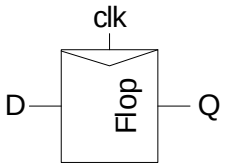
# Timing Diagrams

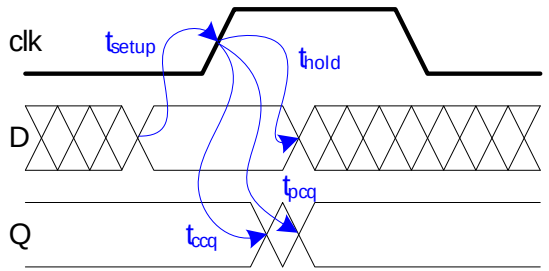
| | |
|---|---|
| $t_{pd}$ | Logic Prop. Delay |
| $t_{cd}$ | Logic Cont. Delay |
| $t_{pcq}$ | Latch/Flop Clk->Q Prop. Delay |
| $t_{ccq}$ | Latch/Flop Clk->Q Cont. Delay |
| $t_{pdq}$ | Latch D->Q Prop. Delay |
| $t_{cdq}$ | Latch D->Q Cont. Delay |
| $t_{setup}$ | Latch/Flop Setup Time |
| $t_{hold}$ | Latch/Flop Hold Time |

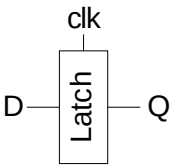
Table: Contamination and Propagation Delays

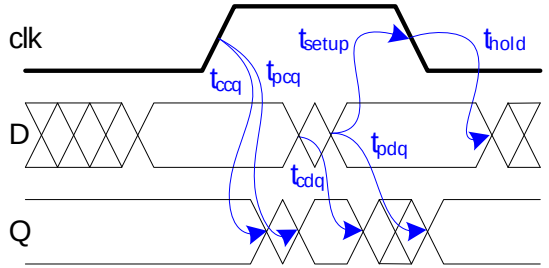


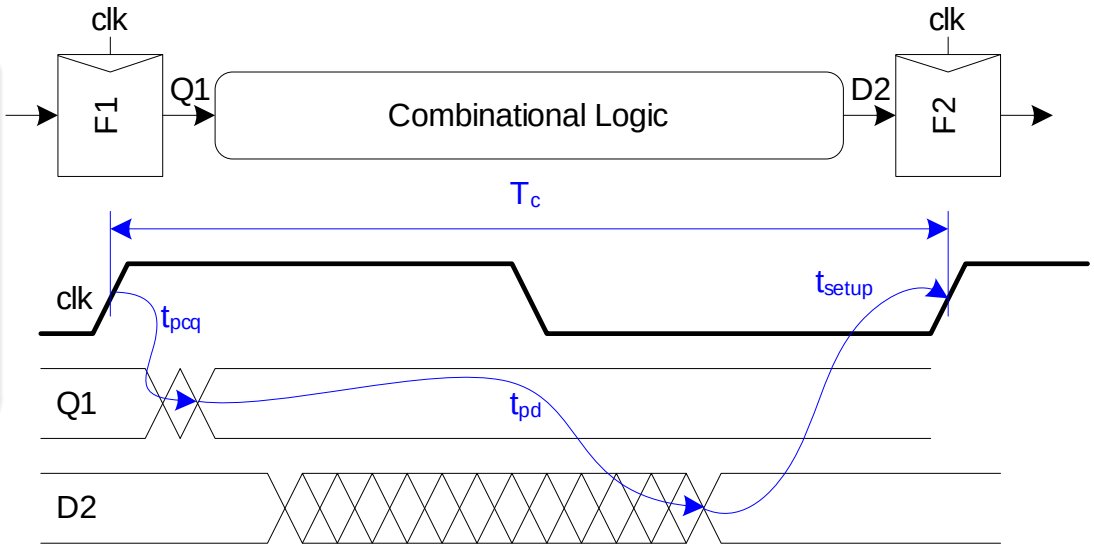



# Max-Delay:Flip-Flops

- $t_{pd} \leq T_c - (?)$
- $t_{pd} \leq T_c - (t_{setup} + t_{pcq})$
- $(t_{setup} + t_{pcq})$ is the sequencing overhead
- setup check



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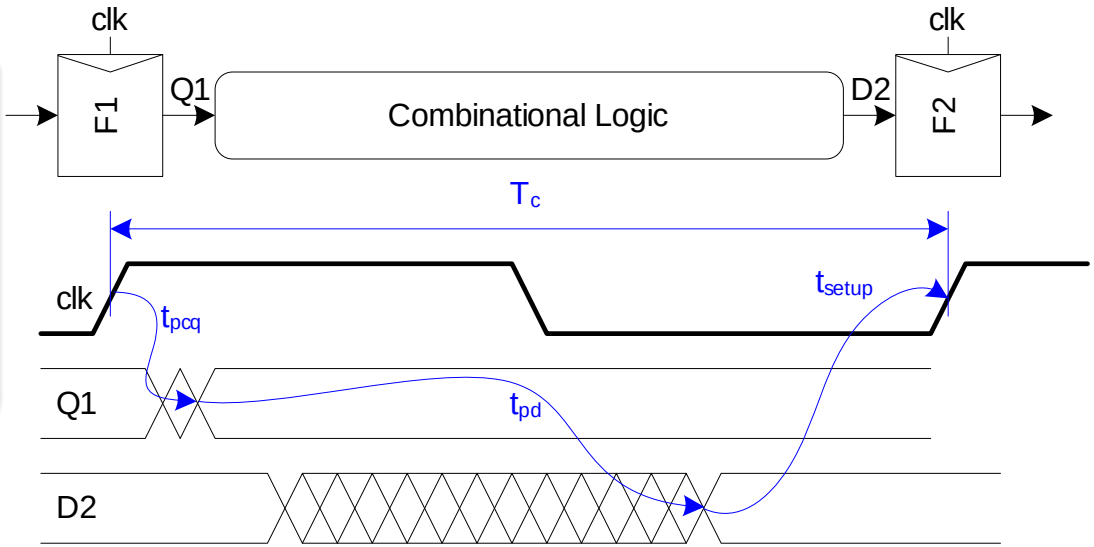

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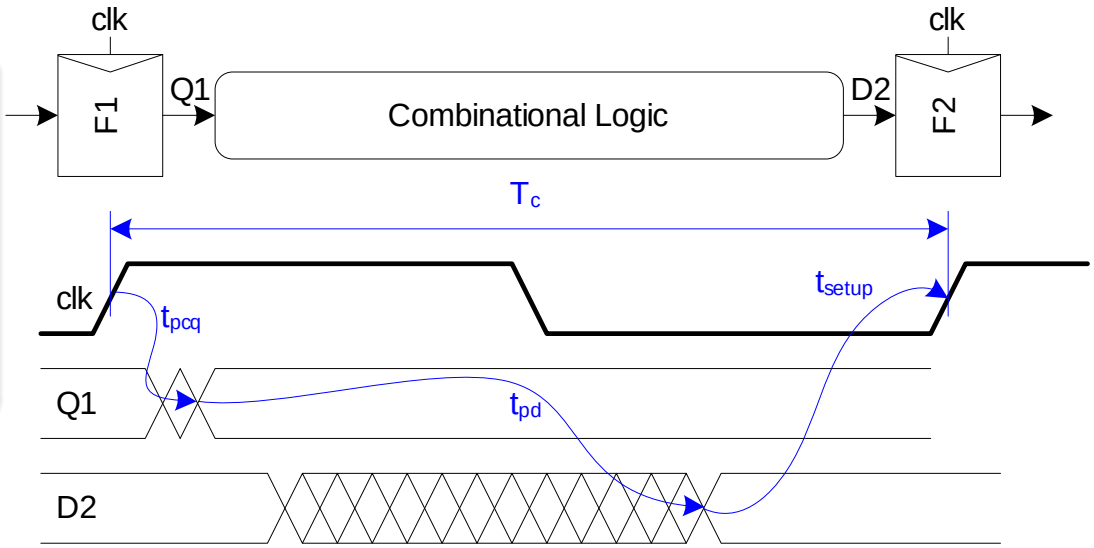

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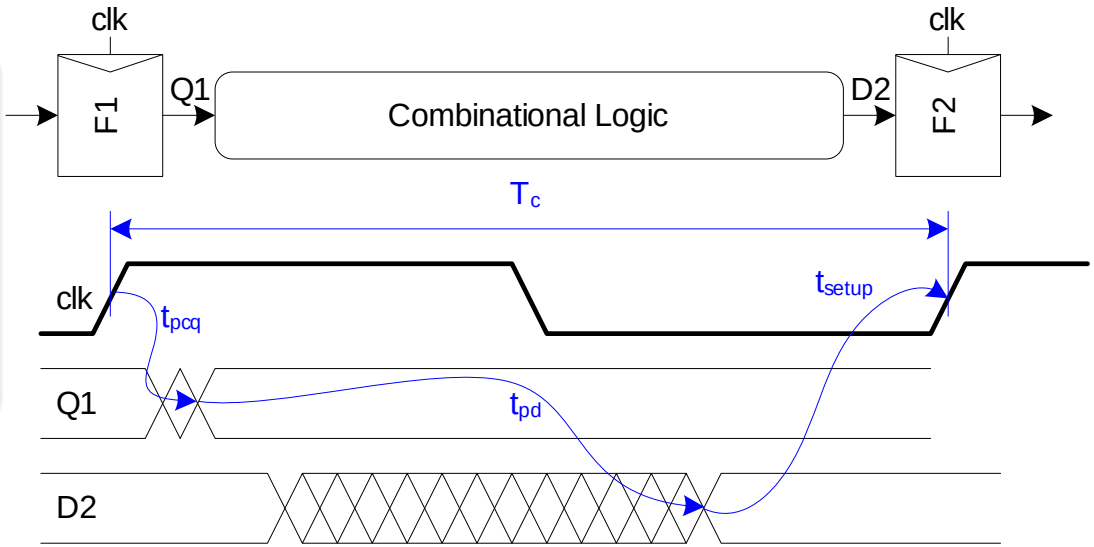

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- $t_{cd} \geq ?$
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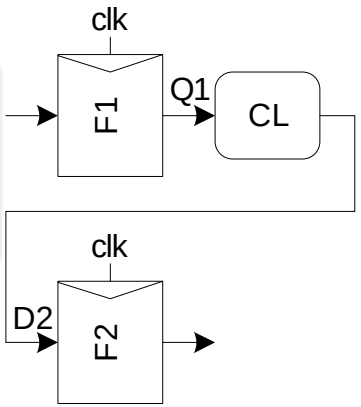
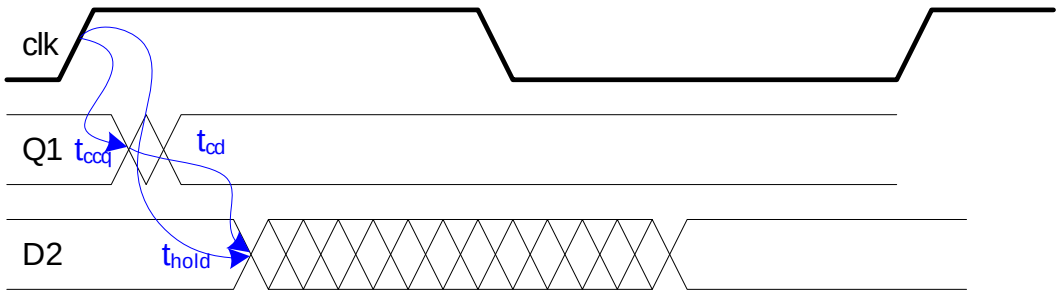
- hold check



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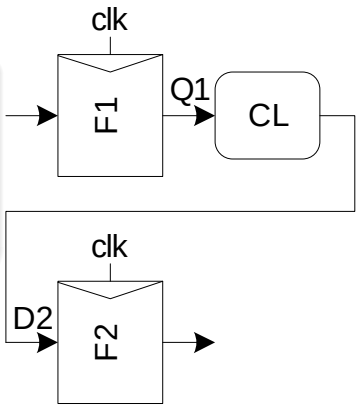


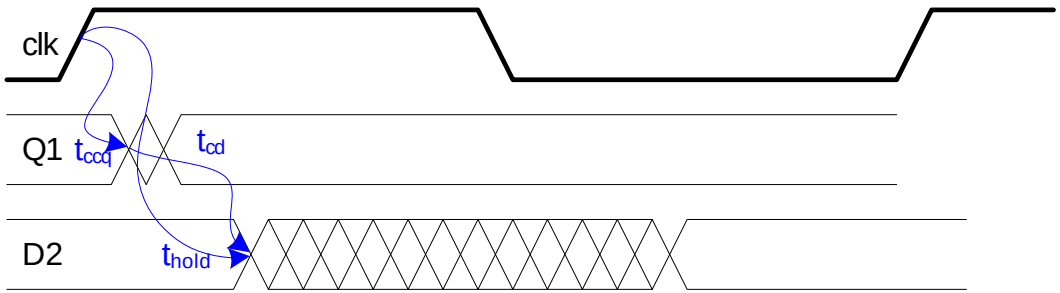

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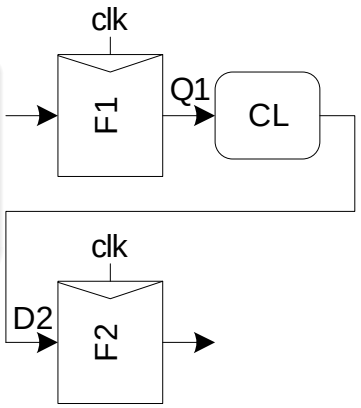


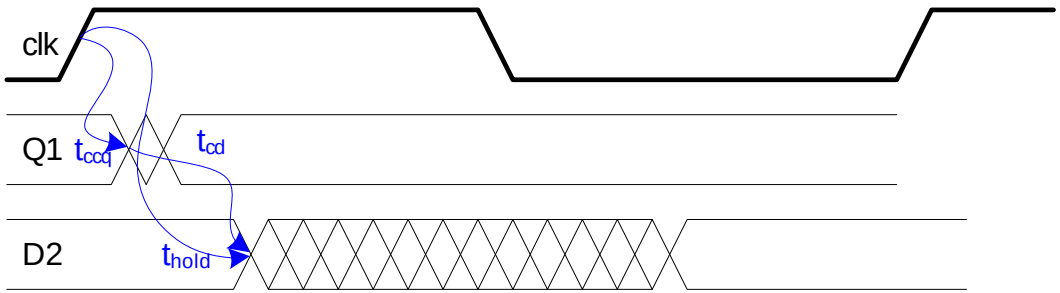

# References I



N. Weste and D. Harris, CMOS VLSI Design: A circuits and systems perspective, 4th Ed., Addison-Wesley, 2010.


R. J. Baker, CMOS Circuit Design, Layout and Simulation, revised 2nd Edition, Wiley-IEEE, 2008.