CMOS Scaling

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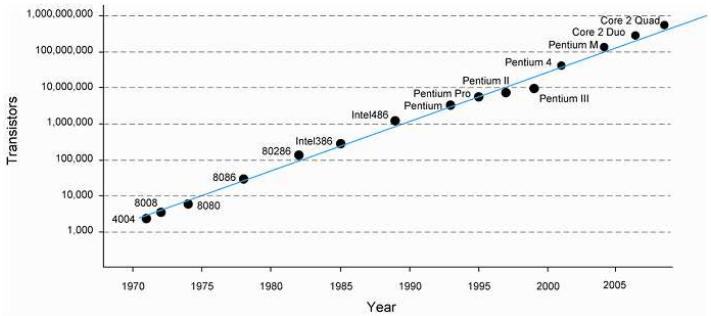
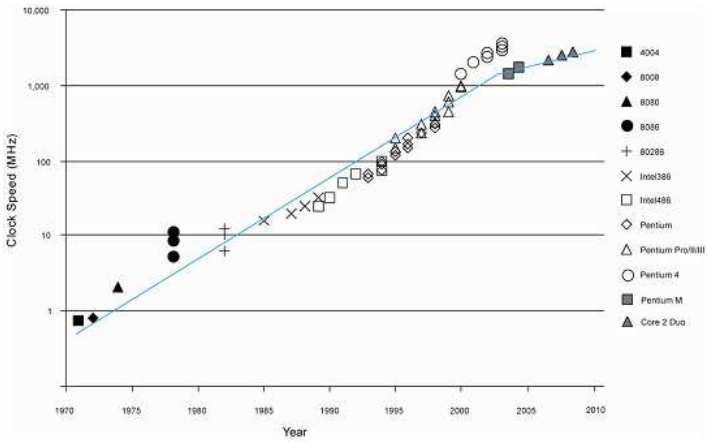
Oct 18, 2010

Moore's Law

- According to the empirical Moore's Law, the number of transistors on in integrated circuit (IC) double approximately evey two years



Moore's law today



Clock speeds have improved

CMOS Scaling

- The increase in density of transistors is achieved by CMOS scaling
  - the minimum channel length (L) is roughly scaled by a factor $S = \frac{1}{\sqrt{2}}$ in every generation
- Two paradigms for device scaling:
  - 1) Constant field scaling
  - 2) Constant voltage scaling
- In practice a combination of both is used to scale CMOS devices

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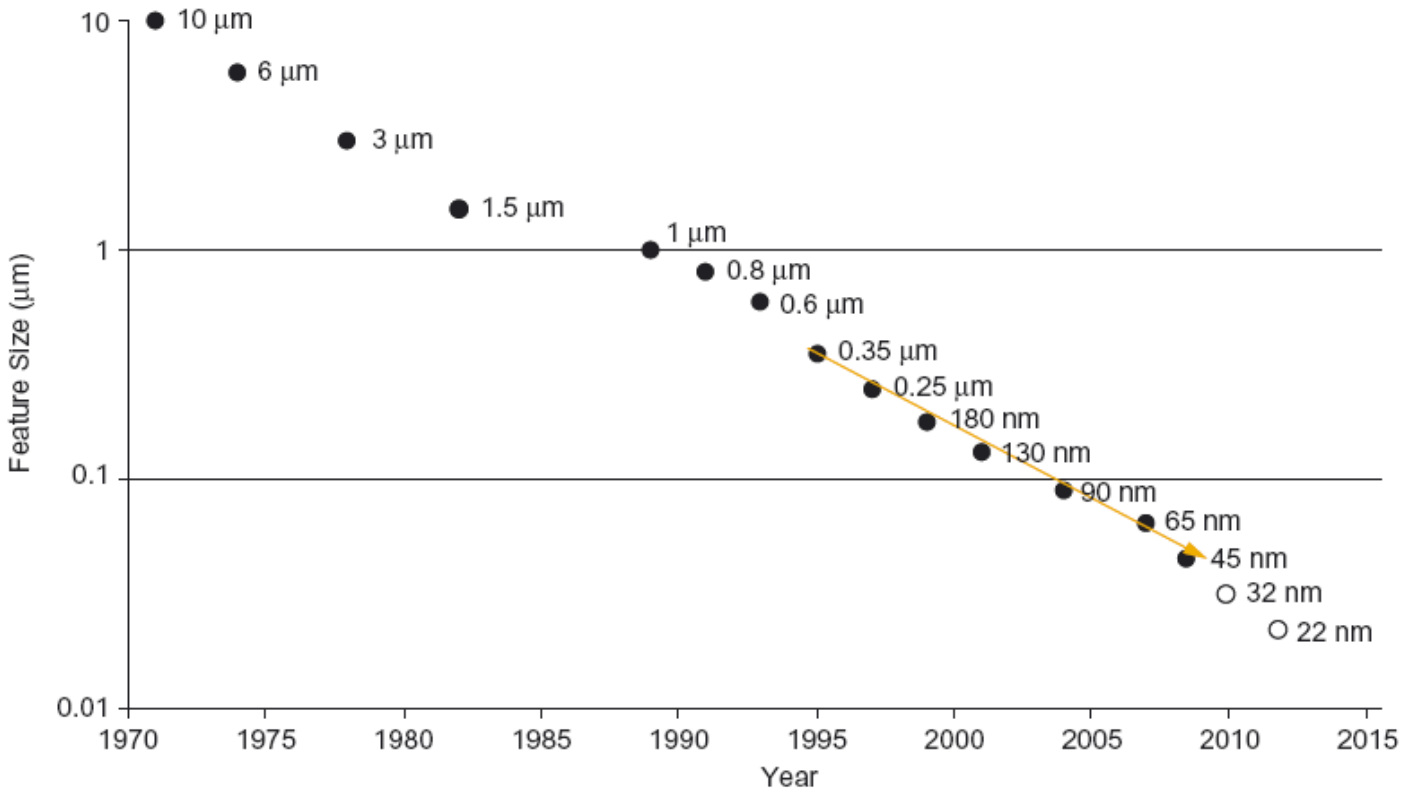
CMOS Nodes with Scaling



Influence of Scaling on CMOS Devices

Parameter	Sensitivity	Scaling Factor
Length: L		S
Width: W		S
GOX thickness: t_{ox}		S
Supply Voltage: V_{DD}		S
Threshold voltage: $V_{THN/P}$		S
Substrate doping: N_A		1/S
β	$\frac{W}{L}\frac{1}{t_{ox}}$	1/S
Current: I_{on}	$\beta(V_{DD}-V_{TH})^2$	S
Resistance: R	$\frac{V_{DD}}{I_{on}}$	1
Gate capacitance: C_{ox}	$\frac{WL}{t_{ox}}$	S
Gate delay: τ	$R \cdot C_{ox}$	S
Clock frequency: f_{clk}	$\frac{1}{\tau}$	1/S

Table: CMOS Scaling

Influence of Scaling on CMOS Devices contd.

Parameter	Sensitivity	Scaling Factor
Dynamic power dissipation: P	$CV^2 f_{clk}$	S^2
Chip area: A	$\sim WL$	S^2
Power density	P/A	1
Current density	I_{on}/A	1/S

Table: CMOS Scaling contd.