CMOS Inverter

Additional Slides

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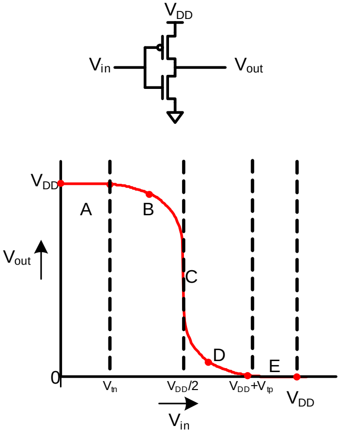
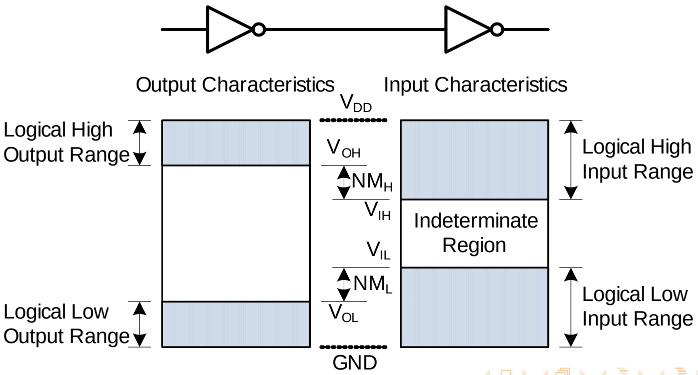
Inverter Operation Regions

Region	NMOS	PMOS
A	Cutoff	Triode
B	Saturation	Triode
C	Saturation	Saturation
D	Triode	Saturation
E	Triode	Cutoff



Noise Margin

- How much noise can a gate input see before it does not recognize the output?
  - Noise margins of a digital gate indicate how well it will perform with noisy input



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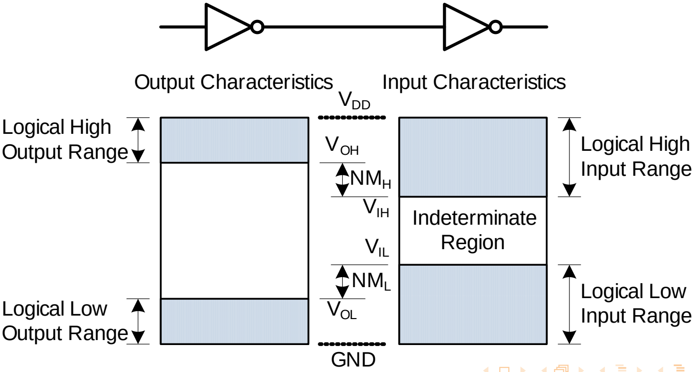

Noise Margin

- $NM_H = V_{IH} - V_{OH}$
  - HIGH noise margin
- $NM_L = V_{IL} - V_{OL}$
  - LOW noise margin
- V_{IH} = minimum HIGH input voltage
- V_{IL} = maximum LOW input voltage
- V_{OH} = minimum HIGH output voltage
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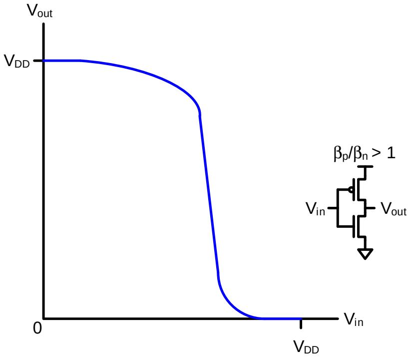
Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristics



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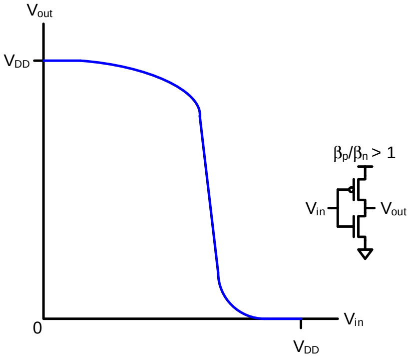

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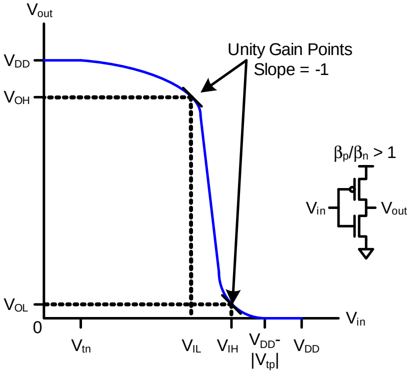

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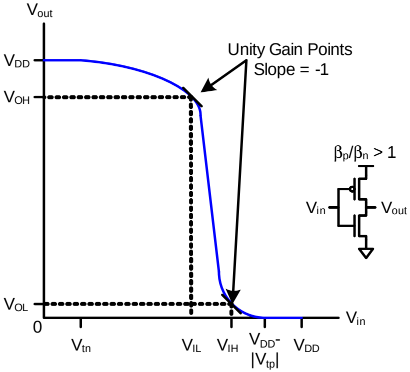

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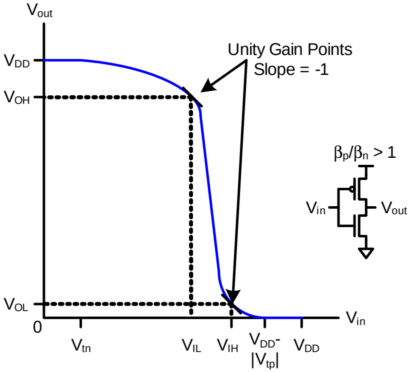
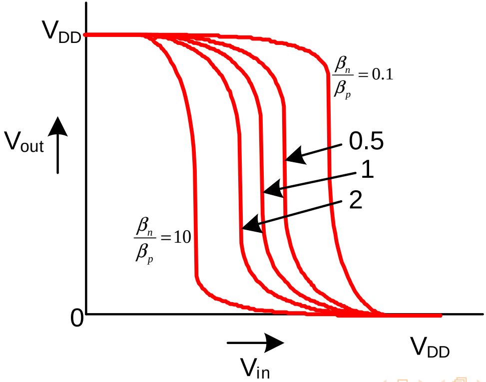


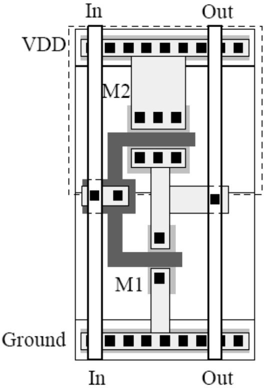
Beta-Ratio

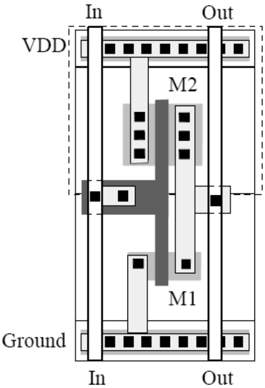
- If $\frac{\beta_n}{\beta_p} \neq 1$, inverter's switching point (V_{SP}) will move from the ideal value of $\frac{V_{DD}}{2}$
  - called skewed gate



Inverter Layout

- Two styles for laying out an inverter
- Power and ground routed on metal-1 using standard frame





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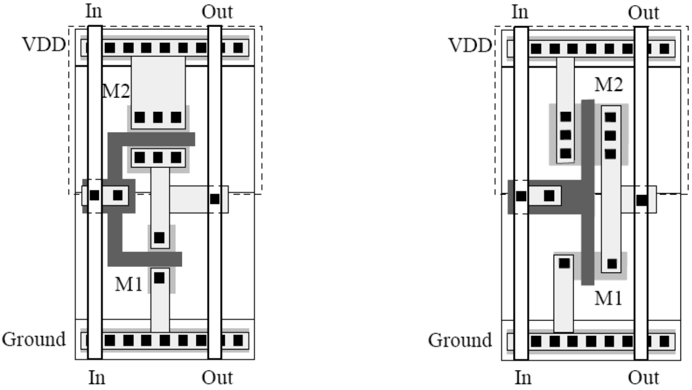
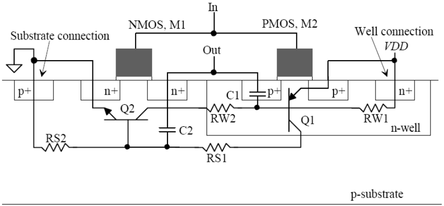
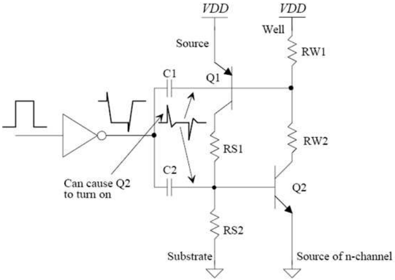


Latch-up

- Fast voltage pulses can feed-through the C1 or C2 and turn on the parasitic BJT
- If any of the BJT is turned on, it creates a positive feedback loop
  - eventually both the BJTs are turned fully on and the circuit is stuck in that state (undesired)



Cross-sectional view of an inverter showing parasitic bipolar transistors and resistors



Schematic for understanding latch-up

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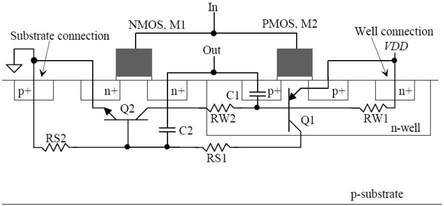

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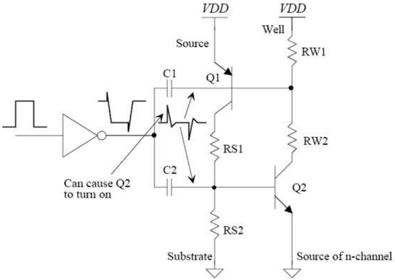

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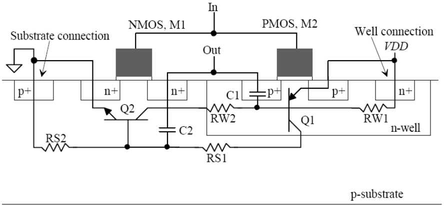

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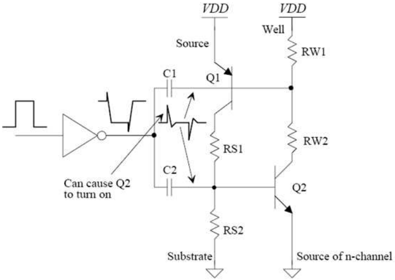

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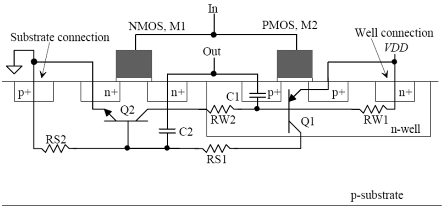
Latch-up prevention

- Reduce the well series resistances (RW1 and RW2) by using as many contacts as possible and closer to the inverter
    - can also use guard ring structures
- Use slow rise and fall times in the logic
- Reduce drain areas to reduce C1 and C2



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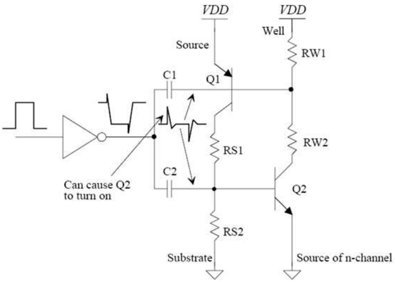

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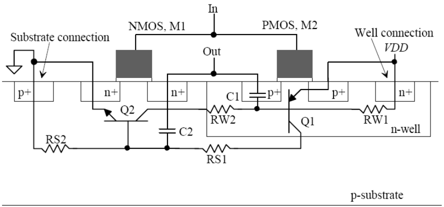

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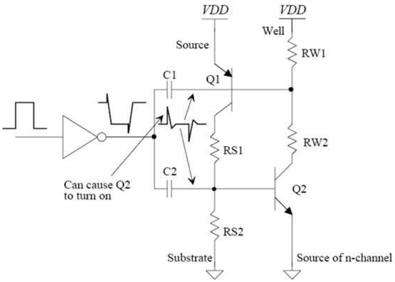

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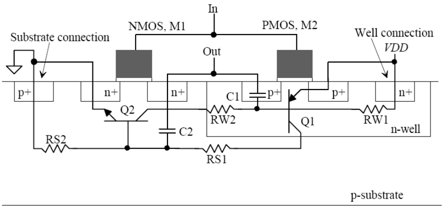

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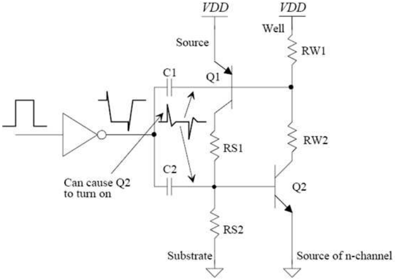

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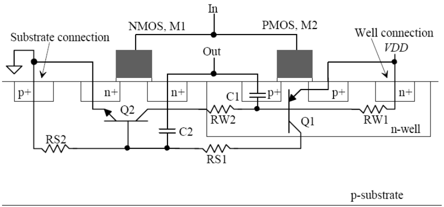

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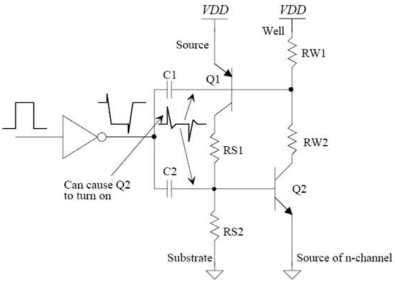

Schematic for understanding latch-up

Normalized Inverter Delay

- In nm-CMOS, assuming that for equal drive strengths $W_p = 2W_n$
  - effective switching resistance of PMOS & NMOS = R
  - in MOSFETs swicthing model assume that $C_{in} = C_{out} = C$
- Propgataion delay (d) = $t_{pLH} = t_{pHL} = 0.7 \times R(C_{outp} + C_{outn}) \triangleq 0.7 \times 3RC$
  - $\Rightarrow \tau = 3RC$
- Can express delay in a process-independent unit
  - $d = d_{abs}/0.7\tau$
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- Delay has two components: $d = f + p$
  - f: effort delay $= g \cdot h$ (a.k.a. stage effort)
  - g: logical effort
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Delay Plots

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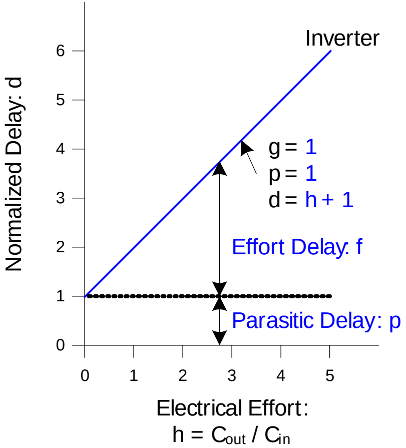

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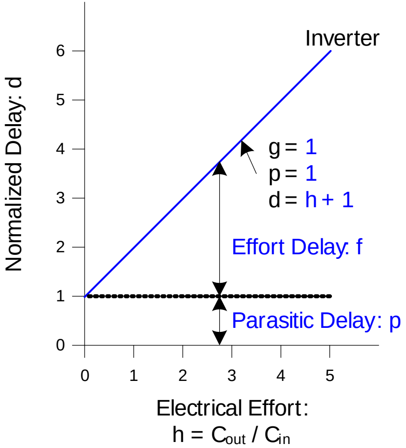

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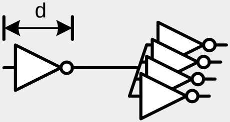
Example: FO4 Inverter

- Estimate the delay of a fanout-of-4 (FO4) inverter



- Logical Effort: g = 1
- Electrical Effort: h = 4
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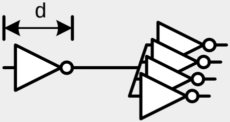

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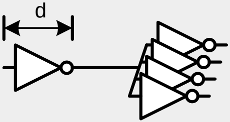

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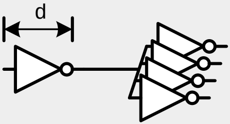

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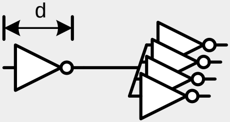

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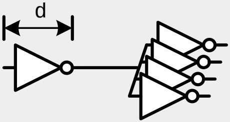

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Multistage Logic Circuits

- Logical effort generalizes to multistage networks
- Path Logical Effort $G = \prod g_i$
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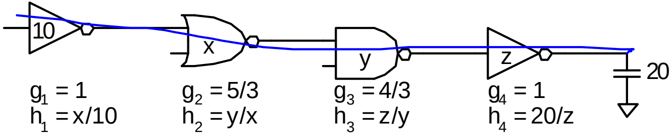
- For a single path (no branching): $F = G \cdot H$



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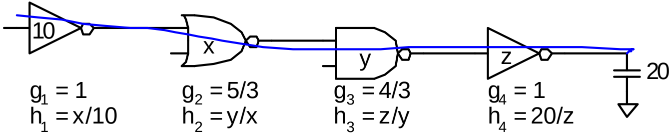

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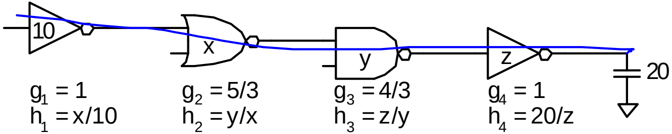

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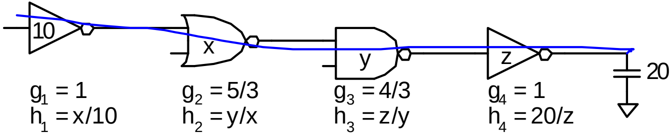

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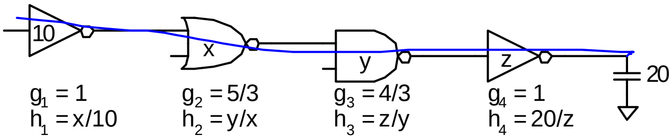

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- How many stages should a buffer use?
  - Minimizing number of stages is not always fastest
- Example: drive $64 \times C$ load with unit inverter
  - $D = NF^{\frac{1}{N}} + P$
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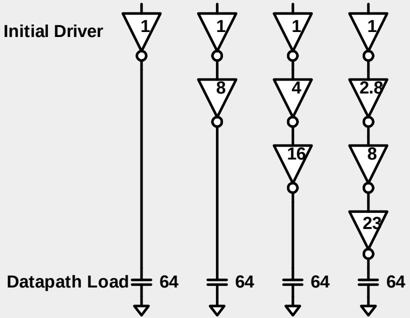

N:
f:
D:

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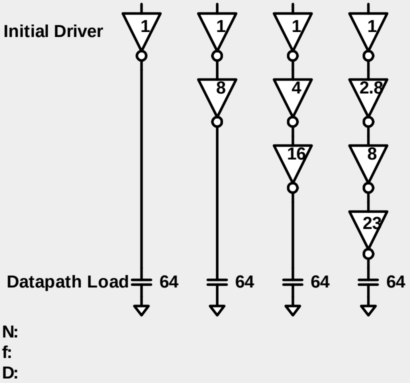

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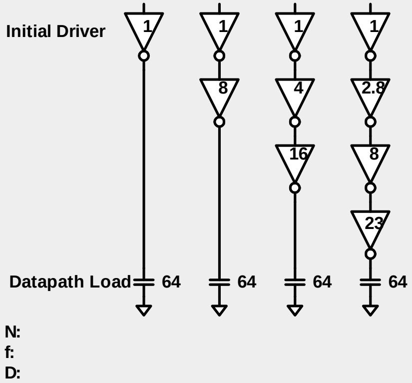

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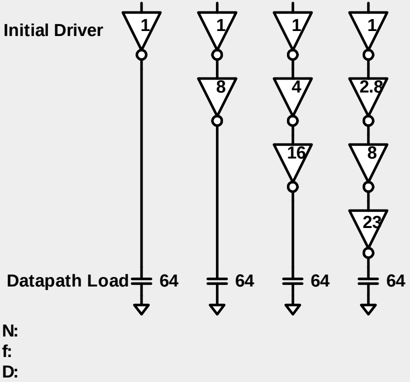

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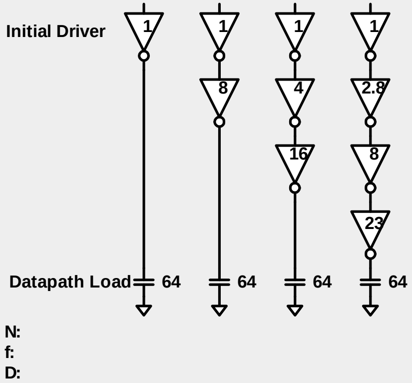

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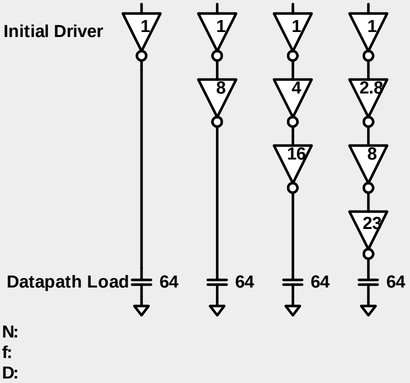

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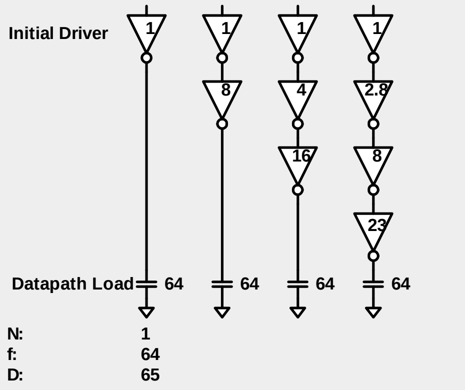

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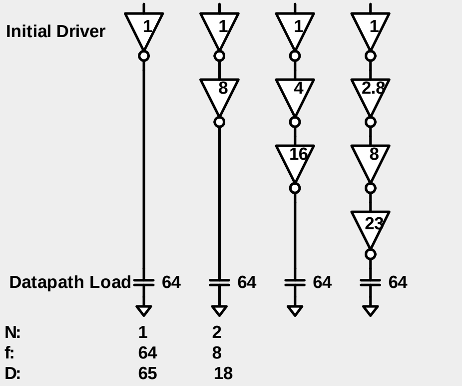

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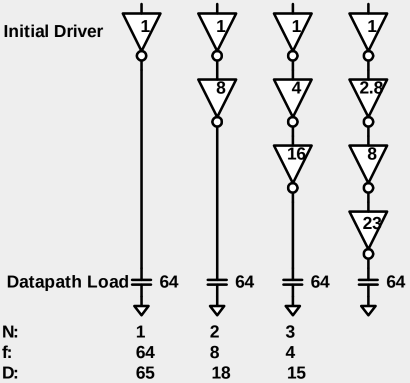

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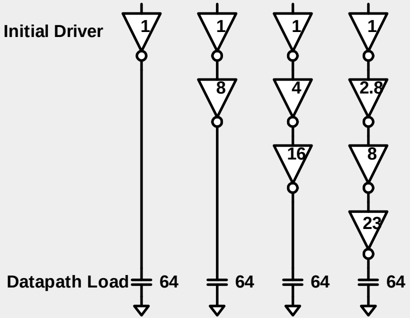

N:	1	2	3	4
f:	64	8	4	2.8
D:	65	18	15	15.3

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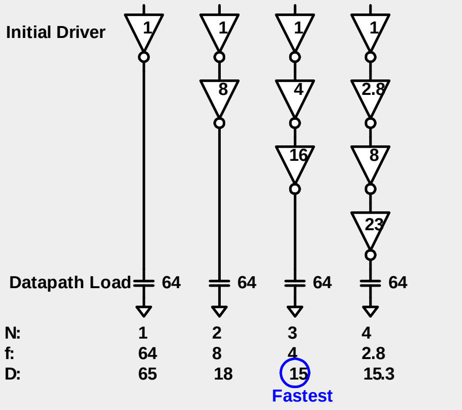

Derivation

- How many inverters in a buffer give the least delay?
- For N inverters: $D = NF^{\frac{1}{N}} + N \cdot p_{inv}$
  - p_{inv} is the parasitic delay of the inverter, F is the path effort
  - Path Effort: $F = G \cdot H = \frac{C_{out}}{C_{in1}}$
- Minimize delay: $\frac{\partial D}{\partial N} = -F^{\frac{1}{N}} \cdot ln\left(F^{\frac{1}{N}}\right) + F^{\frac{1}{N}} + p_{inv} = 0$
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Best Stage Effort

- $p_{inv} + \rho(1 - ln\rho) = 0$ has no closed form solution
- Neglecting parasitics ($p_{inv} = 0$) we find $\rho = e = 2.718$
- For $p_{inv} = 1$, numerical solution yields $\rho = 3.59$
- Least delay for:
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  - and when using $\hat{N} = log_{\rho} F$
  - $= log_4 F = log_4 \left(\frac{C_{out}}{C_{in1}}\right)$
- Rule of thumb: Fan-out of 4 (FO4) stage effort results in fastest path

Best Stage Effort

- $p_{inv} + \rho(1 - ln\rho) = 0$ has no closed form solution
- Neglecting parasitics ($p_{inv} = 0$) we find $\rho = e = 2.718$
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- How sensitive is delay to using exactly the best number of stages?
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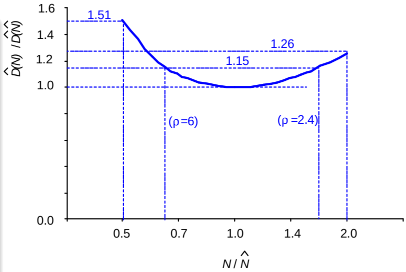

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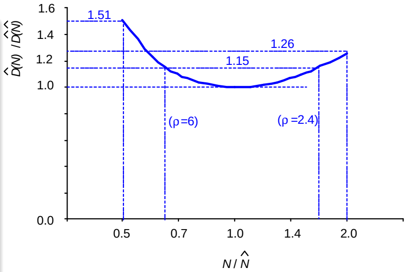

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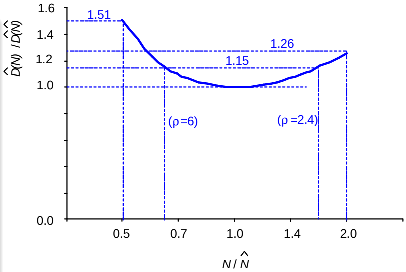

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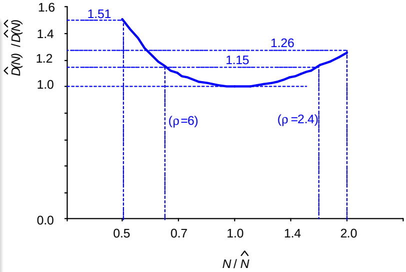

Method of Logical Effort

- Note that for the buffer design problem: $G = B = 1$, $g_i = 1$, and $F = H = \frac{C_{out}}{C_{in_1}}$

Minimizing Layout Area?

- Total transistor area can be roughly estimated as $A = A_1 \sum_{i=0}^{N-1} \left(\hat{f}\right)^N$, where A_1 is the area of the first inverter.
- The area can be minimized for a specified delay (D_0) by optimizing the following set of constraints
  - $$minimize \frac{\left(\hat{f}\right)^N - 1}{\hat{f} - 1}$$
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References I

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